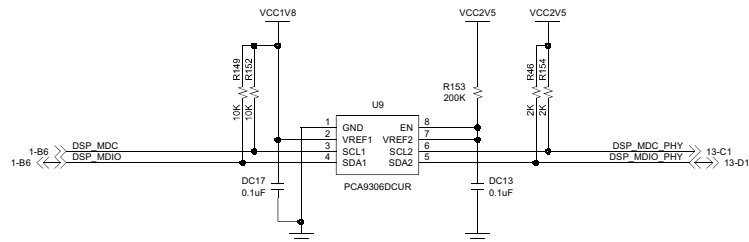
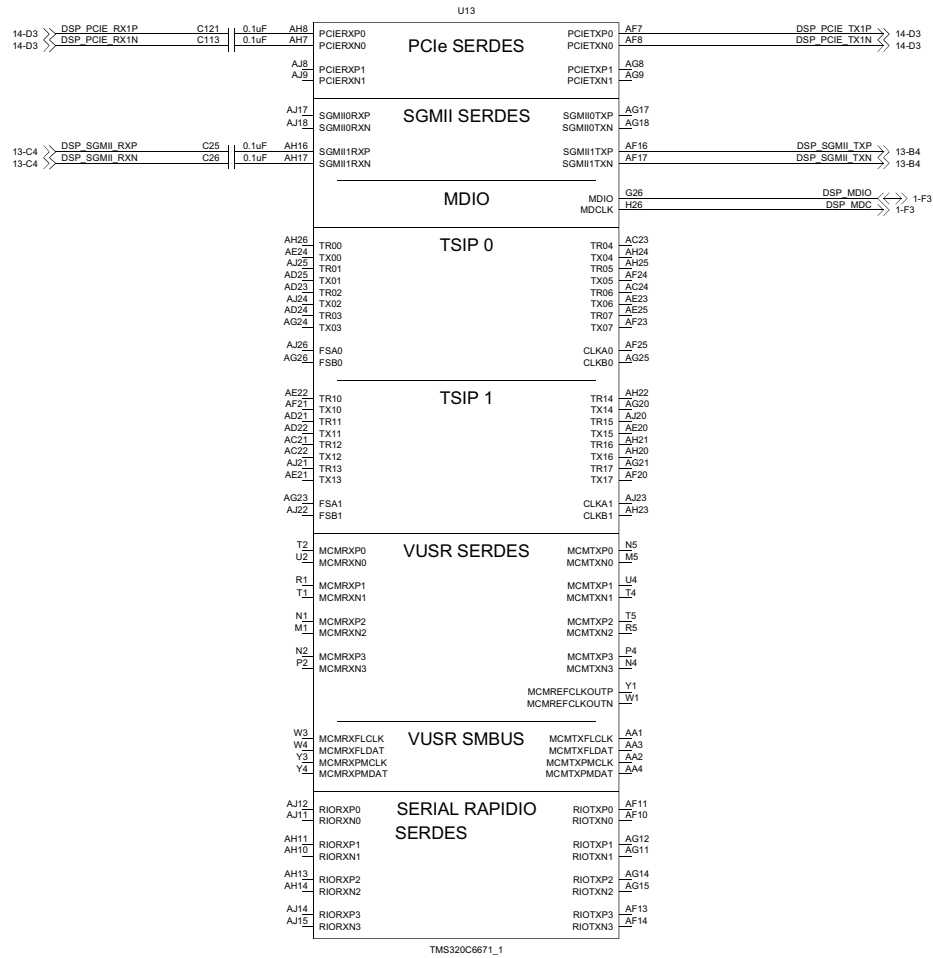


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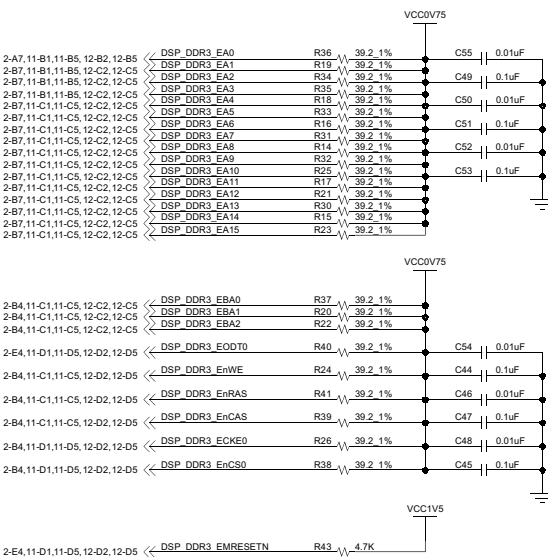
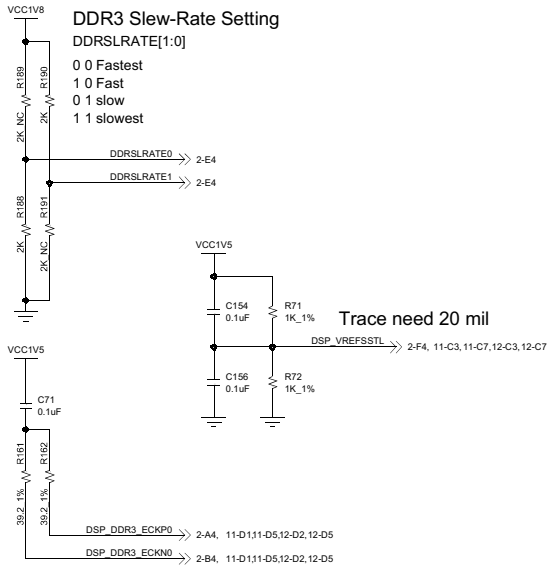
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### DDR3 Slew-Rate Setting

DDRSLRATE[1:0]

- 0 0 Fastest
- 1 0 Fast
- 0 1 slow
- 1 1 slowest



U13		U13		U13		U13	
2-C2, 11-D1, 11-D5, 12-D2, 12-D5	<< DSP_DDR3_ECKP0	A12	DORCLKOUTP0	A14	DSP_DDR3_EA0	2-D2, 11-B1, 11-B5, 12-C2, 12-E	
2-C2, 11-D1, 11-D5, 12-D2, 12-D5	<< DSP_DDR3_ECKN0	B12	DORCLKOUTN0	F14	DSP_DDR3_EA1	2-D2, 11-B1, 11-B5, 12-C2, 12-E	
		A16	DORCLKOUTP1	F13	DSP_DDR3_EA2	2-D2, 11-B1, 11-B5, 12-C2, 12-E	
		B16	DORCLKOUTN1	A15	DSP_DDR3_EA3	2-D2, 11-B1, 11-B5, 12-C2, 12-E	
2-F2, 11-D1, 11-D5, 12-D2, 12-D5	<< DSP_DDR3_ECKE0	D11	DORCKE0	C15	DSP_DDR3_EA4	2-D2, 11-C1, 11-C5, 12-C2, 12-E	
		E18	DORCKE1	B15	DSP_DDR3_EA5	2-D2, 11-C1, 11-C5, 12-C2, 12-E	
2-F2, 11-D1, 11-D5, 12-D2, 12-D5	<< DSP_DDR3_EnCS0	C11	DORNCAS	D15	DSP_DDR3_EA6	2-D2, 11-C1, 11-C5, 12-C2, 12-E	
		C12	DORNCAS	F15	DSP_DDR3_EA7	2-D2, 11-C1, 11-C5, 12-C2, 12-E	
2-F2, 11-C1, 11-C5, 12-D2, 12-D5	<< DSP_DDR3_EnCAS	D12	DORNCAS	E15	DSP_DDR3_EA8	2-D2, 11-C1, 11-C5, 12-C2, 12-E	
2-E2, 11-C1, 11-C5, 12-D2, 12-D5	<< DSP_DDR3_EnRAS	C10	DORNRAS	E16	DSP_DDR3_EA9	2-D2, 11-C1, 11-C5, 12-C2, 12-E	
2-E2, 11-C1, 11-C5, 12-D2, 12-D5	<< DSP_DDR3_EnWE	E12	DORNRAS	D16	DSP_DDR3_EA10	2-D2, 11-C1, 11-C5, 12-C2, 12-E	
			DORNRAS	E17	DSP_DDR3_EA11	2-E2, 11-C1, 11-C5, 12-C2, 12-E	
2-E2, 11-C1, 11-C5, 12-C2, 12-C5	<< DSP_DDR3_EBA0	A13	DORBA0	C16	DSP_DDR3_EA12	2-E2, 11-C1, 11-C5, 12-C2, 12-E	
2-E2, 11-C1, 11-C5, 12-C2, 12-C5	<< DSP_DDR3_EBA1	B13	DORBA1	C16	DSP_DDR3_EA13	2-E2, 11-C1, 11-C5, 12-C2, 12-E	
2-E2, 11-C1, 11-C5, 12-C2, 12-C5	<< DSP_DDR3_EBA2	C13	DORBA2	D17	DSP_DDR3_EA14	2-E2, 11-C1, 11-C5, 12-C2, 12-E	
			DORBA2	C17	DSP_DDR3_EA15	2-E2, 11-C1, 11-C5, 12-C2, 12-E	
11-D1	<< DSP_DDR3_EDM0	E29	DORDM0	E28	DSP_DDR3_ED00	11-C3	
11-D1	<< DSP_DDR3_EDM1	C27	DORDM1	D28	DSP_DDR3_ED01	11-C3	
11-D1	<< DSP_DDR3_EDM2	A25	DORDM2	E27	DSP_DDR3_ED02	11-C3	
11-D1	<< DSP_DDR3_EDM3	A22	DORDM3	D28	DSP_DDR3_ED03	11-C3	
11-D1	<< DSP_DDR3_EDM4	A10	DORDM4	D27	DSP_DDR3_ED04	11-C3	
11-D1	<< DSP_DDR3_EDM5	A8	DORDM5	B28	DSP_DDR3_ED05	11-C3	
12-D2	<< DSP_DDR3_EDM6	B5	DORDM6	F25	DSP_DDR3_ED06	11-C3	
12-D2	<< DSP_DDR3_EDM7	B2	DORDM7	F24	DSP_DDR3_ED07	11-C3	
12-D5	<< DSP_DDR3_EDM7	B5	DORDM7	E24	DSP_DDR3_ED08	11-C3	
		A20	DORDM8	E25	DSP_DDR3_ED09	11-C3	
			DORDM8	E26	DSP_DDR3_ED10	11-C3	
11-D1	<< DSP_DDR3_EDOSP0	C28	DOROS0P	D25	DSP_DDR3_ED11	11-C3	
11-D1	<< DSP_DDR3_EDOSN0	C29	DOROS0N	D26	DSP_DDR3_ED12	11-C3	
			DOROS0N	B26	DSP_DDR3_ED13	11-C3	
11-D1	<< DSP_DDR3_EDOSP1	A27	DOROS1P	A26	DSP_DDR3_ED14	11-C3	
11-D1	<< DSP_DDR3_EDOSN1	B27	DOROS1N	B27	DSP_DDR3_ED15	11-C3	
			DOROS1N	A23	DSP_DDR3_ED16	11-C3	
11-D1	<< DSP_DDR3_EDOSP2	A24	DOROS2P	B23	DSP_DDR3_ED17	11-C3	
11-D1	<< DSP_DDR3_EDOSN2	B24	DOROS2N	B23	DSP_DDR3_ED18	11-C3	
			DOROS2N	B24	DSP_DDR3_ED19	11-C3	
11-D1	<< DSP_DDR3_EDOSP3	A21	DOROS3P	C22	DSP_DDR3_ED20	11-C3	
11-D1	<< DSP_DDR3_EDOSN3	B21	DOROS3N	C22	DSP_DDR3_ED21	11-C3	
			DOROS3N	D22	DSP_DDR3_ED22	11-C3	
12-D2	<< DSP_DDR3_EDOSP4	A9	DOROS4P	E22	DSP_DDR3_ED23	11-C3	
12-D2	<< DSP_DDR3_EDOSN4	B9	DOROS4N	E22	DSP_DDR3_ED24	11-C3	
			DOROS4N	D21	DSP_DDR3_ED25	11-C3	
12-D2	<< DSP_DDR3_EDOSP5	B6	DOROS5P	F21	DSP_DDR3_ED26	11-C3	
12-D2	<< DSP_DDR3_EDOSN5	A6	DOROS5N	F21	DSP_DDR3_ED27	11-C3	
			DOROS5N	D22	DSP_DDR3_ED28	11-C3	
12-D2	<< DSP_DDR3_EDOSP6	B6	DOROS6P	C21	DSP_DDR3_ED29	11-C3	
12-D2	<< DSP_DDR3_EDOSN6	A3	DOROS6N	B22	DSP_DDR3_ED30	11-C3	
			DOROS6N	C22	DSP_DDR3_ED31	11-C3	
12-D5	<< DSP_DDR3_EDOSP7	D1	DOROS7P	E10	DSP_DDR3_ED32	12-D3	
12-D5	<< DSP_DDR3_EDOSN7	C1	DOROS7N	D10	DSP_DDR3_ED33	12-D3	
			DOROS7N	B10	DSP_DDR3_ED34	12-D3	
			DOROS8P	D9	DSP_DDR3_ED35	12-D3	
			DOROS8N	E9	DSP_DDR3_ED36	12-D3	
			DOROS8N	C9	DSP_DDR3_ED37	12-D3	
			DOROS8N	B8	DSP_DDR3_ED38	12-D3	
			DOROS8N	E8	DSP_DDR3_ED39	12-D3	
			DOROS8N	A7	DSP_DDR3_ED40	12-D3	
			DOROS8N	D7	DSP_DDR3_ED41	12-D3	
			DOROS8N	E7	DSP_DDR3_ED42	12-D3	
			DOROS8N	C7	DSP_DDR3_ED43	12-D3	
			DOROS8N	B7	DSP_DDR3_ED44	12-D3	
			DOROS8N	E6	DSP_DDR3_ED45	12-D3	
			DOROS8N	D6	DSP_DDR3_ED46	12-D3	
			DOROS8N	C6	DSP_DDR3_ED47	12-D3	
			DOROS8N	A6	DSP_DDR3_ED48	12-D3	
			DOROS8N	A5	DSP_DDR3_ED49	12-D3	
			DOROS8N	B4	DSP_DDR3_ED50	12-D3	
			DOROS8N	A4	DSP_DDR3_ED51	12-D3	
			DOROS8N	D4	DSP_DDR3_ED52	12-D3	
			DOROS8N	E4	DSP_DDR3_ED53	12-D3	
			DOROS8N	C4	DSP_DDR3_ED54	12-D3	
			DOROS8N	F4	DSP_DDR3_ED55	12-D3	
			DOROS8N	C3	DSP_DDR3_ED56	12-D3	
			DOROS8N	D2	DSP_DDR3_ED57	12-D3	
			DOROS8N	E2	DSP_DDR3_ED58	12-D3	
			DOROS8N	C2	DSP_DDR3_ED59	12-D3	
			DOROS8N	F2	DSP_DDR3_ED60	12-D3	
			DOROS8N	F3	DSP_DDR3_ED61	12-D3	
			DOROS8N	E1	DSP_DDR3_ED62	12-D3	
			DOROS8N	D1	DSP_DDR3_ED63	12-D3	

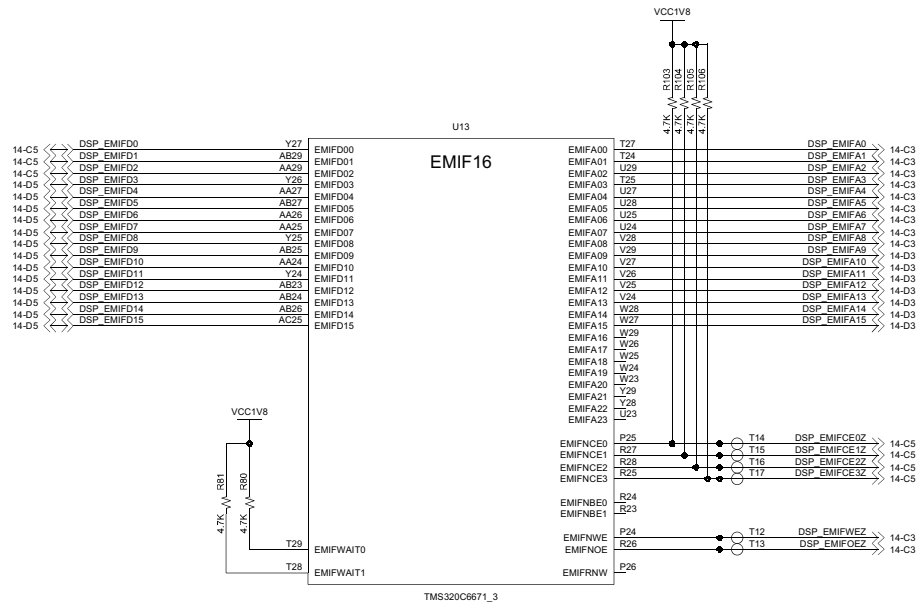
### DDR3 CONTROLLER

U13

TMS320C6671\_2

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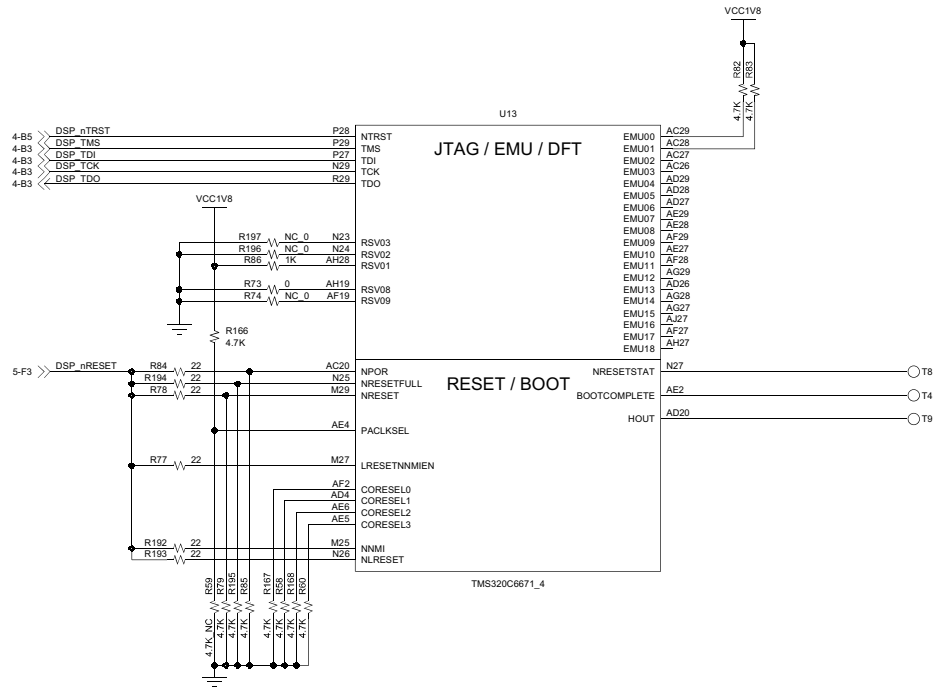
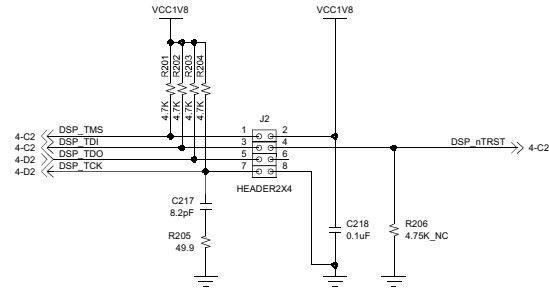
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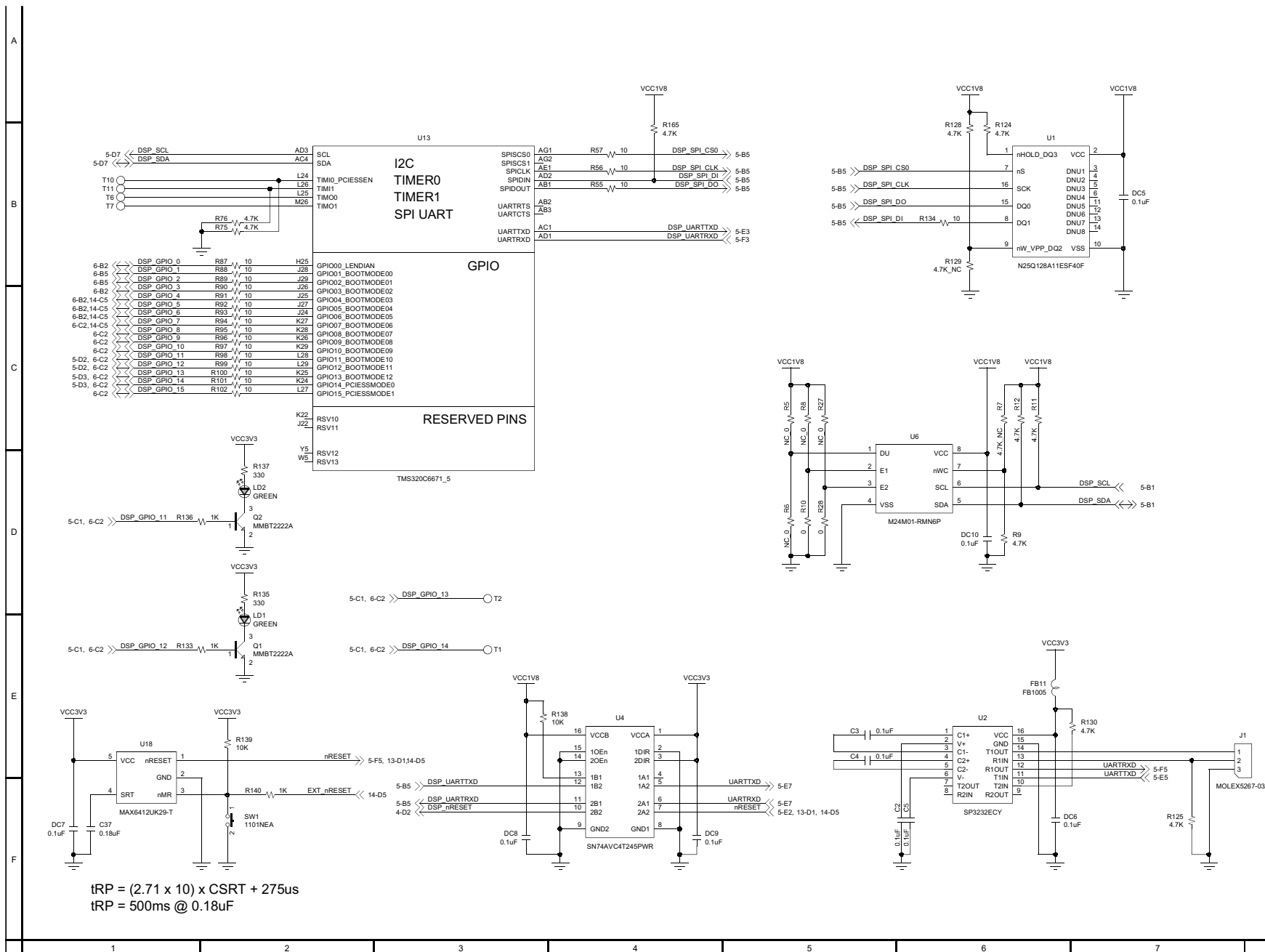
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$t_{RP} = (2.71 \times 10) \times CSRT + 275us$   
 $t_{RP} = 500ms @ 0.18\mu F$

A

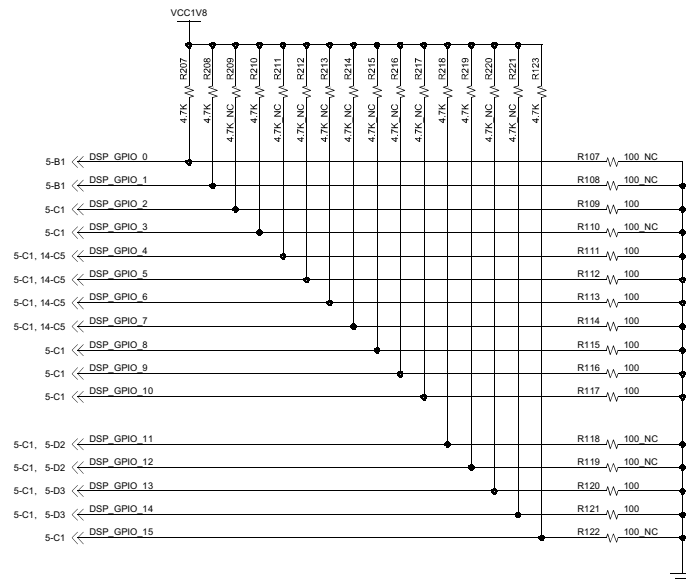
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### Boot Configuration

DSP	Boot Mode	Primary Function	
		Pull Up	Pull Down
GPIO0	LENDIAN	Little Endian	Big Endian
GPIO1	BOOTMODE00	Boot Device	
GPIO2	BOOTMODE01	Boot Device	
GPIO3	BOOTMODE02	Boot Device	
GPIO4	BOOTMODE03	Device Cfg	
GPIO5	BOOTMODE04	Device Cfg	
GPIO6	BOOTMODE05	Device Cfg	
GPIO7	BOOTMODE06	Device Cfg	
GPIO8	BOOTMODE07	Device Cfg	
GPIO9	BOOTMODE08	Device Cfg	
GPIO10	BOOTMODE09	Device Cfg	
GPIO11	BOOTMODE10	PLL Multiplier / I2C	
GPIO12	BOOTMODE11	PLL Multiplier / I2C	
GPIO13	BOOTMODE12	PLL Multiplier / I2C	
GPIO14	PCIESSMODE0	Endpt / RootComplex	
GPIO15	PCIESSMODE1	Endpt / RootComplex	

### Boot Device

GPIO	BOOT Device	NOTE
3 2 1	EMIF16	
0 0 0	sRIO	
0 1 0	SMGII	PA driven from core clk
0 1 1	SGMII	PA driven from PA clk
1 0 0	PCle	
1 0 1	I2C	
1 1 0	SPI	
1 1 1	HyperLink	

### Device Configuration

GPIO	Device Configuration Field	The device configuration fields GPIO[10:4] are used to configure the boot peripheral and, therefore, the bit definitions depend on the boot mode.
[10:4]		

### PLL Settings

GPIO	INPUT CLK (MHz)	CorePac System PLL Configuration
13 12 11	50.00	
0 0 0	66.67	
0 0 1	80.00	PA driven from core clk
0 1 0	100.00	PA driven from PA clk
1 0 0	156.25	
1 0 1	250.00	
1 1 0	312.50	
1 1 1	122.88	

### PCle Mode selection(PCIESSMODE[1:0])

GPIO[15:14] INPUT	Description
00b	PCle in End-point mode
01b	PCle in Legacy End-point mode (no support for MSI)
10b	PCle in Legacy Root complex mode

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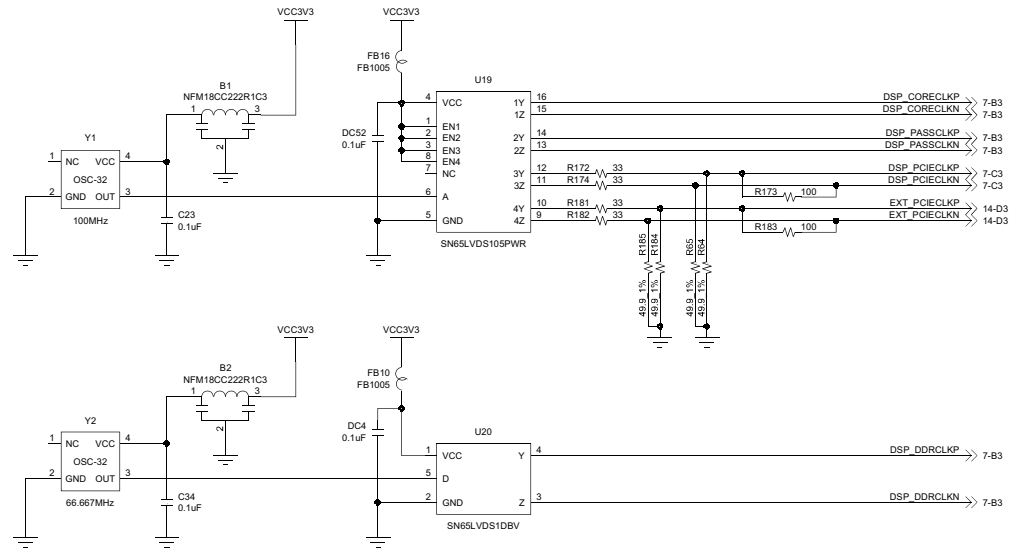
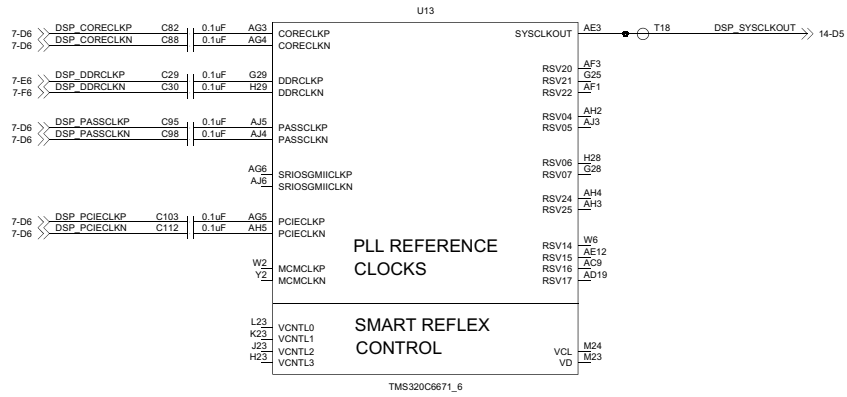
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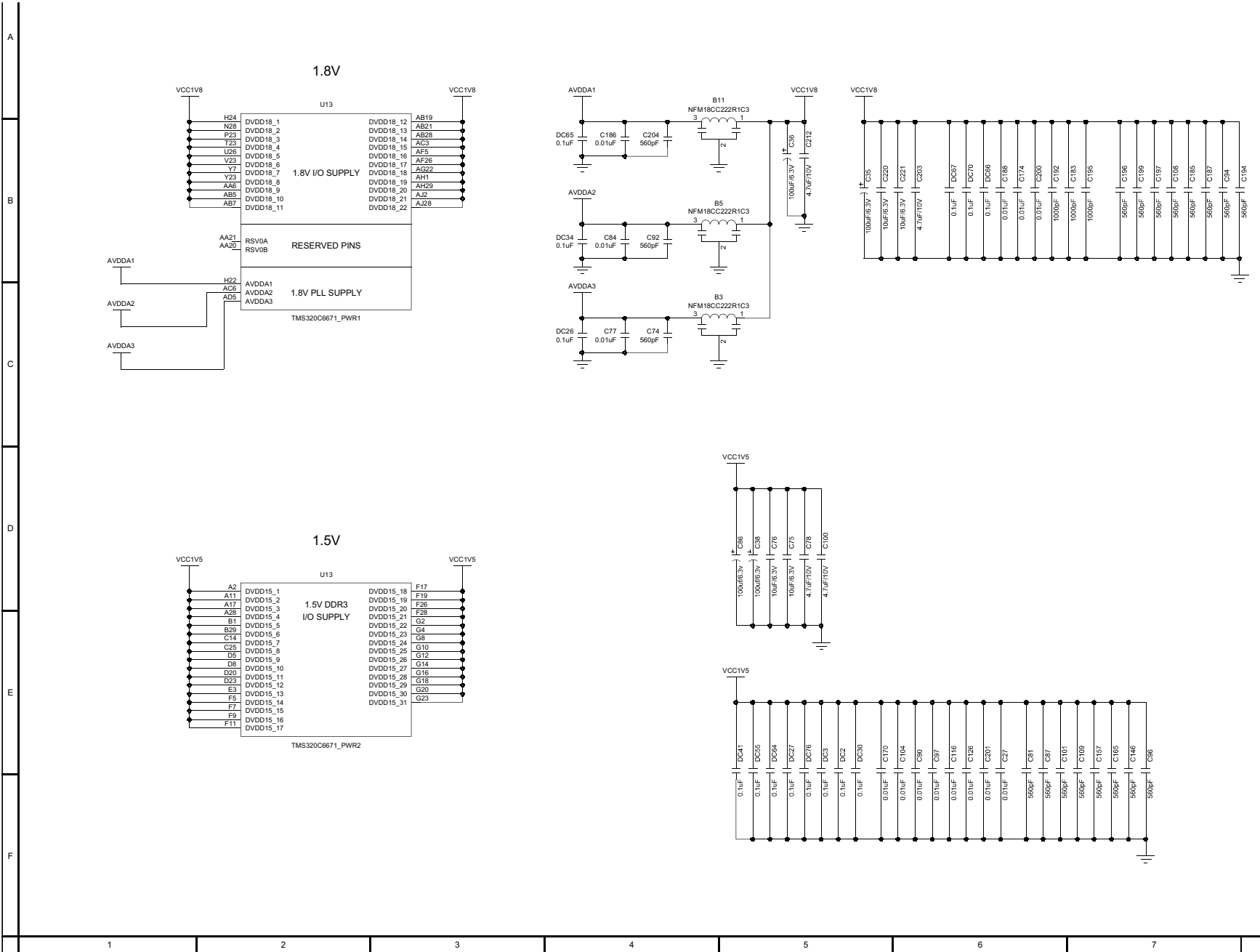
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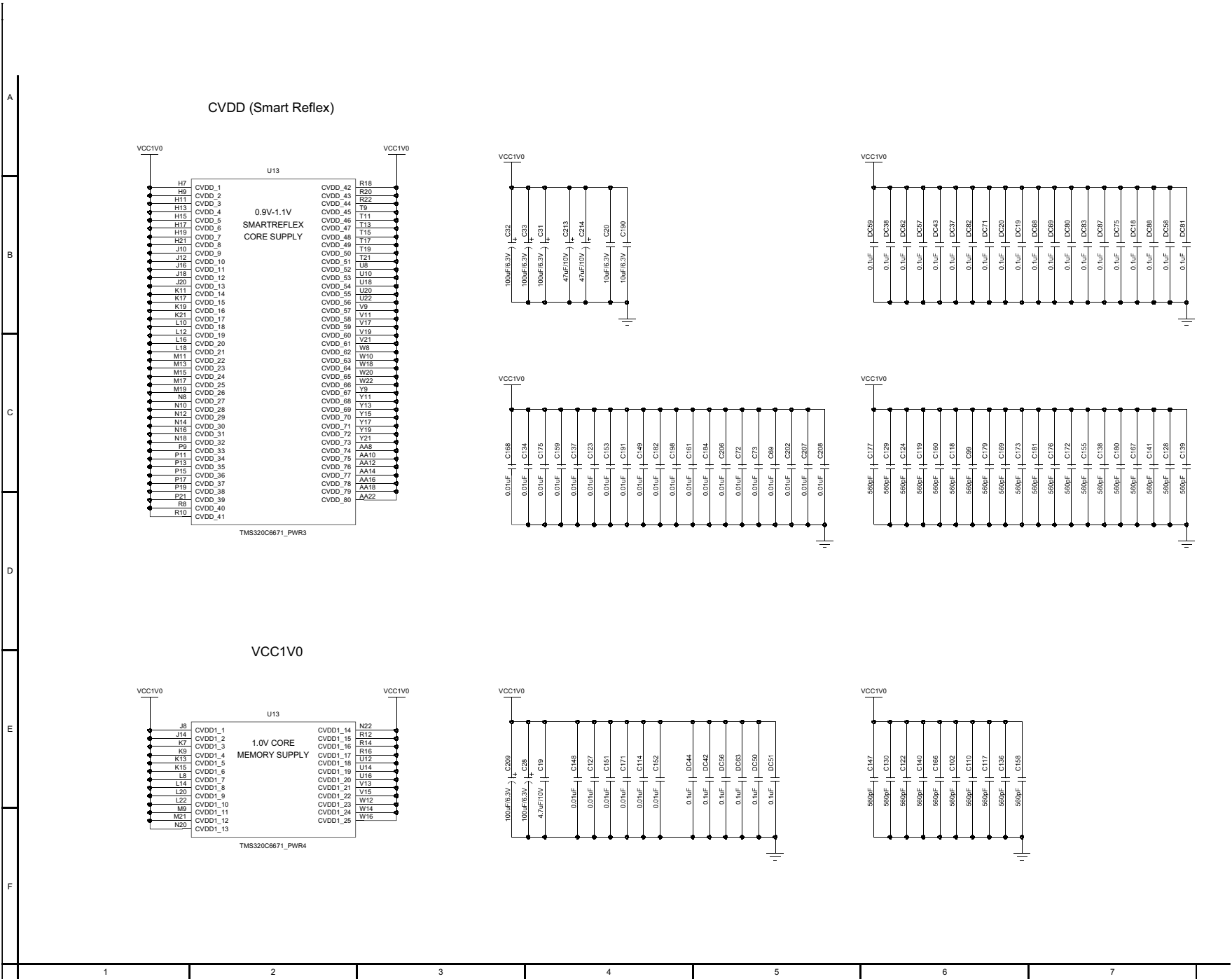
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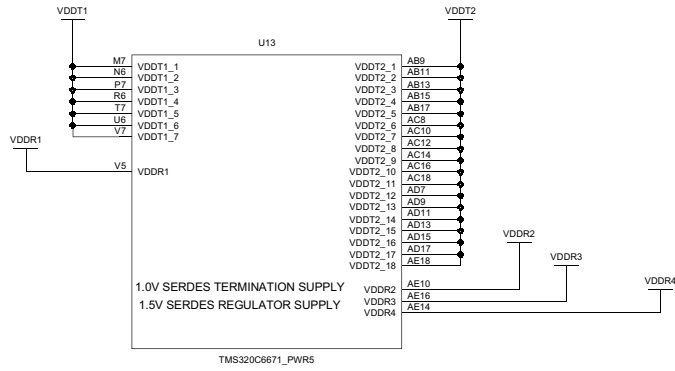
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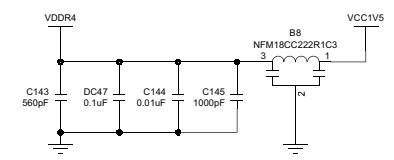
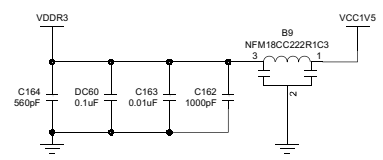
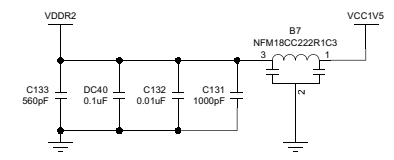
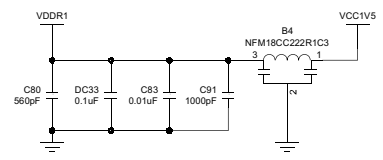
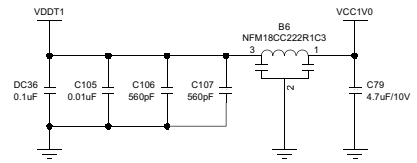
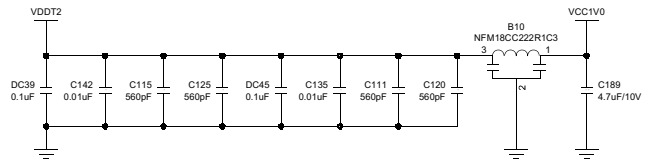


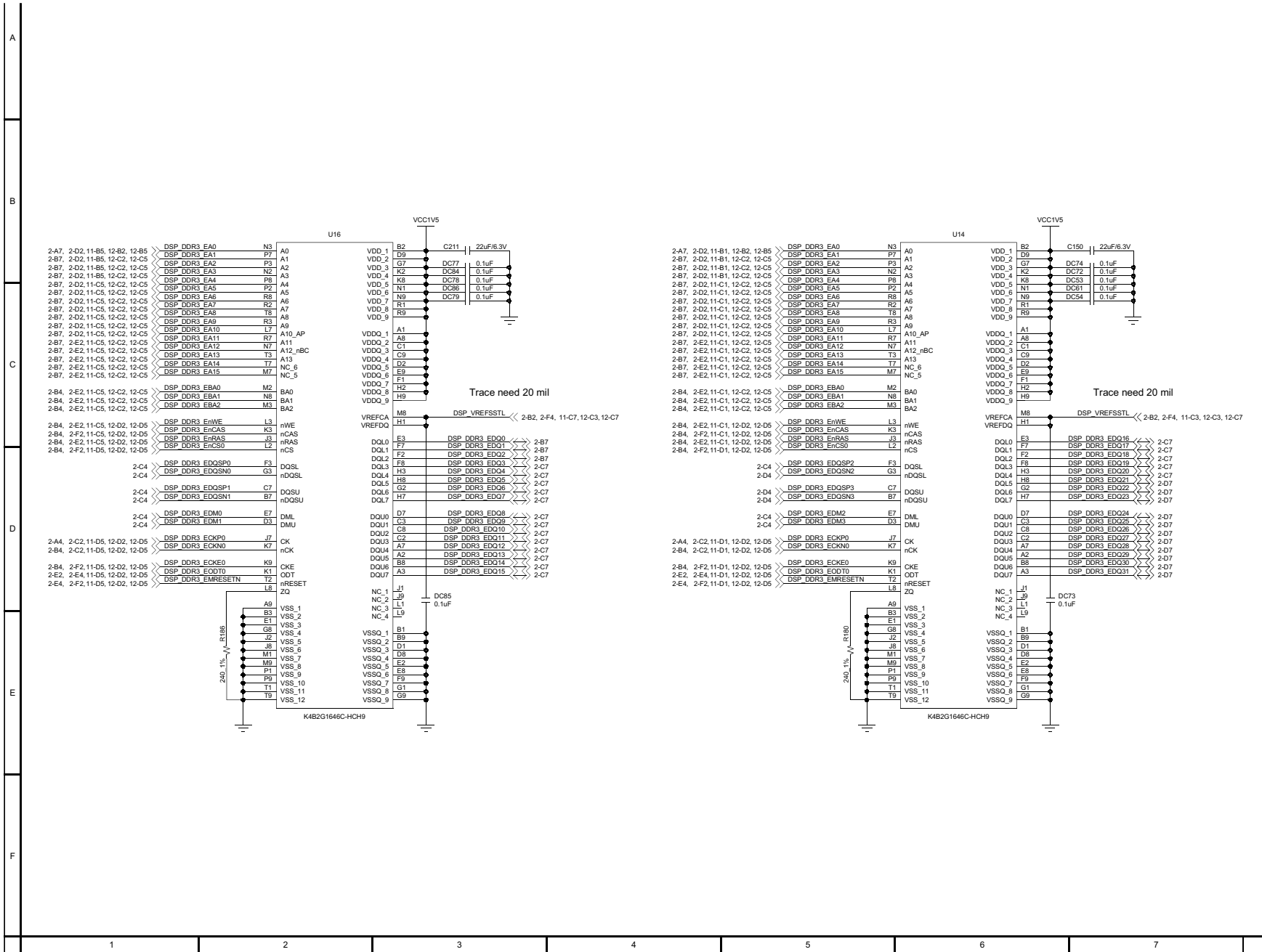
### 1.0V & 1.5V for Serdes



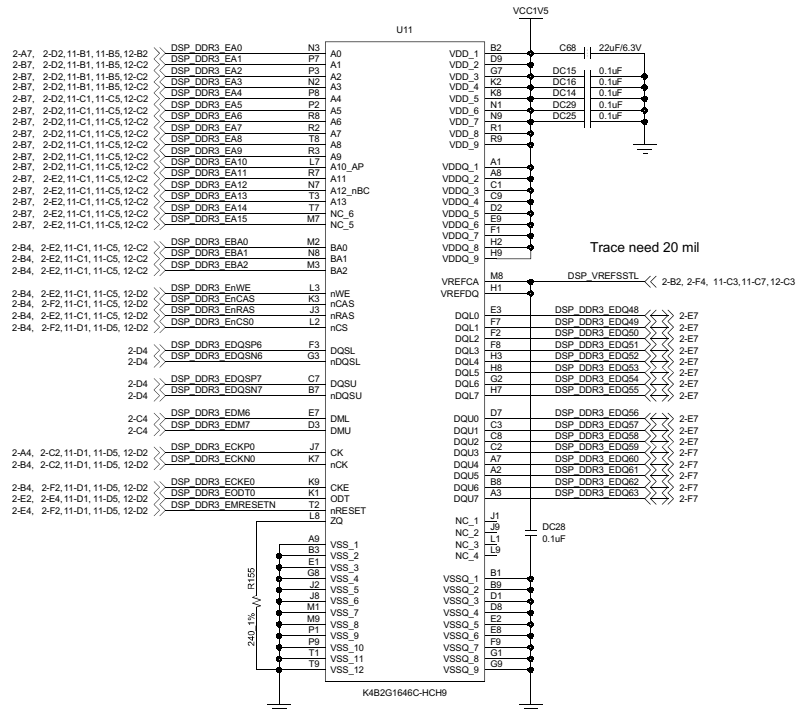
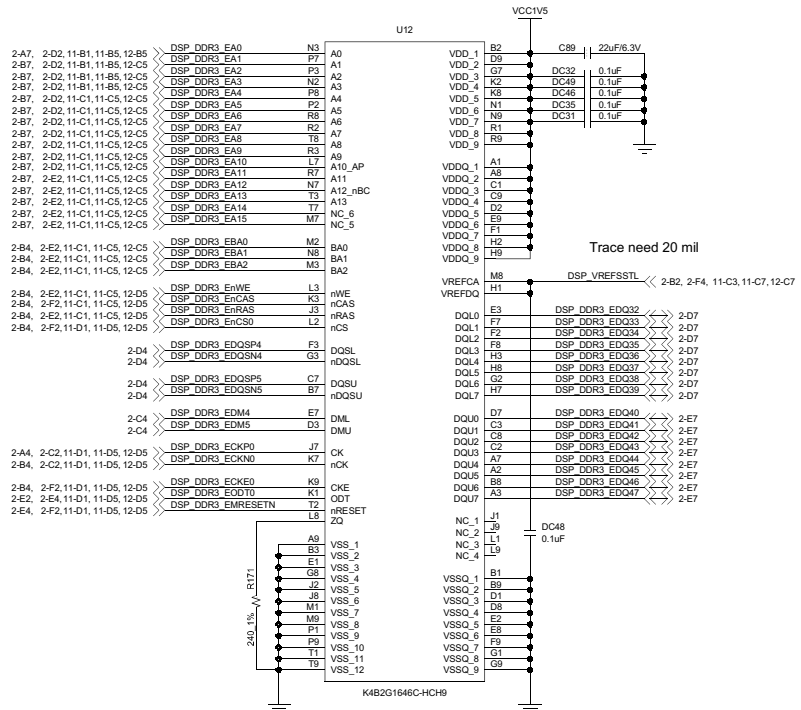
U13  
TMS320C6671\_GND

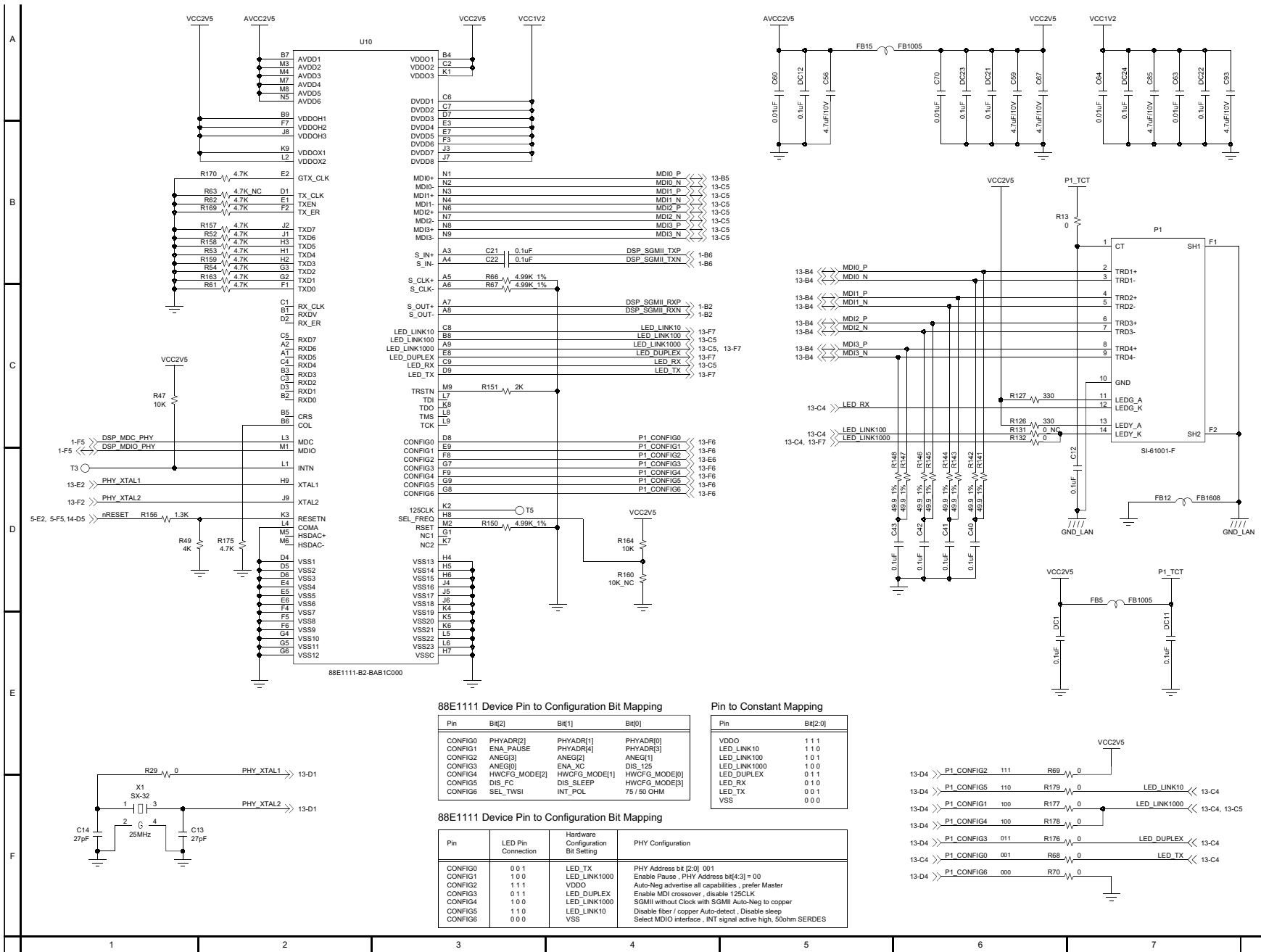
A1	VSS_1		VSS_168	W7
A25	VSS_2		VSS_169	W9
B11	VSS_3		VSS_170	W11
B17	VSS_4	L19	VSS_171	W13
B25	VSS_5	L21	VSS_172	W15
C3	VSS_6	M2	VSS_173	W17
C23	VSS_7	M3	VSS_174	W19
D3	VSS_8	M4	VSS_175	W21
D14	VSS_9	M6	VSS_176	Y5
D18	VSS_10	M8	VSS_177	Y7
E5	VSS_11	M10	VSS_178	Y9
E20	VSS_12	M12	VSS_179	Y11
F6	VSS_13	M14	VSS_180	Y13
F8	VSS_14	M16	VSS_181	Y15
F10	VSS_15	M18	VSS_182	Y17
F12	VSS_16	M20	VSS_183	Y19
F16	VSS_17	M22	VSS_184	Y21
F18	VSS_18	M28	VSS_185	Y23
G1	VSS_19	N3	VSS_186	AA5
G11	VSS_20	N7	VSS_187	AA7
G13	VSS_21	N9	VSS_188	AA9
G3	VSS_22	N11	VSS_189	AA11
G6	VSS_23	N13	VSS_190	AA13
G7	VSS_24	N15	VSS_191	AA15
G9	VSS_25	N17	VSS_192	AA17
G11	VSS_26	N19	VSS_193	AA19
G13	VSS_27	N21	VSS_194	AA21
G15	VSS_28	P1	VSS_195	AA23
G17	VSS_29	P3	VSS_196	AA25
G19	VSS_30	P5	VSS_197	AA27
G21	VSS_31	P7	VSS_198	AA29
H1	VSS_32	P9	VSS_199	AA31
H2	VSS_33	P11	VSS_200	AA33
H3	VSS_34	P13	VSS_201	AA35
H4	VSS_35	P15	VSS_202	AA37
H5	VSS_36	P17	VSS_203	AA39
H6	VSS_37	P19	VSS_204	AA41
H7	VSS_38	P21	VSS_205	AA43
H8	VSS_39	P23	VSS_206	AA45
H9	VSS_40	R2	VSS_207	AA47
H10	VSS_41	R3	VSS_208	AA49
H12	VSS_42	R4	VSS_209	AA51
H14	VSS_43	R7	VSS_210	AA53
H16	VSS_44	R9	VSS_211	AA55
H18	VSS_45	R11	VSS_212	AA57
H20	VSS_46	R13	VSS_213	AA59
J1	VSS_47	R15	VSS_214	AA61
J2	VSS_48	R17	VSS_215	AA63
J3	VSS_49	R19	VSS_216	AA65
J4	VSS_50	R21	VSS_217	AA67
J5	VSS_51	T3	VSS_218	AA69
J6	VSS_52	T6	VSS_219	AA71
J7	VSS_53	T8	VSS_220	AA73
J8	VSS_54	T10	VSS_221	AA75
J9	VSS_55	T12	VSS_222	AA77
J11	VSS_56	T14	VSS_223	AA79
J13	VSS_57	T16	VSS_224	AA81
J15	VSS_58	T18	VSS_225	AA83
J17	VSS_59	T20	VSS_226	AA85
J19	VSS_60	T22	VSS_227	AA87
J21	VSS_61	T26	VSS_228	AA89
K1	VSS_62	U1	VSS_229	AA91
K2	VSS_63	U3	VSS_230	AA93
K3	VSS_64	U5	VSS_231	AA95
K4	VSS_65	U7	VSS_232	AA97
K5	VSS_66	U9	VSS_233	AA99
K6	VSS_67	U11	VSS_234	AA101
K7	VSS_68	U13	VSS_235	AA103
K8	VSS_69	U15	VSS_236	AA105
K9	VSS_70	U17	VSS_237	AA107
K10	VSS_71	U19	VSS_238	AA109
K11	VSS_72	U21	VSS_239	AA111
K12	VSS_73	V1	VSS_240	AA113
K13	VSS_74	V2	VSS_241	AA115
K14	VSS_75	V3	VSS_242	AA117
K15	VSS_76	V4	VSS_243	AA119
K16	VSS_77	V6	VSS_244	AA121
K17	VSS_78	V8	VSS_245	AA123
K18	VSS_79	V10	VSS_246	AA125
L1	VSS_80	V12	VSS_247	AA127
L2	VSS_81	V14	VSS_248	AA129
L3	VSS_82	V16	VSS_249	AA131
L4	VSS_83	V18	VSS_250	AA133
L5	VSS_84	V20	VSS_251	AA135
L6	VSS_85	V22	VSS_252	AA137





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88E1111 Device Pin to Configuration Bit Mapping

Pin	B#(2)	B#(1)	B#(0)
CONFIG0	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG2	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG3	ANEG[0]	ENA_XC	DIS_125
CONFIG4	HWCFG_MODE[2]	HWCFG_MODE[1]	HWCFG_MODE[0]
CONFIG5	DIS_FC	DIS_SLEEP	HWCFG_MODE[3]
CONFIG6	SEL_TWSI	INT_POL	75 / 50 Ohm

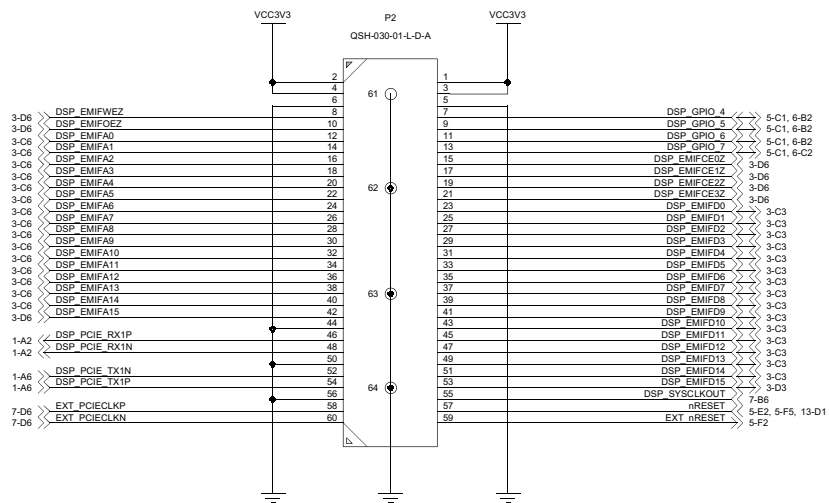
Pin to Constant Mapping

Pin	B#(2:0)
VDD0	1 1 1
LED_LINK10	1 1 0
LED_LINK100	1 0 1
LED_LINK1000	1 0 0
LED_DUPLEX	0 1 1
LED_RX	0 1 0
LED_TX	0 0 1
VSS	0 0 0

88E1111 Device Pin to Configuration Bit Mapping

Pin	LED Pin Connection	Hardware Configuration Bit Setting	PHY Configuration
CONFIG0	0 0 1	LED_TX	PHY Address bit [2:0] 001
CONFIG1	1 0 0	LED_LINK1000	Enable Pause , PHY Address bit[4:3] = 00
CONFIG2	1 1 1	VDD0	Auto-Neg advertise all capabilities , prefer Master
CONFIG3	0 1 1	LED_DUPLEX	Enable MDI crossover , disable 125CLK
CONFIG4	1 0 0	LED_LINK1000	SGMII without Clock with SGMII Auto-Neg to copper
CONFIG5	1 1 0	LED_LINK10	Disable fiber / copper Auto-detect , Disable sleep
CONFIG6	0 0 0	VSS	Select MDIO interface , INT signal active high, 50ohm SERDES

A  
B  
C  
D  
E  
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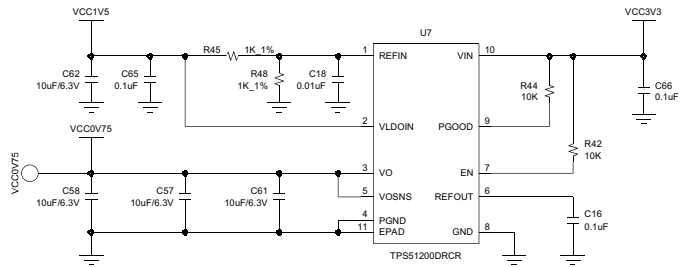
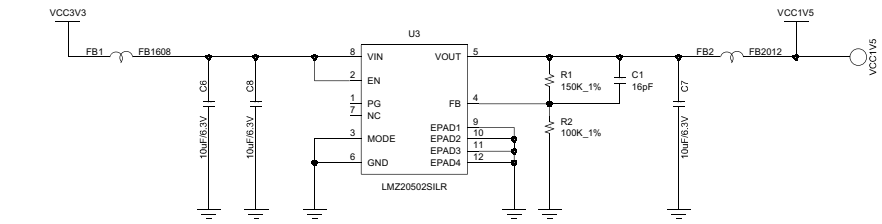
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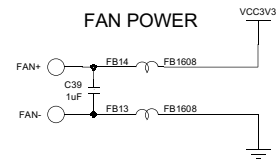
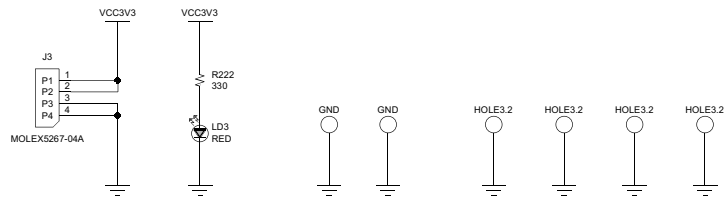
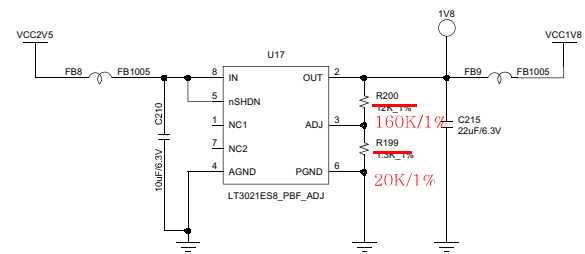
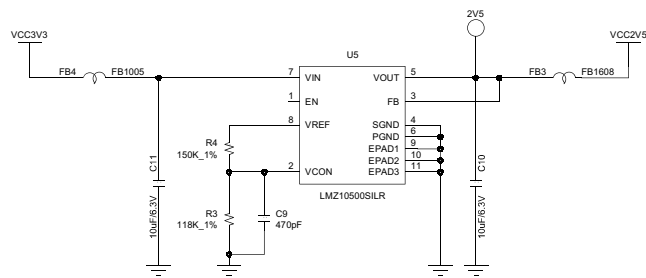
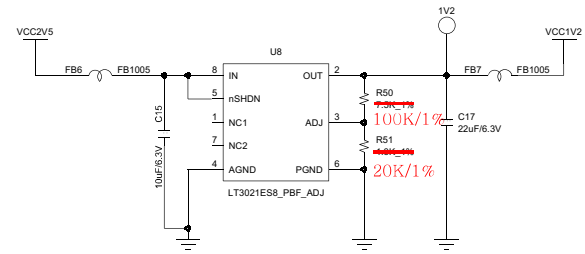
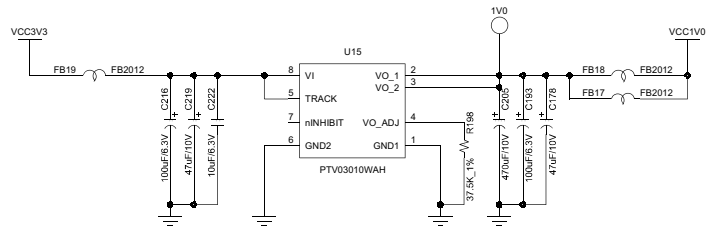
B

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