REV	DESCRIPTION	DATE	BY
A0	Production Release	23/12/2019	FEDD

P01 TITLE PAGE
P02 12V INPUT, 3.3V ~~AND 5V SWITCHERS~~
P03 TPS6590374 1 CONTROL
P04 TPS6590374 2 RESET, & RTC
P05 TPS6590374 3 MPU,DDR, & DSP SWITCHERS
P06 TPS6590374 4 CORE & 1.8V
P07 AM5728 CORE POWER & EEPROM
P08 AM5728 CLOCKS AND RESET
P09 AM5728 IO POWER AND GROUND
P10 AM5728 DDR3 POWER & JTAG
P11 AM5728 ETHERNET 1
P12 AM5728 ETHERNET 2
P13 AM5728 GPMC & LCD
P14 ~~AM5728 USB INTERFACES~~
P15 AM5728 I/O, LEDs, AND GPIO
P16 ~~AM5728 AUDIO &~~ DEBUG SERIAL
P17 ~~AM5728 HDMI PORT~~
P18 AM5728 eMMC, MMC3, & uSD
P19 AM5728 DDR INTERFACE 1
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P21 DDR3 BANK 1
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P23 DDR3 BANK 2 CAPS & TERM
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P25 ~~USB & SATA CONNECTOR~~
P26 PCIe, ~~SATA,~~ & SERDES CLOCK
P27 EXPANSION HEADERS
P28 MECHANICAL

This schematic is *NOT SUPPORTED* and DOES NOT constitute a reference design. Only “community” support is allowed via resources at BeagleBoard.org/discuss.

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Title	E6303A0	
Size B	Document Number	Rev A0
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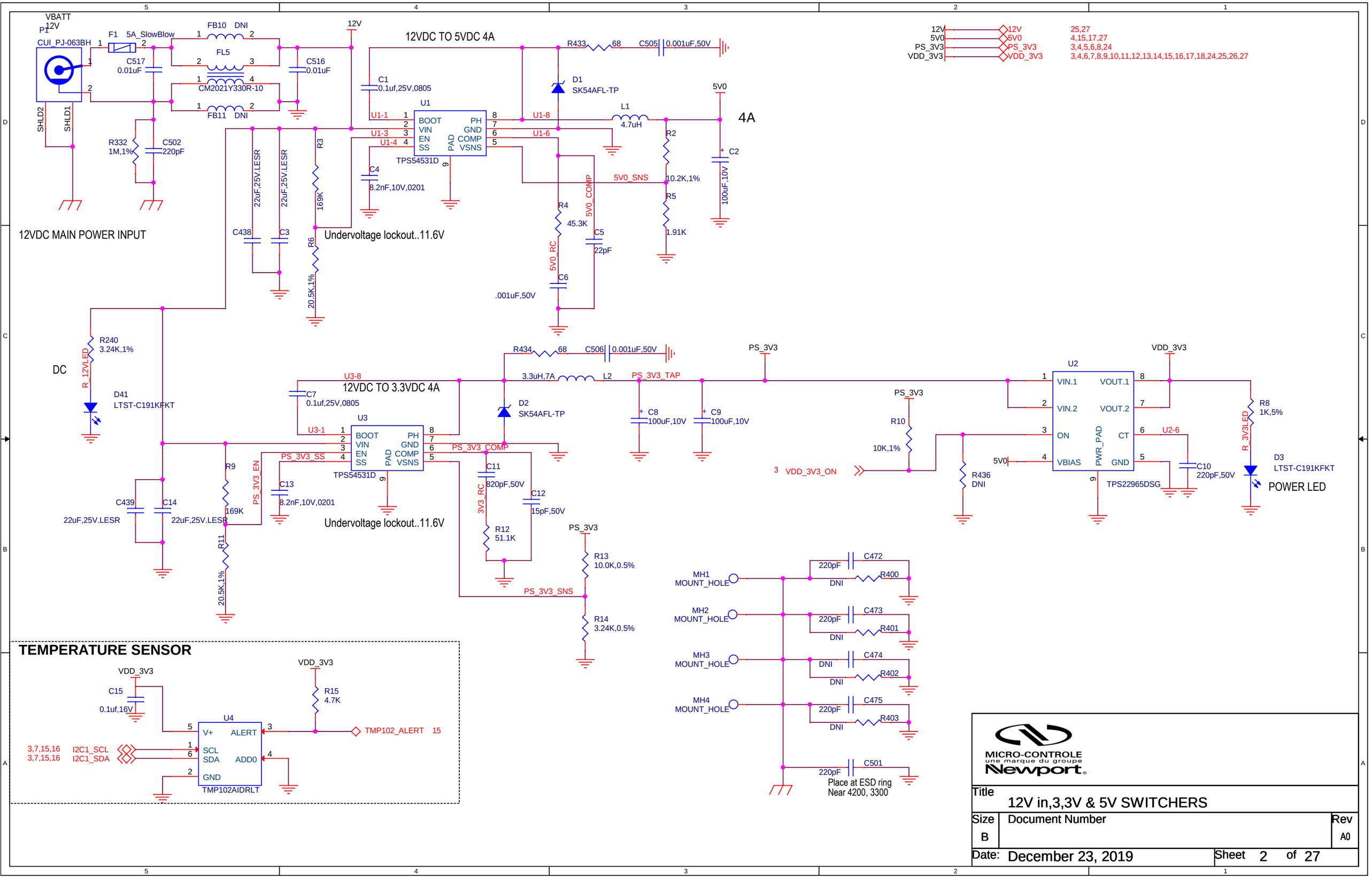
12VDC TO 5VDC 4A
12VDC MAIN POWER INPUT
Undervoltage lockout..11.6V
12VDC TO 3.3VDC 4A
Undervoltage lockout..11.6V
TEMPERATURE SENSOR
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Title
12V in,3,3V & 5V SWITCHERS
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Y9 OPTIONAL PACKAGE
CHANGE C452 & C453
VALUE AS NEEDED

PMIC

U5B

TPS6590376ZWSR

8,16,18,26,27 RSTOUTn — R318 1.74K — R319 2K

VDD_3V3 — R16 2.2K,1% — R17 2.2K,1%

C452 12pF/0402/50V — Y9 16.384MHz — C453 12pF/0402/50V

PMIC_XTAL_IN A3 OSC16MIN

PMIC_XTAL_OUT A2 OSC16MOUT

C16 0.1uf,16V — VBG B7 VBG

CLK32KGO M11

OSC16MCAP C1 — C496 2.2uF,6.3V

8 PMIC_RESET_IN

2,7,15,16 I2C1_SDA — L2 I2C1_SDA_SDI VIO_IN

2,7,15,16 I2C1_SCL — L1 I2C1_SCL_SCK VIO_IN

LDO_VRTC — R453 10K,1%

R18 2.2K,1% PMIC_SDO — H8 I2C2_SDA_SDO VIO_IN

R19 2.2K,1% PMIC_SCE — M3 I2C2_SCL_SCE VIO_IN

8 PMIC_OFF — R322 1.74K,DNI — R323 2K,DNI — E5 NSLEEP VRTC

PS_3V3 — R407 10K,1% — E6 NRESWARM VRTC

K9 RESET_IN VRTC-5.25VT

BOOT0=0=1.35V DDR
BOOT1=1=WarmReset PORz Pulse

S1 — SW PUSH TH — G8 PWRON

C216 47pF PB_ESD — POWER BUTTON — C478 0.1uf,16V

C11 RPWRON

PMIC_BOOT0 — L3 BOOT0 VRTC

PMIC_BOOT1 — K7 BOOT1 VRTC

VRTC POWERGOOD — J7 PMIC_POWERGOOD

VIO_IN INT — K1 PMIC_INT 8

VCC1 REGEN1 — F8 VDD_3V3_ON 2

RESET_OUT — G6 PMIC_RESET_OUT 8

LDO_VRTC — R23 10K,1%,DNI — R20 10K,DNI — R21 10K,1% — R22 10K,1% — R214 10K,1%,DNI

TPS_ENABLE1 — J5 ENABLE1

TPS_PWRDOWN — K8 PWRDOWN VRTC-5.25VT

27 PWRON

VPROG/TESTV — N12 TESTV

13 VBUS_DET

PMIC_GPIO_0 — B12 GPIO_0 VRTC-5.25VT

C13 GPIO_1/VBUSDET VCC1

A12 GPIO_2/REGEN2 VCC1

PMIC_GPIO_3 — H9 GPIO_3 VRTC-5.25VT

PMIC_GPIO_5 — K10 GPIO_4/SYSEN1 VIO_IN

C10 GPIO_5/CLK32KGO VRTC-3.6VT

PMIC_POWERHOLD — N11 GPIO_6/SYSEN2 VIO_IN

G9 GPIO_7/POWERHOLD VRTC-5.25VT

GPADC_REF B4

GPADC_IN0 B2

GPADC_IN1 C2

GPADC_IN2 C3

R26 10K,1% — R27 10K,1% — R28 10K,1%

PS_3V3 — R29 0,1% VCC_SENSE2 — A11 VCC_SENSE2

R30 0,1% VCC_SENSE — B3 VCC_SENSE

14 USB2_VBUS — D8 VBUS

E7 VAC/ACOK

GNDANA A7 — AGND.1 F5 — AGND.2 M13 — REFGND1 A4 — GND_DIG M12

J5 — HDR_1x1_M_.1, DNI — LDO_VRTC

R421 10K,1%

R411 10K,1%, DNI

Insert wire here to enable use of the JTAG without boot image present. Otherwise board will power off.

VDD_3V3 — VDD_3V3 2,4,6,7,8,9,10,11,12,13,14,15,16,17,18,24,25,26,27

PS_3V3 — PS_3V3 2,4,5,6,8,24

LDO_VRTC — LDO_VRTC 4,8

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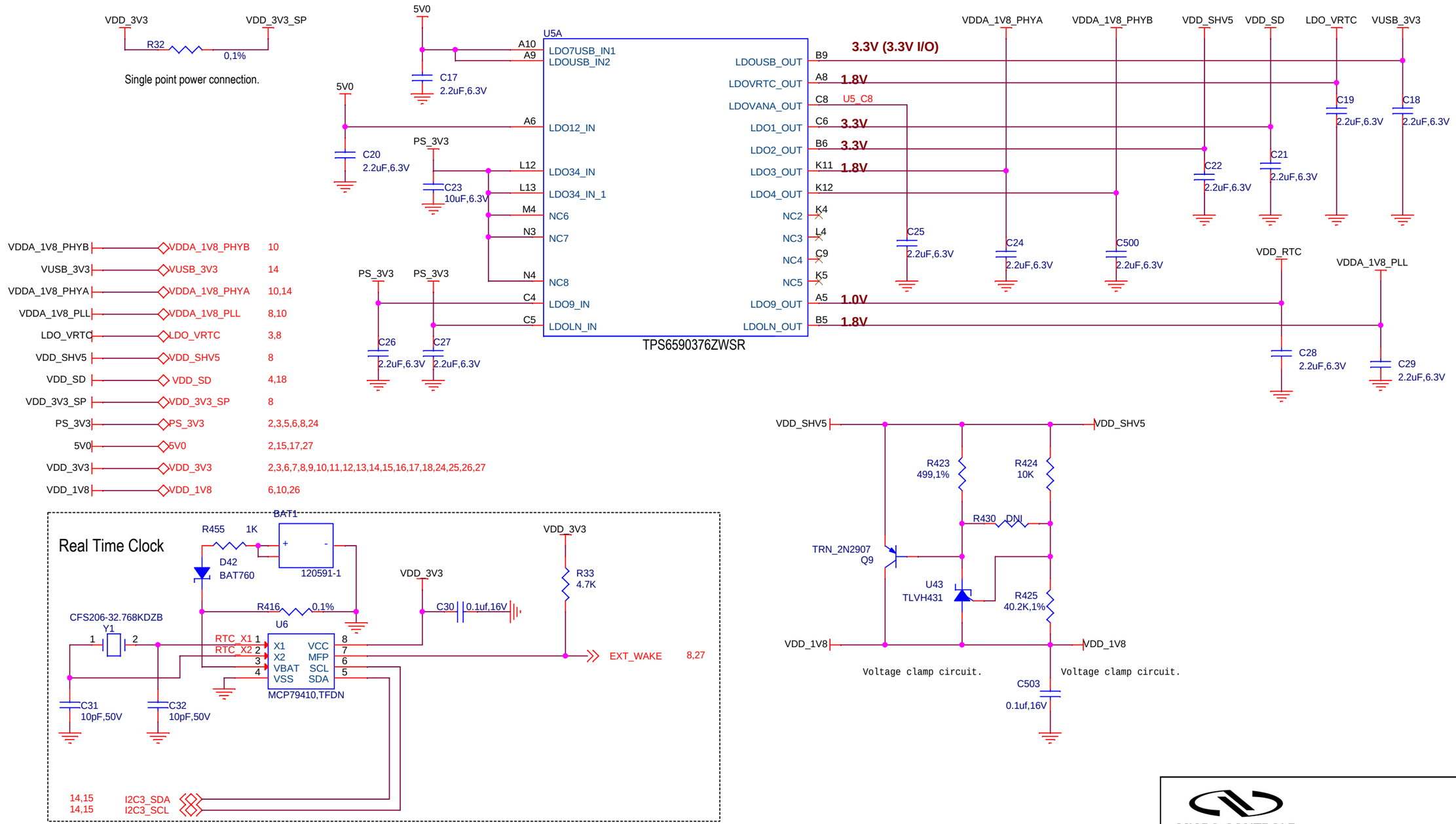
Title	TPS6590371 CONTROL		
Size B	Document Number		Rev A0
Date: December 23, 2019		Sheet 3 of 27	



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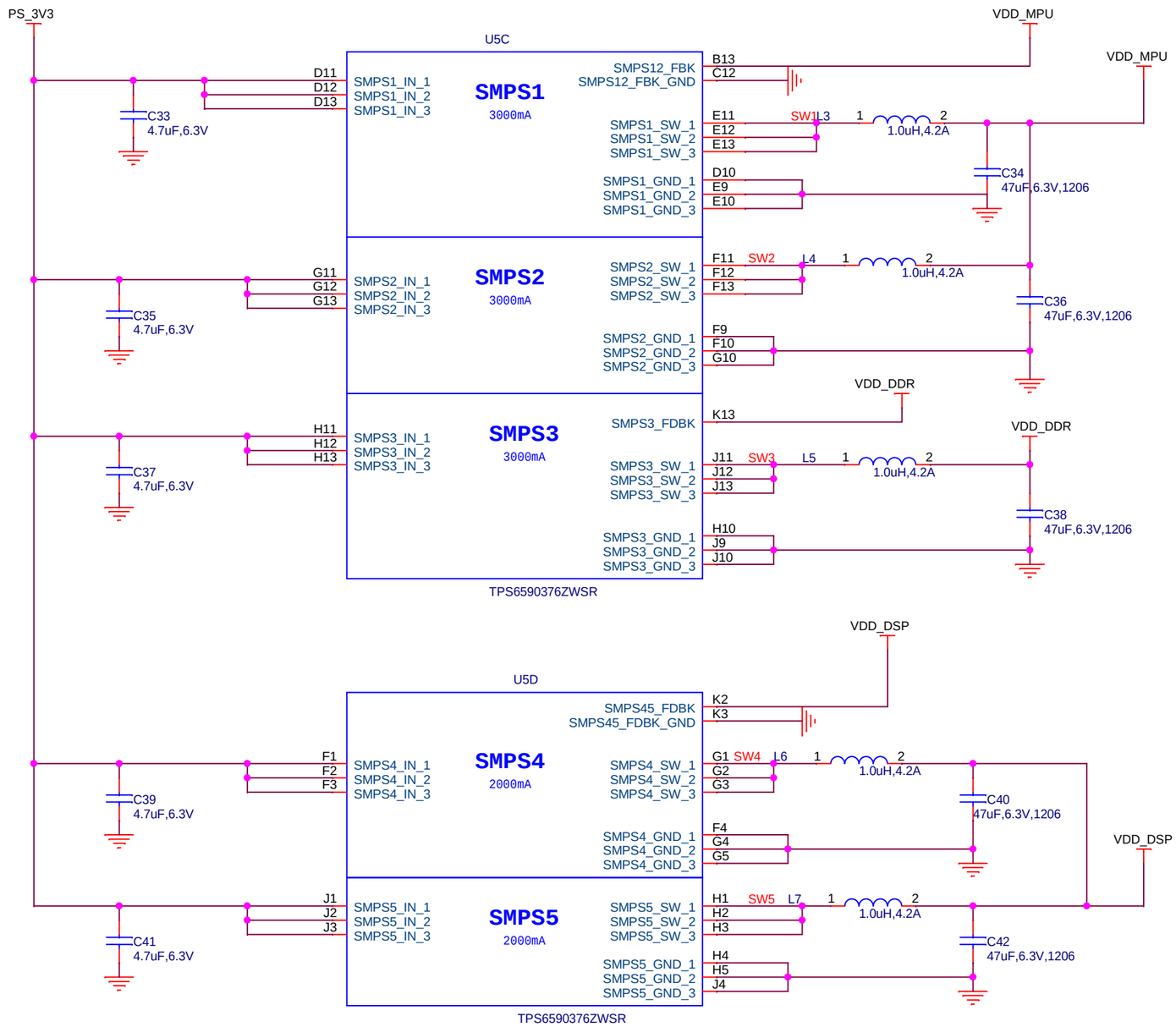
Title	TPS6590371 CONTROL	
Size B	Document Number	Rev A0
Date: December 23, 2019	Sheet 4 of 27	



VDD_MPU	VDD_MPU	7,8
VDD_DDR	VDD_DDR	10,19,21,22,23,24
VDD_DSP	VDD_DSP	7
PS_3V3	PS_3V3	2,3,4,6,8,24

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Title
TPS6590371 MPU, DDR, & DSP

Size	Document Number	Rev
B		A0

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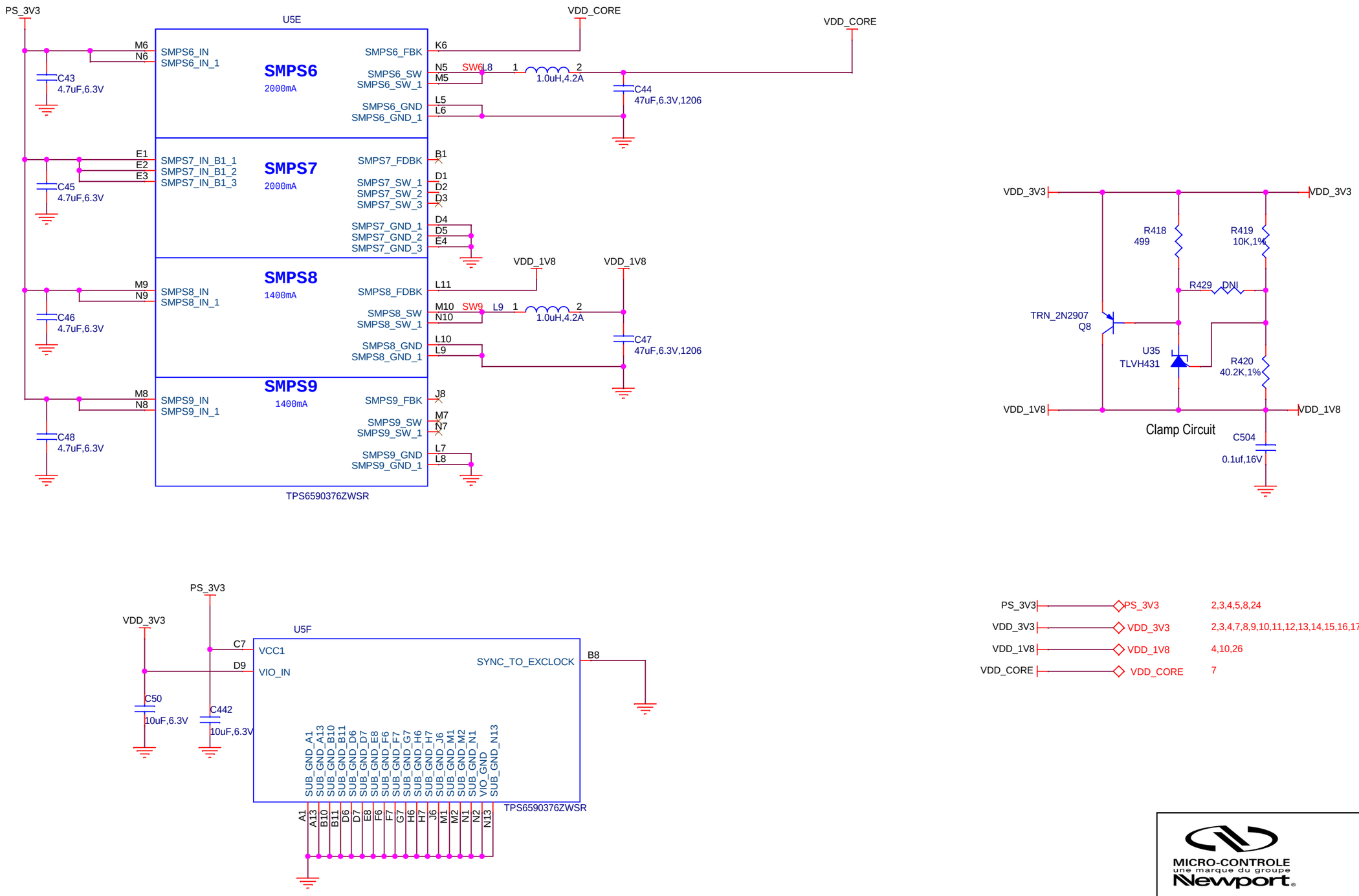

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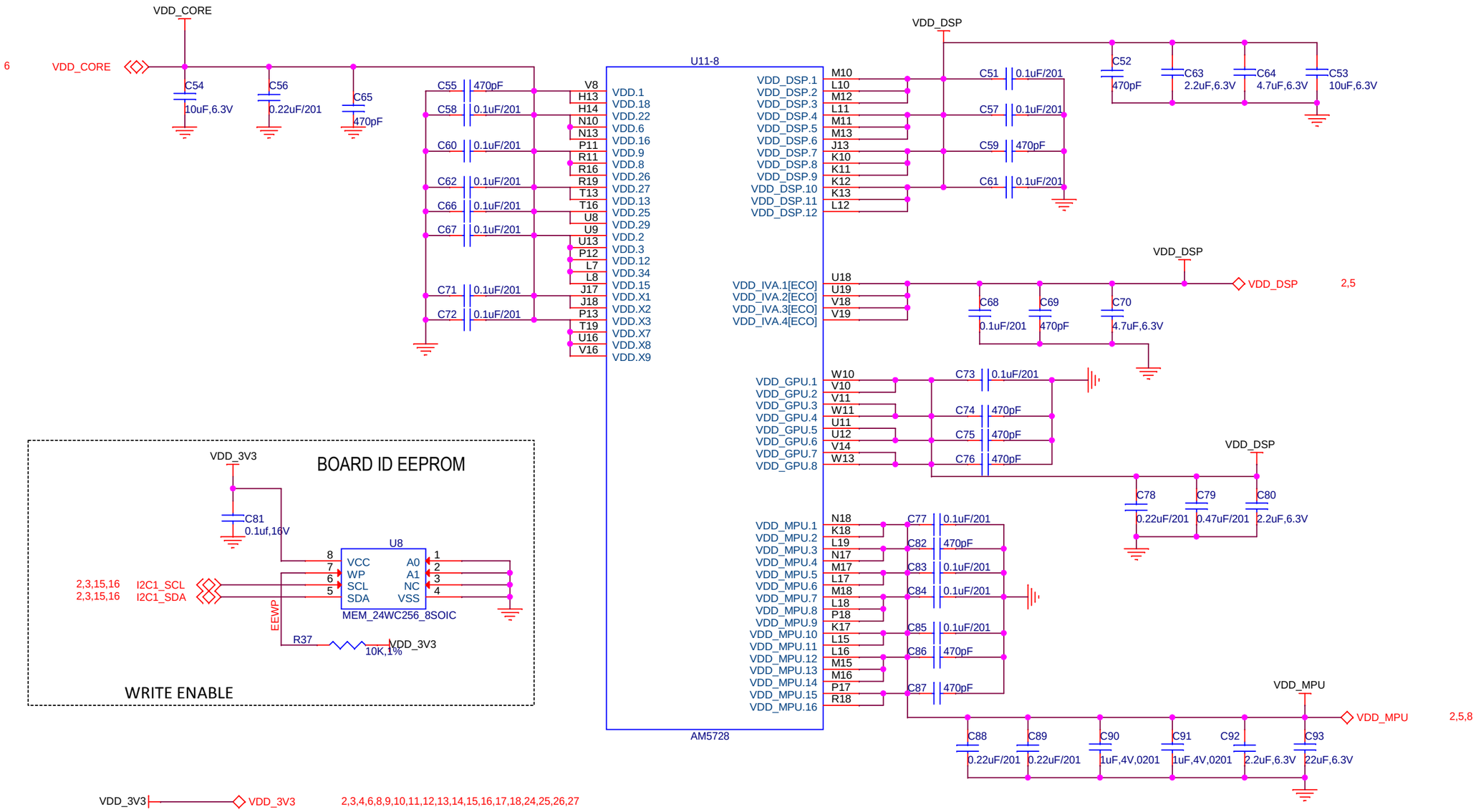
Title	TPS6590374 SWITCHERS	
Size B	Document Number	Rev A0
Date: December 23, 2019	Sheet 6 of 27	



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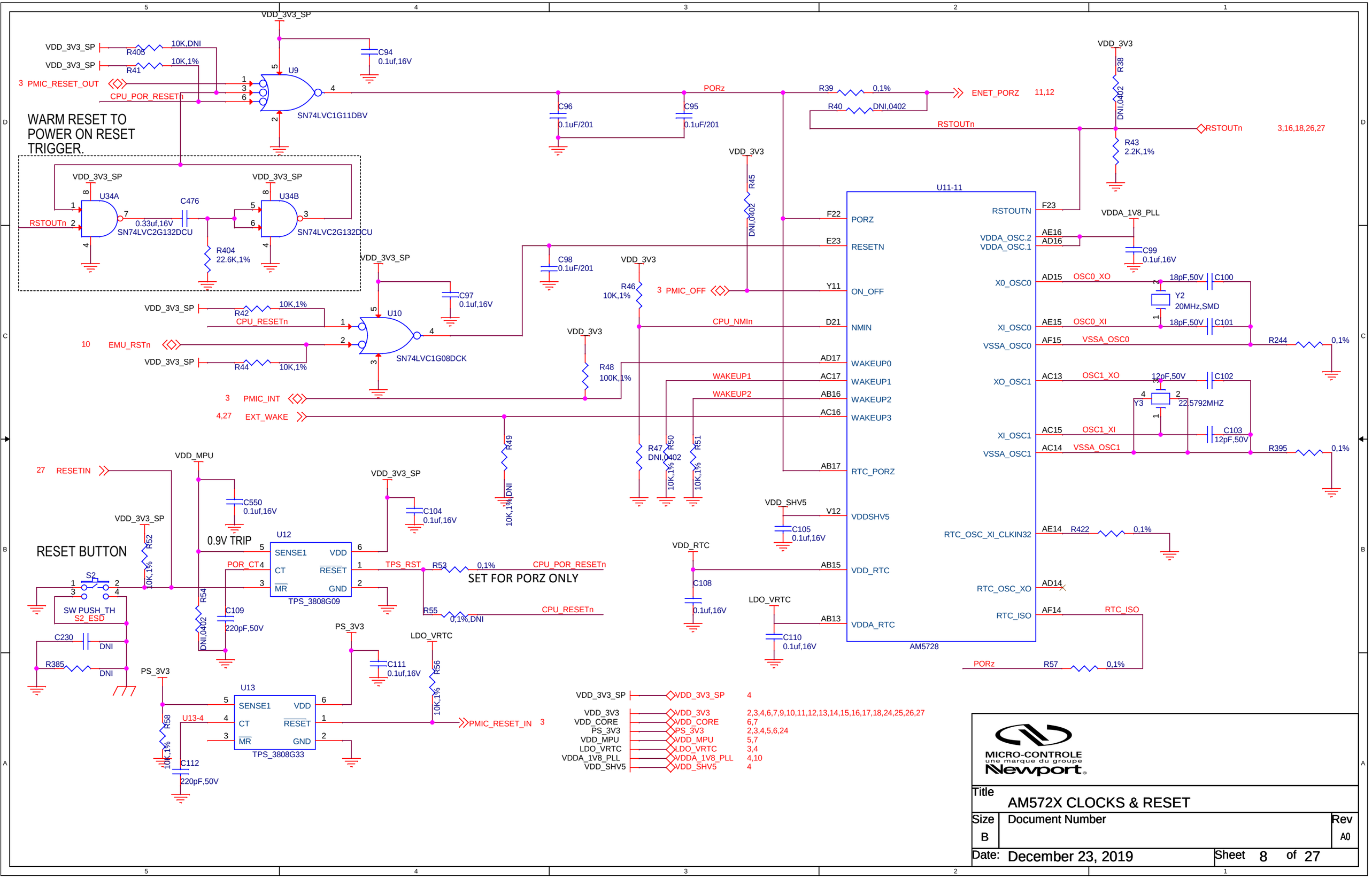
Title	AM5728 CORE POWER	
Size B	Document Number	Rev A0
Date: December 23, 2019	Sheet 7 of 27	



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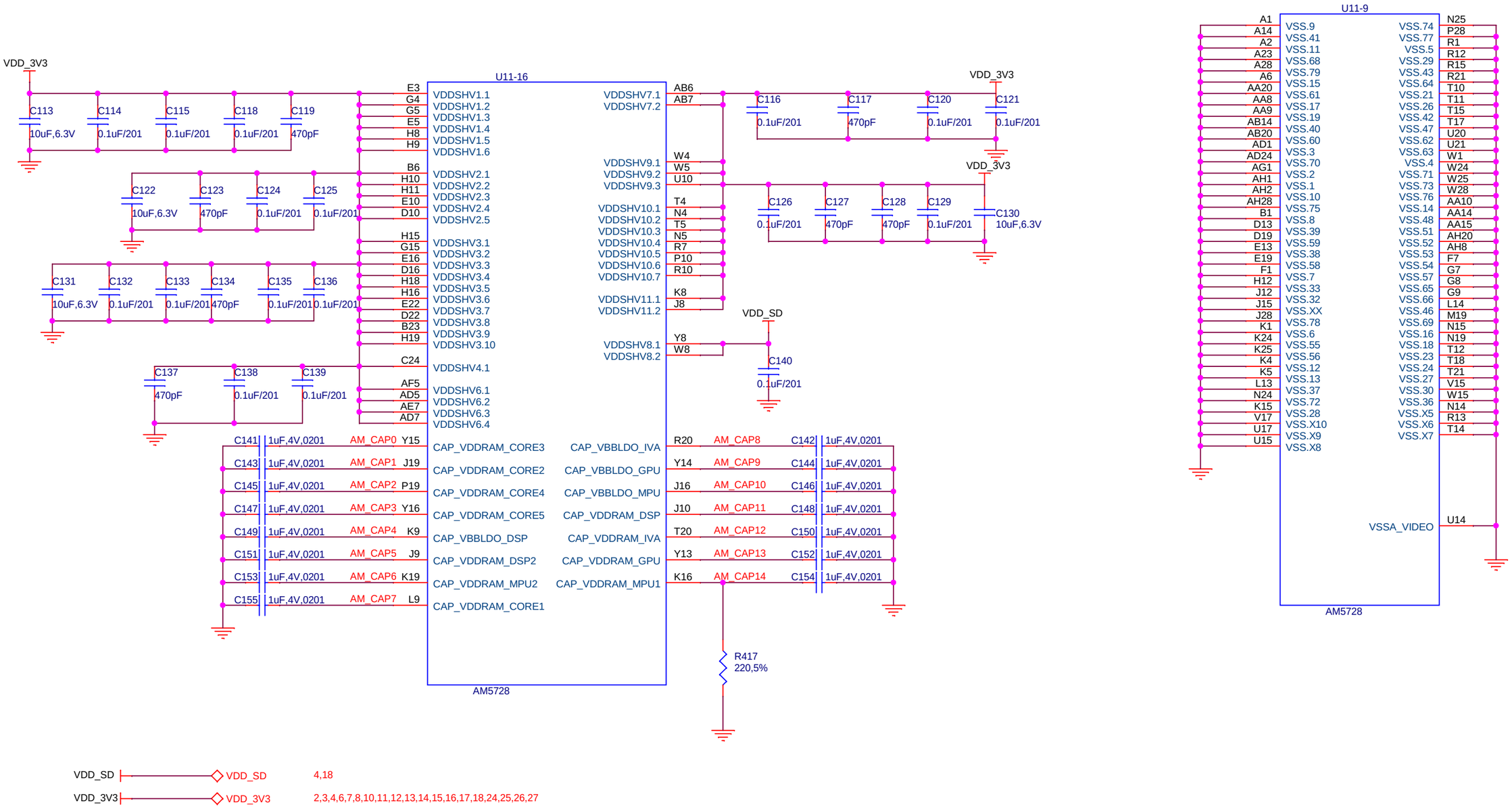
Title	AM572X CLOCKS & RESET	
Size B	Document Number	Rev A0
Date: December 23, 2019	Sheet 8 of 27	



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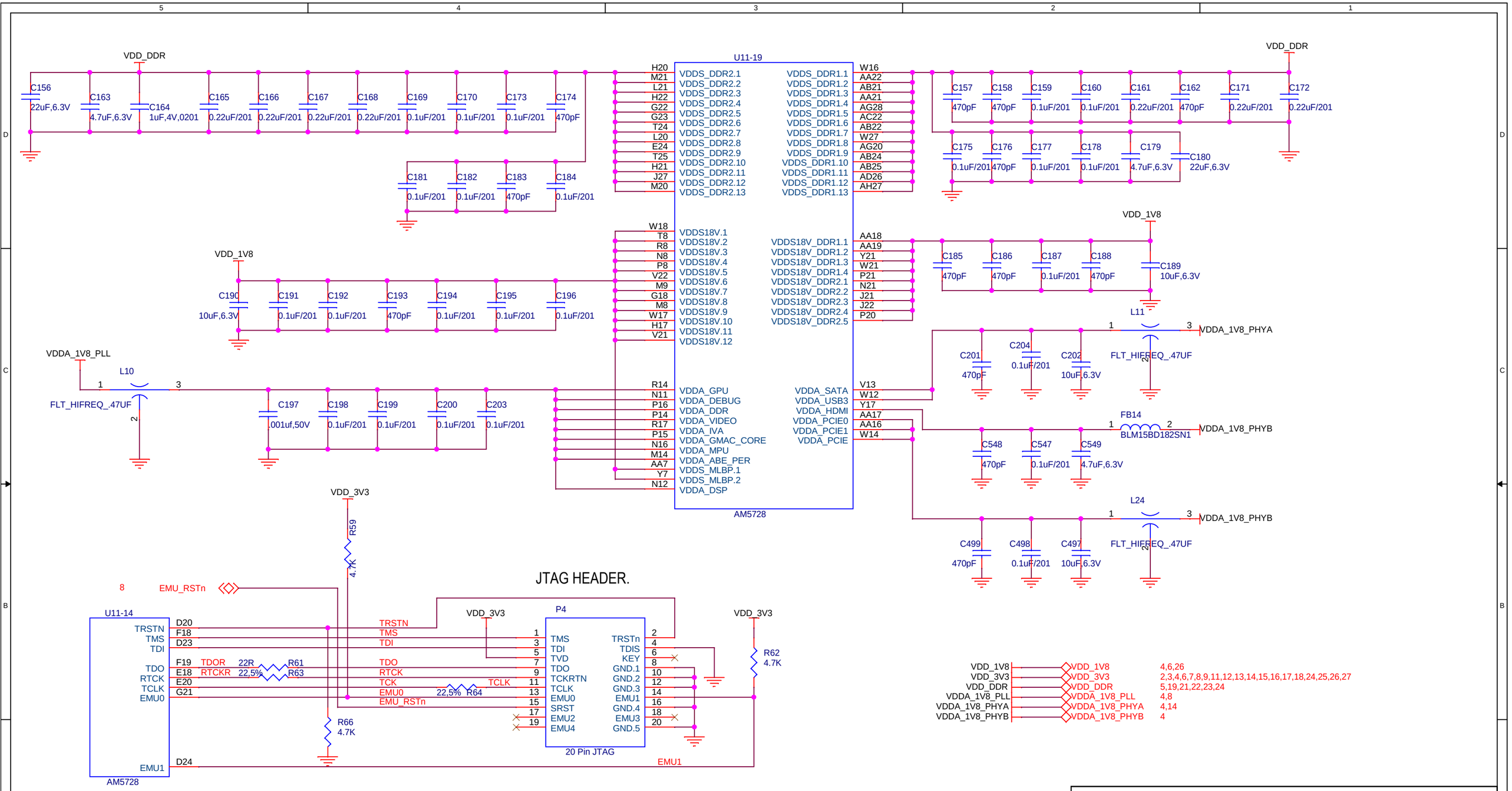
Title	AM572X I/O POWER & GROUND	
Size B	Document Number	Rev A0
Date: December 23, 2019	Sheet 9 of 27	



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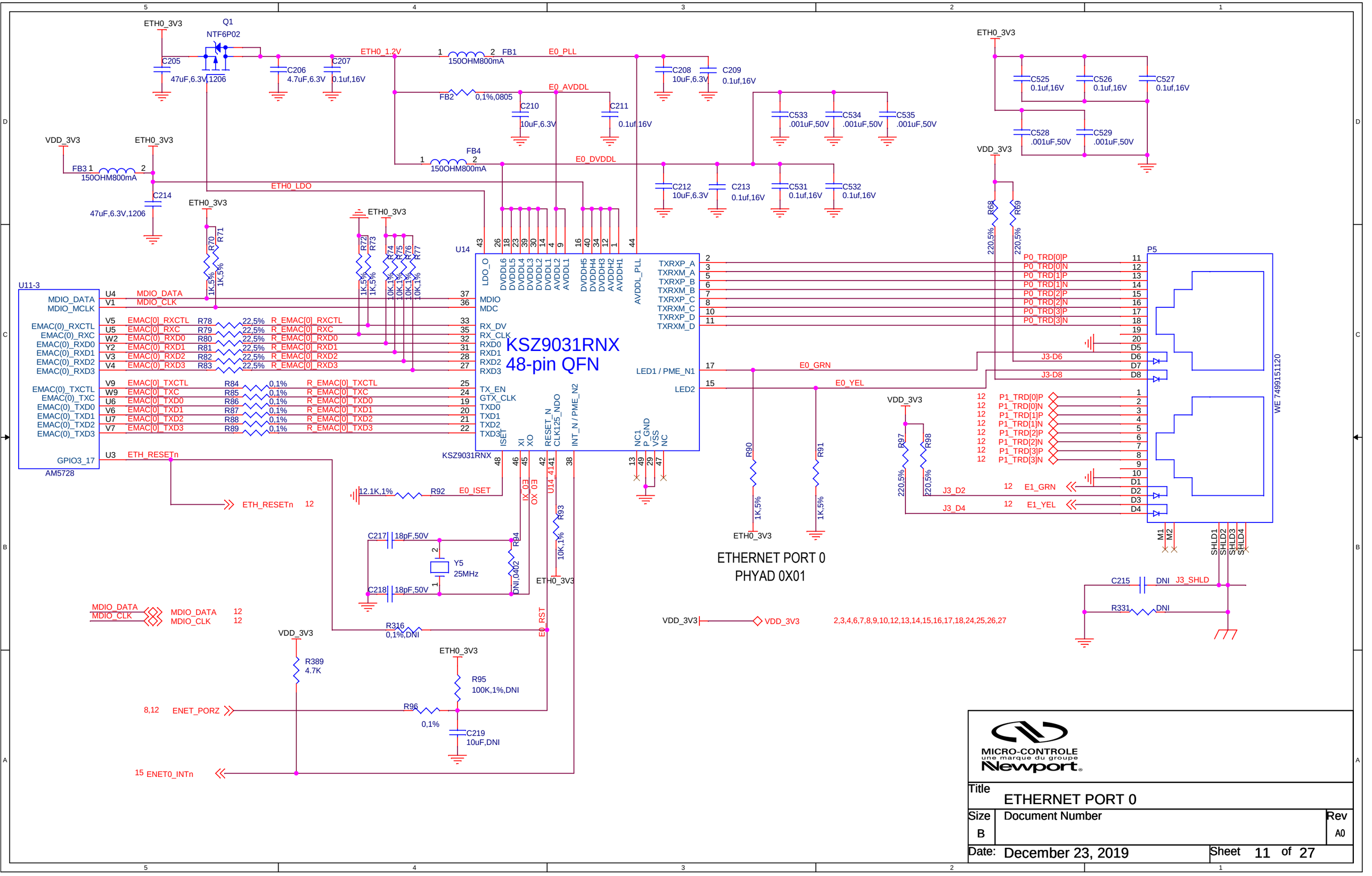
Title	AM572X 1.8V & DDR POWER	
Size B	Document Number	Rev A0
Date: December 23, 2019	Sheet 10 of 27	



Title: ETHERNET PORT 0

Size: B | Document Number | Rev: A0

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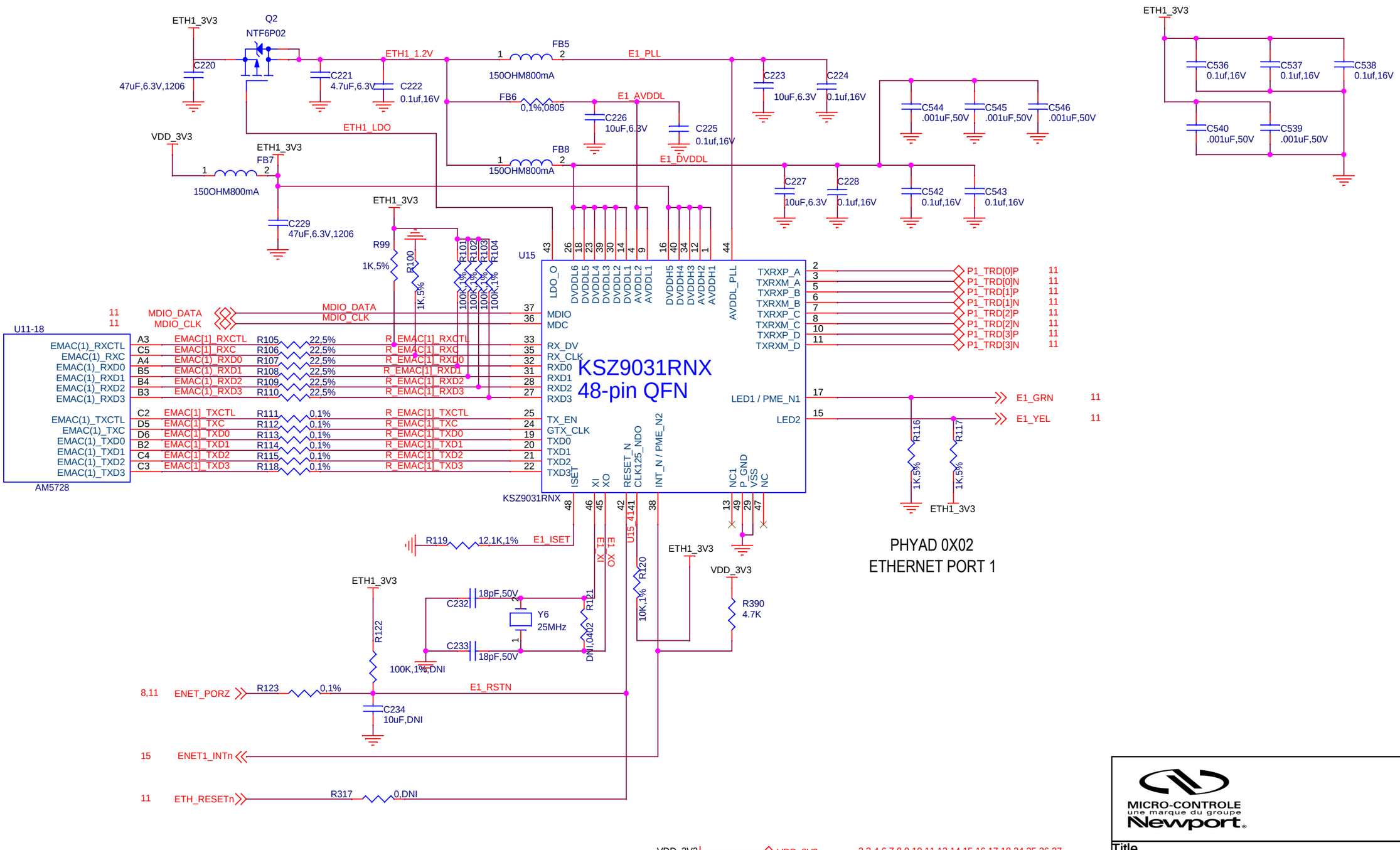

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Title	ETHERNET PORT 1	
Size B	Document Number	Rev A0
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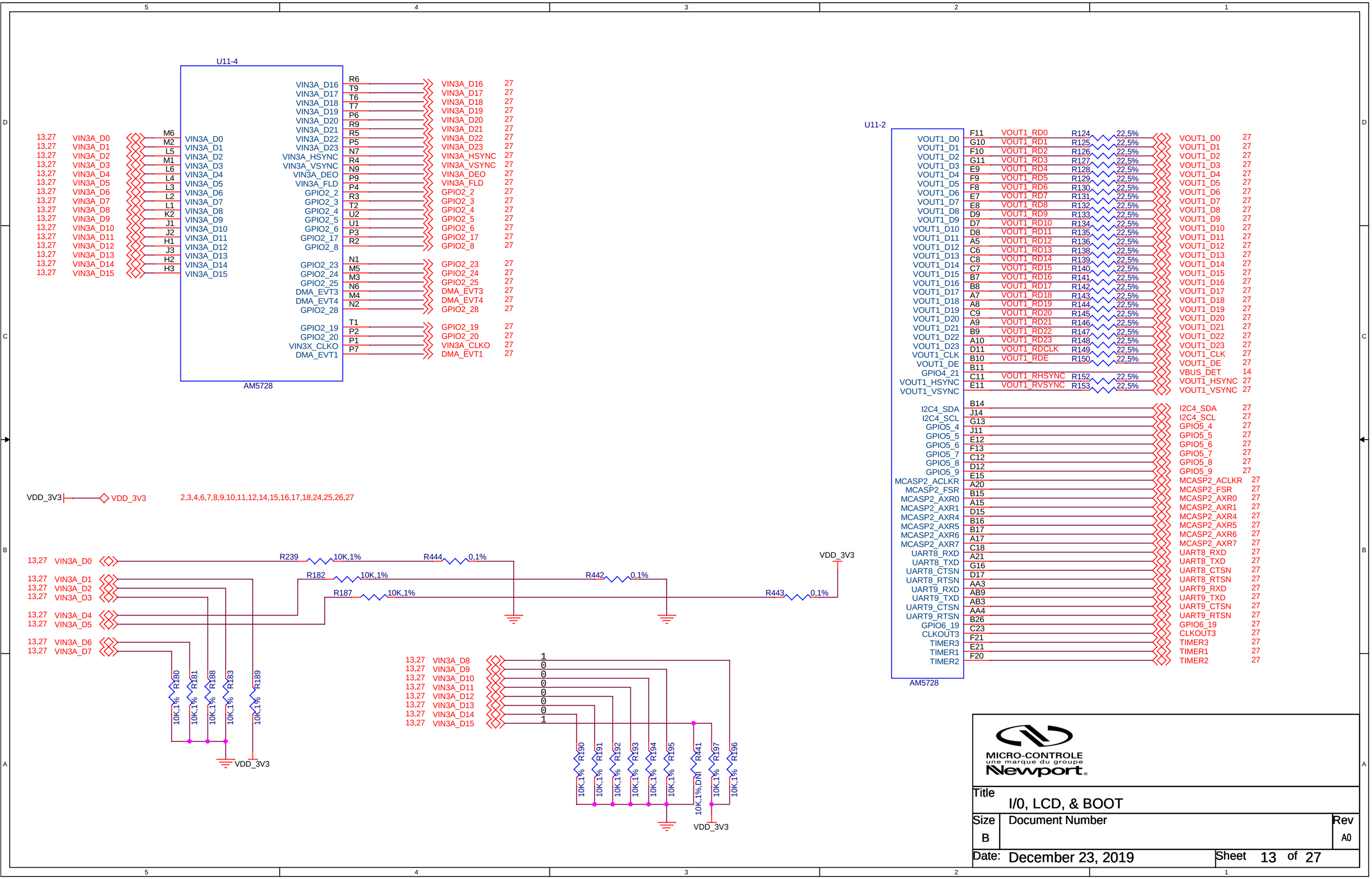

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Title	I/0, LCD, & BOOT	
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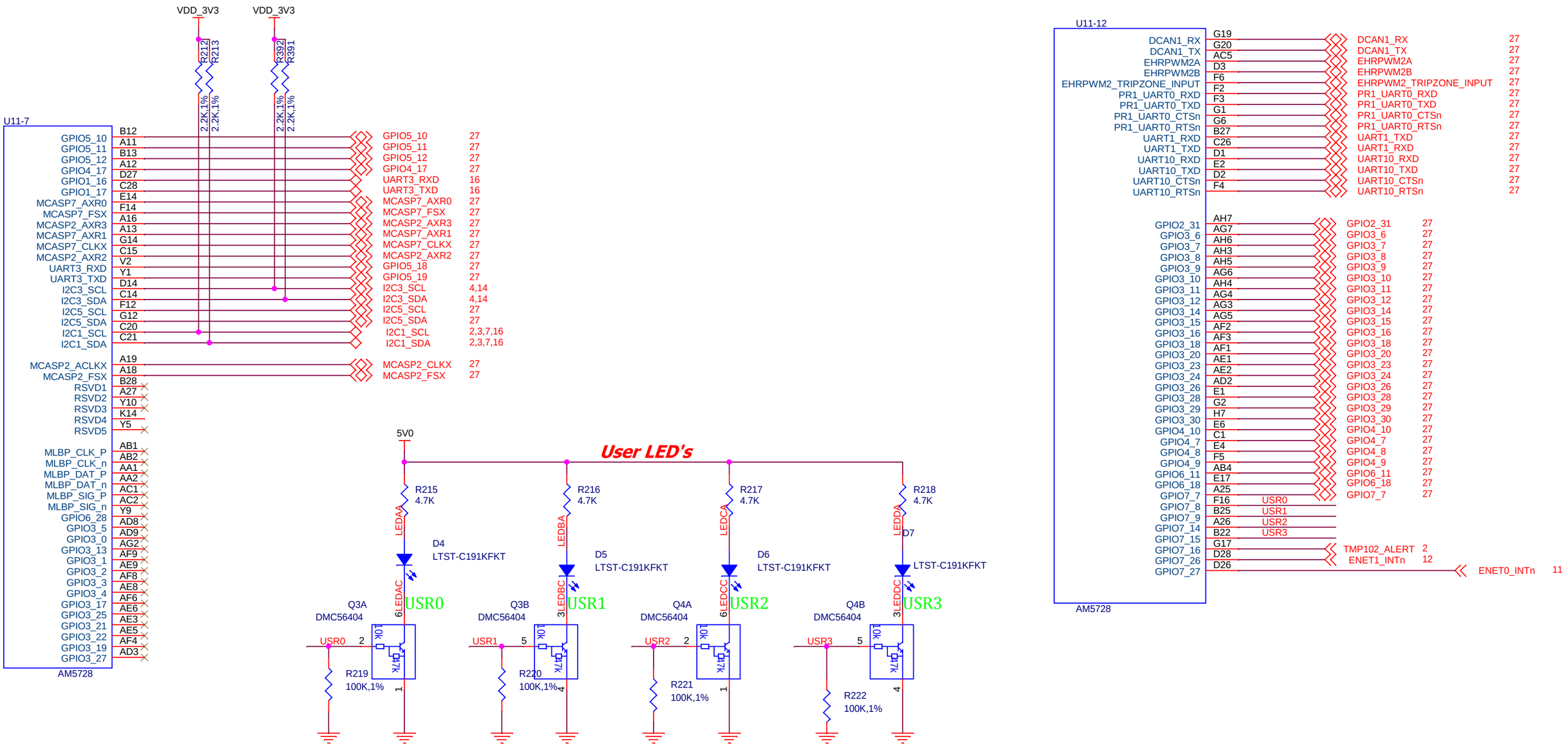

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Title	AM5728 I/O & LEDS	
Size B	Document Number	Rev A0
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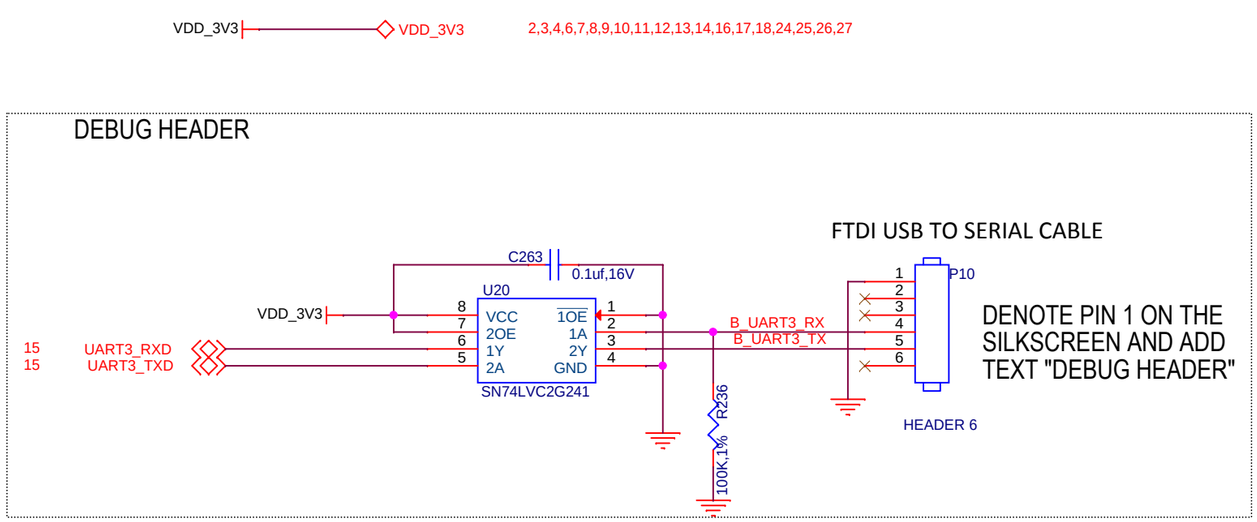

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Title	DEBUG PORT	
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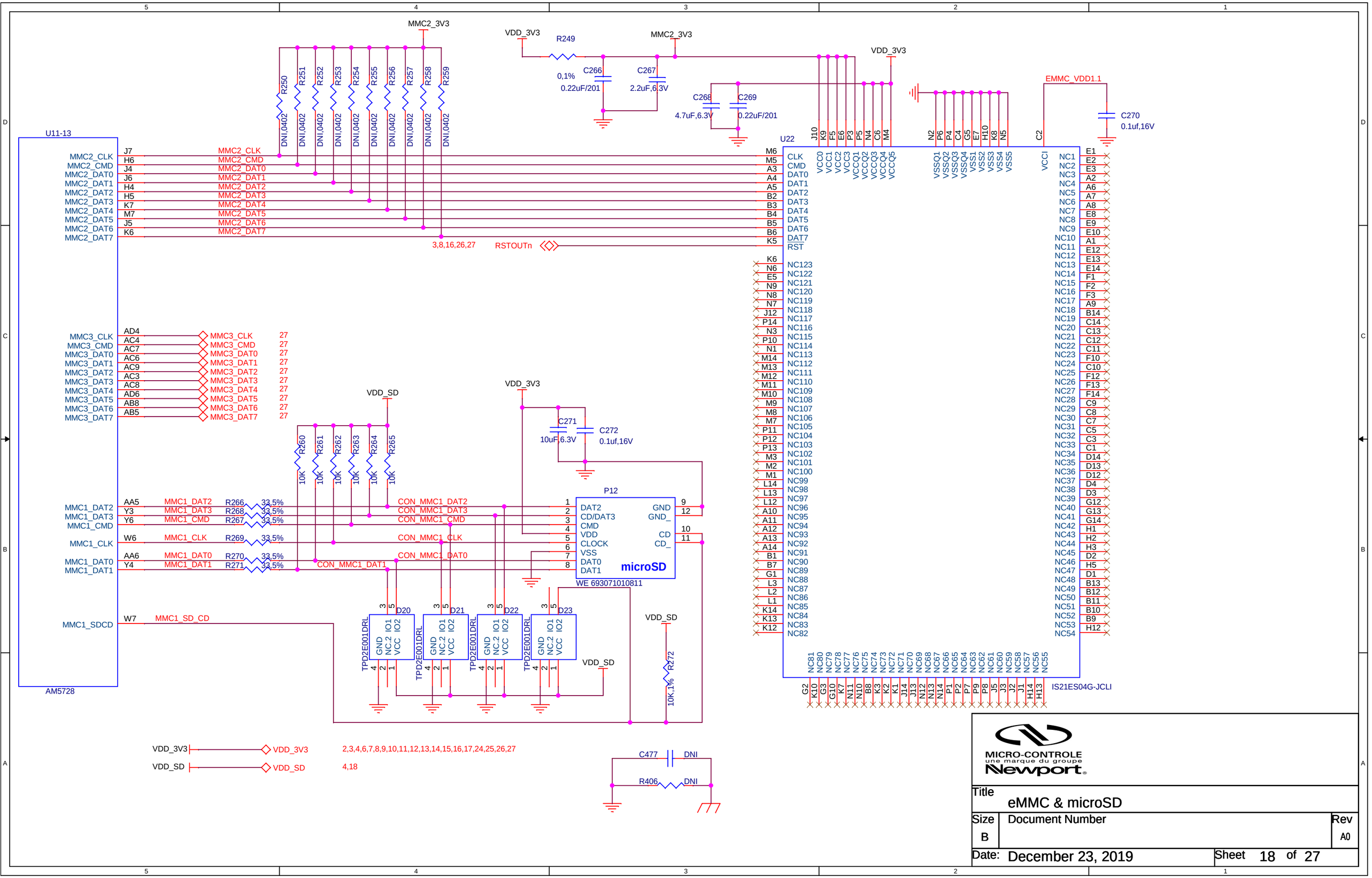

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Title	eMMC & microSD	
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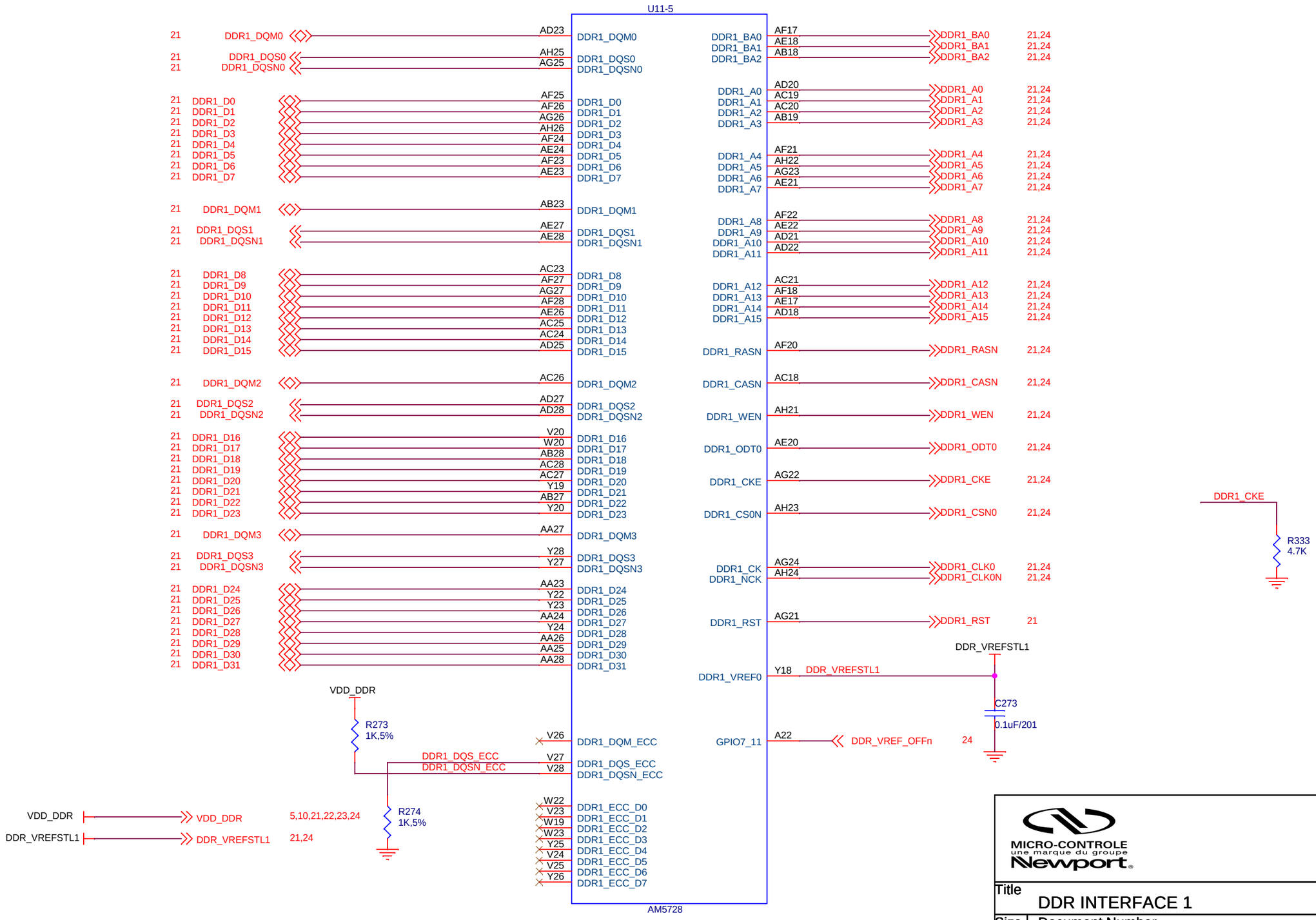

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Title	DDR INTERFACE 1	
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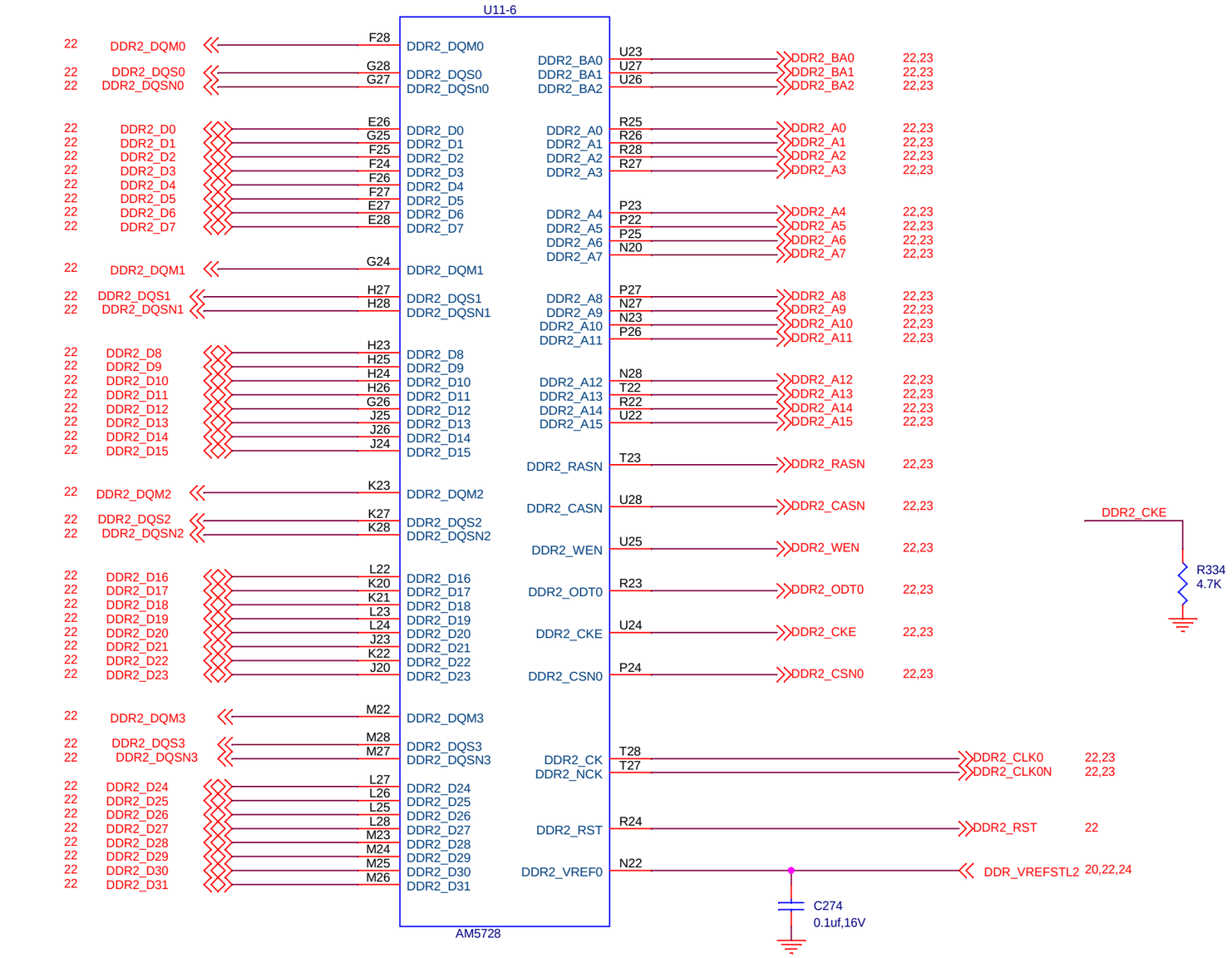

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Title	DDR INTERFACE2	
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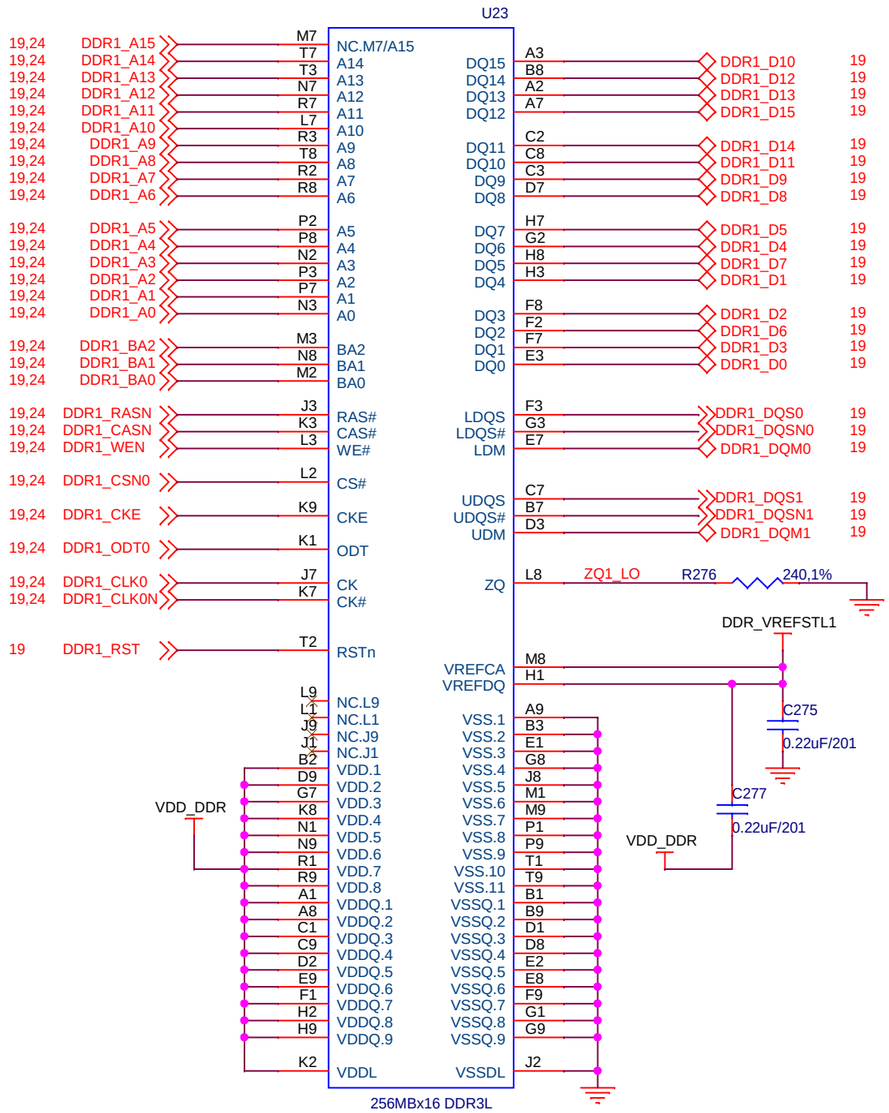

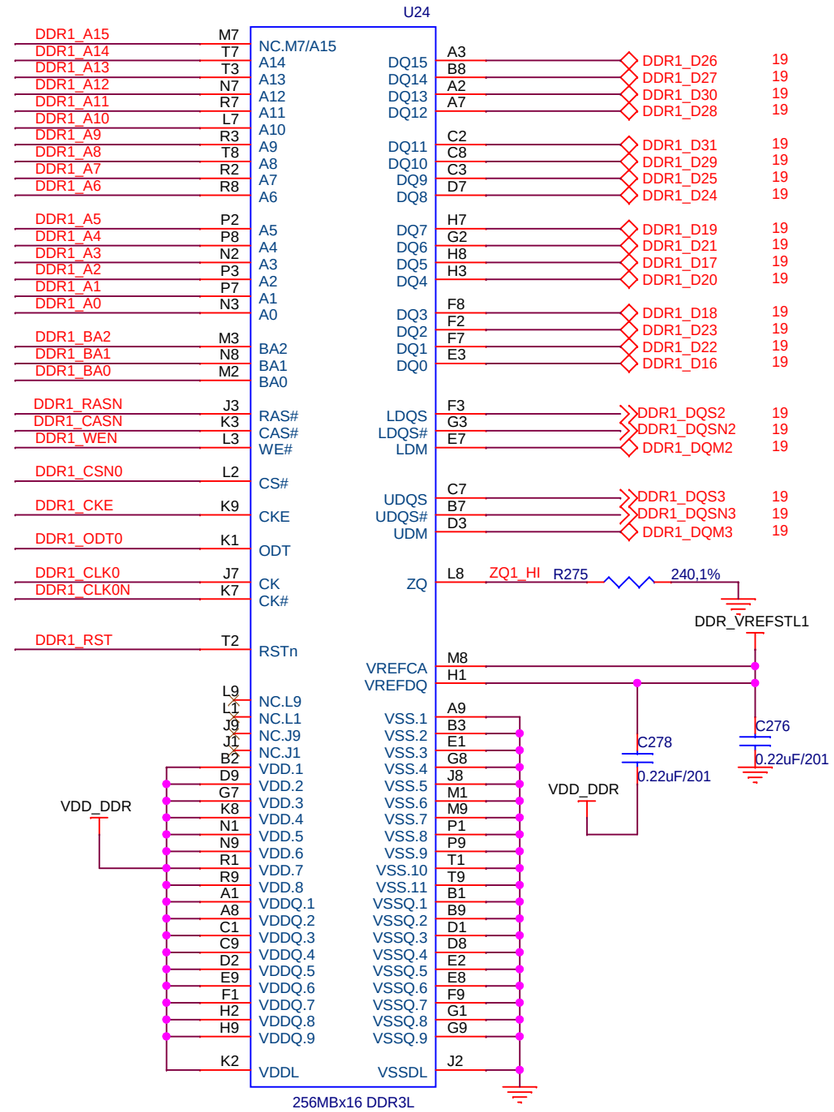

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Title	DDR BANK 1	
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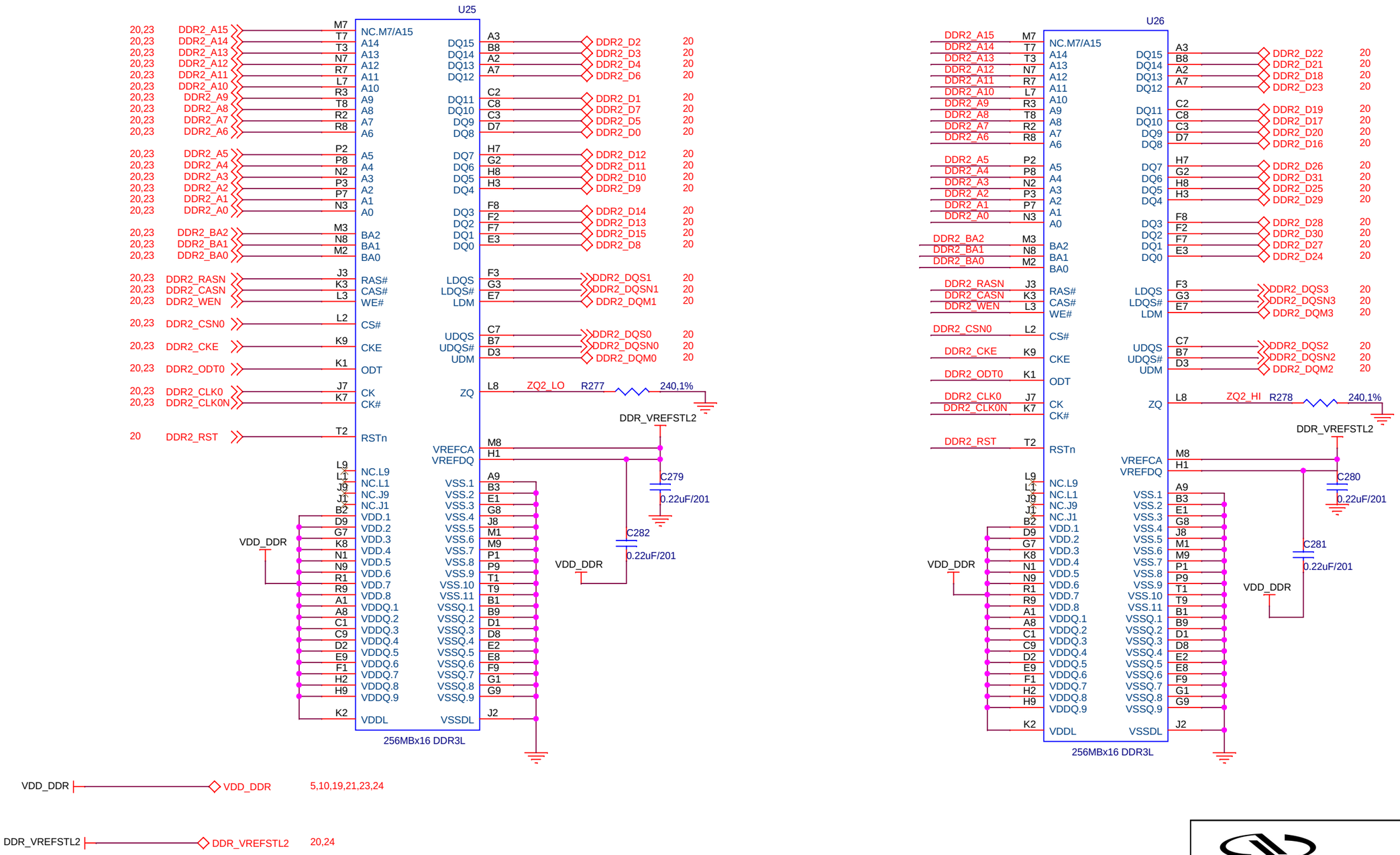

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Title	DDR BANK 2	
Size B	Document Number	Rev A0
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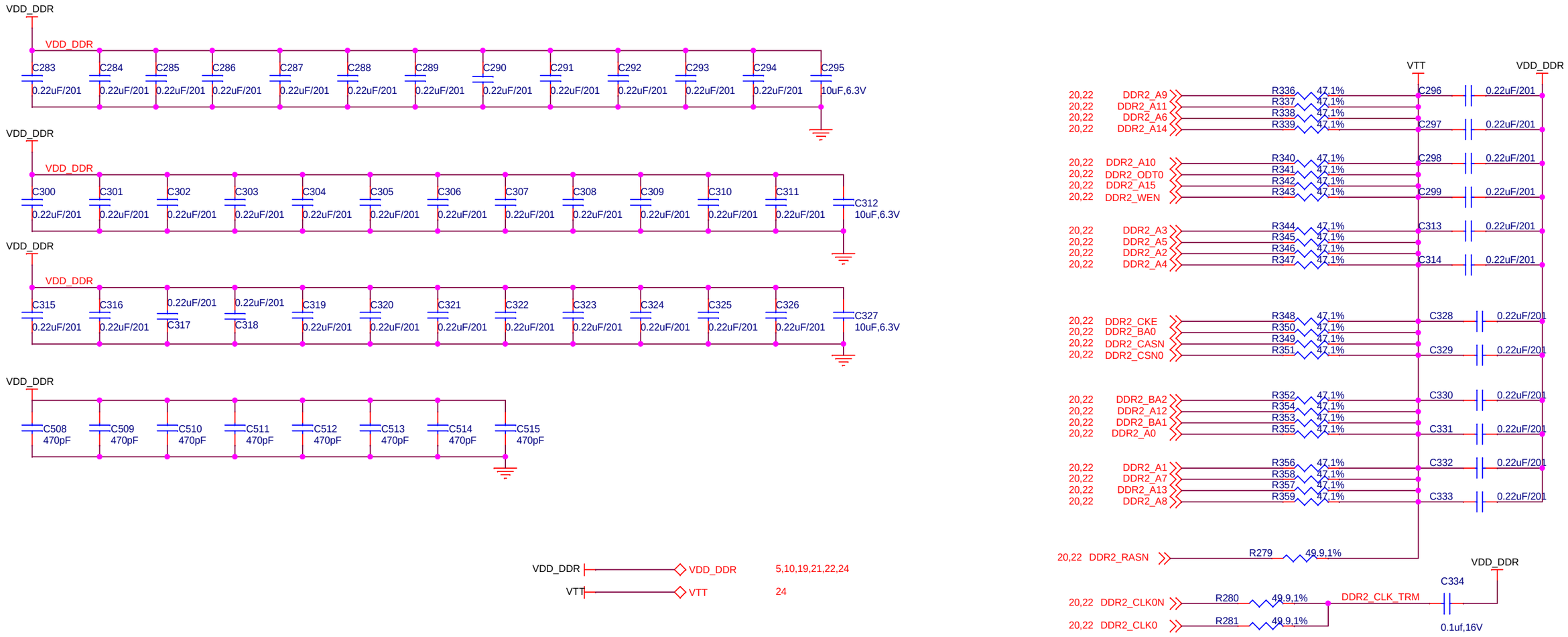

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Title	DDR3L BANK 2 CAPS AND TERMINATIONS	
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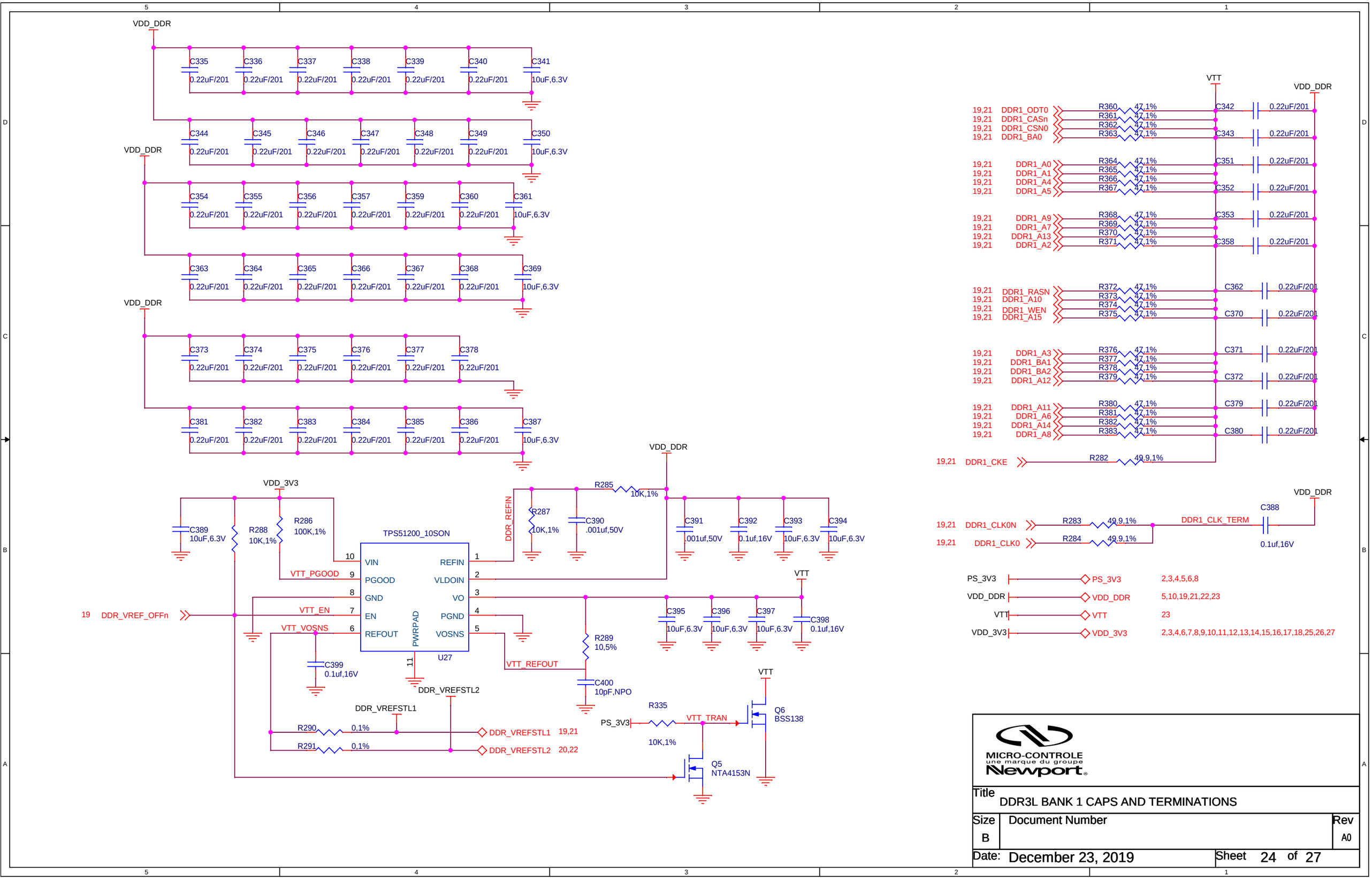

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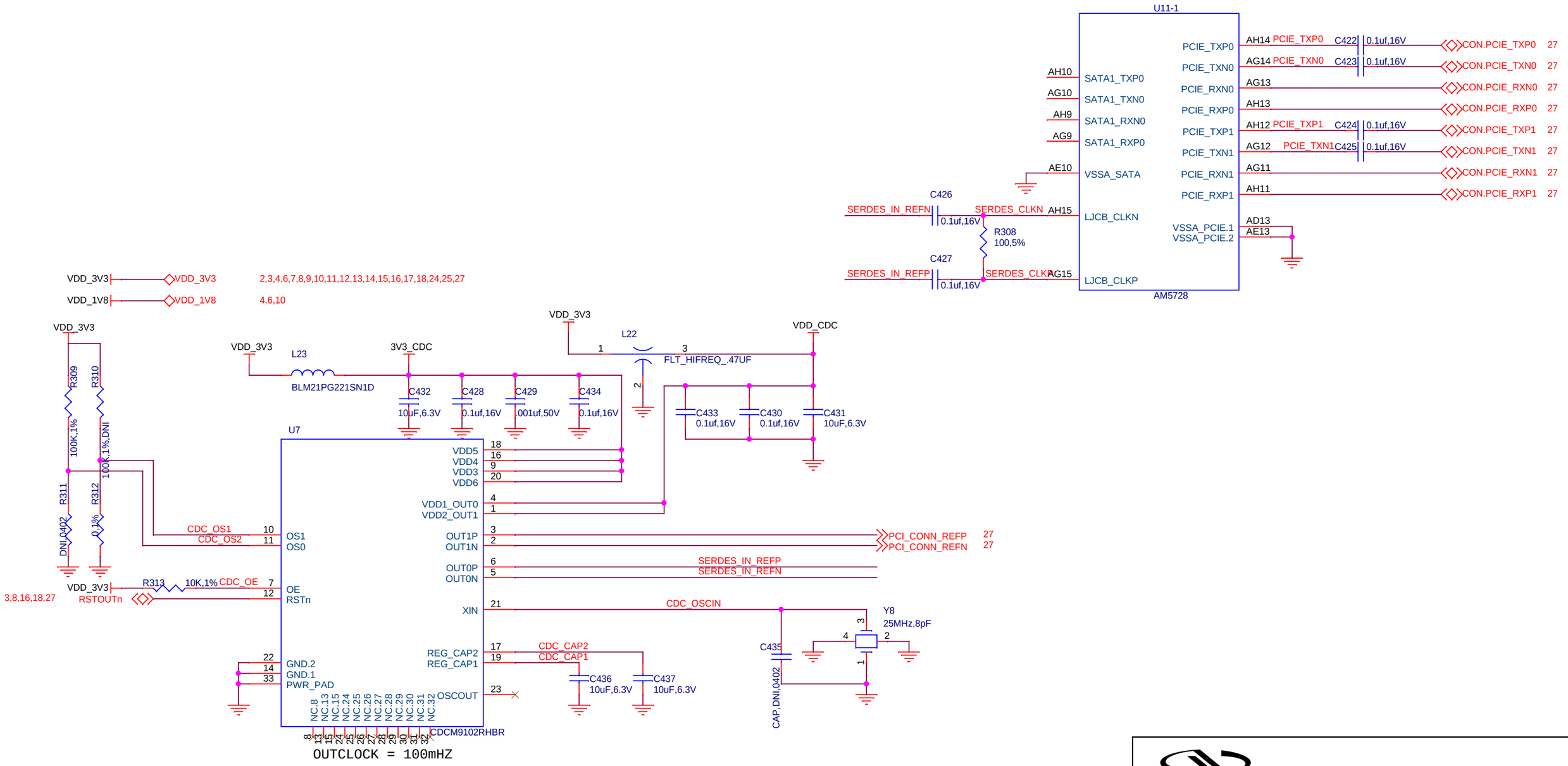
Title	DDR3L BANK 1 CAPS AND TERMINATIONS	
Size B	Document Number	Rev A0
Date: December 23, 2019	Sheet 24 of 27	



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Title	SERDES CLOCK, SATA, AND PCIe	
Size B	Document Number	Rev A0
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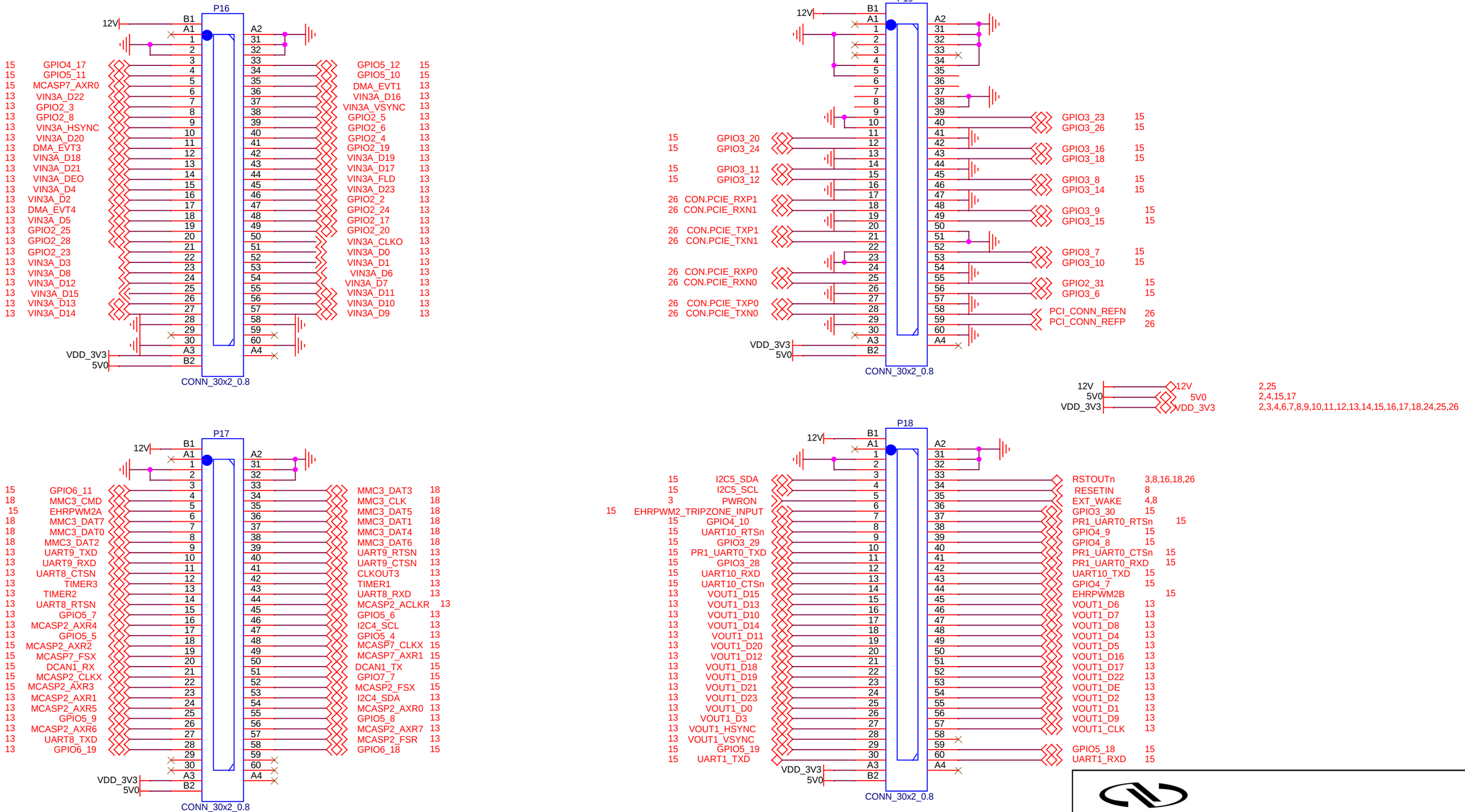

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Title	EXPANSION CONNECTORS	
Size B	Document Number	Rev A0
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