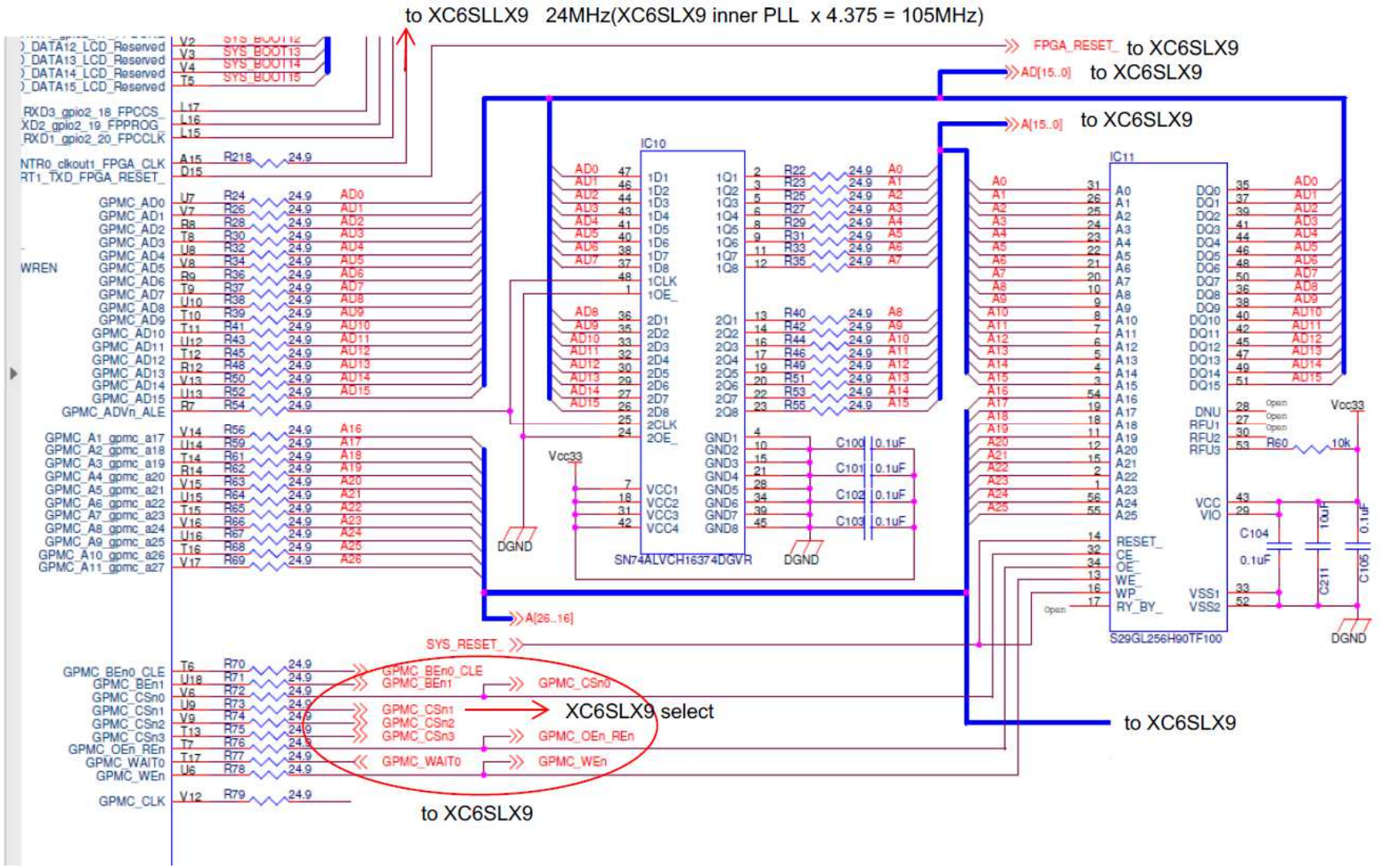
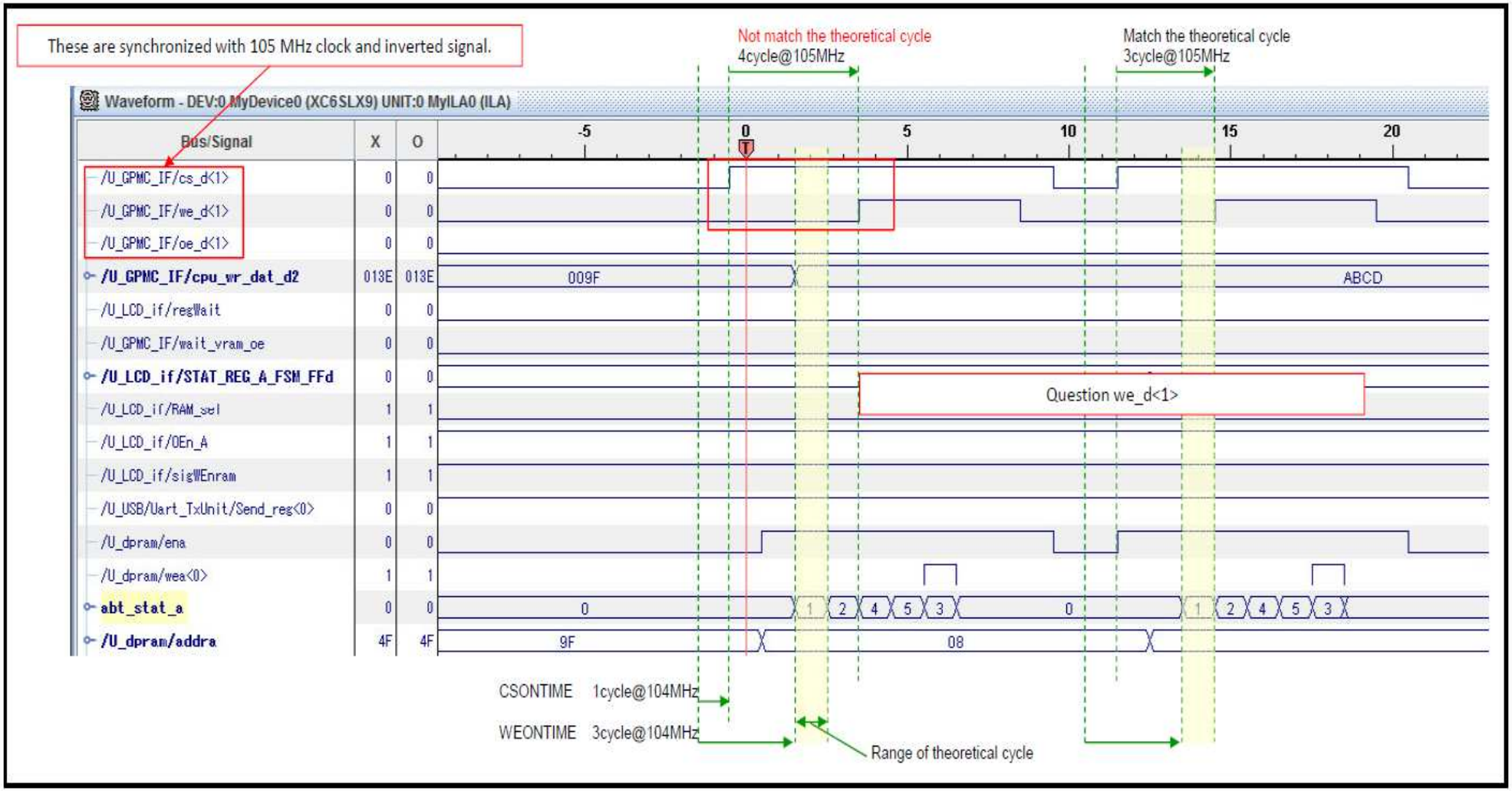

to XC6SLLX9 24MHz(XC6SLX9 inner PLL x 4.375 = 105MHz)
FPGA_RESET_ to XC6SLX9
AD[15..0] to XC6SLX9
A[15..0] to XC6SLX9
A[26..16]
SYS_RESET_
to XC6SLX9
XC6SLX9 select
to XC6SLX9
to XC6SLX9
IC10
SN74ALVCH16374DGVR
IC11
S29GL256H90TF100
Vcc33
DGND
GPMC_WREN
GPMC_ADVn_ALE
GPMC_CLK
GPMC_BEn0_CLE
GPMC_BEn1
GPMC_CSn0
GPMC_CSn1
GPMC_CSn2
GPMC_CSn3
GPMC_OEn_REn
GPMC_WAIT0
GPMC_WEn


These are synchronized with 105 MHz clock and inverted signal.
Not match the theoretical cycle
4cycle@105MHz
Match the theoretical cycle
3cycle@105MHz
Waveform - DEV:0 MyDevice0 (XC6SLX9) UNIT:0 MyILA0 (ILA)
Bus/Signal
X
O
/U_GPMC_IF/cs_d<1>
/U_GPMC_IF/we_d<1>
/U_GPMC_IF/oe_d<1>
/U_GPMC_IF/cpu_wr_dat_d2
/U_LCD_if/regWait
/U_GPMC_IF/wait_vram_oe
/U_LCD_if/STAT_REG_A_FSM_FFd
/U_LCD_if/RAM_sel
/U_LCD_if/OEn_A
/U_LCD_if/sigWEnram
/U_USB/Uart_TxUnit/Send_reg<0>
/U_dpram/ena
/U_dpram/wea<0>
abt_stat_a
/U_dpram/addra
009F
ABCD
Question we_d<1>
9F
08
CSONTIME 1cycle@104MHz
WEONTIME 3cycle@104MHz
Range of theoretical cycle