1. Here is the result of core0 on normal board and core1 on normal board:

C66xx\_1: GEL Output: Setup\_Memory\_Map...

C66xx\_1: GEL Output: Setup\_Memory\_Map... Done.

C66xx\_1: GEL Output: C6678L GEL file Ver is 2.004

C66xx\_1: GEL Output: Global Default Setup...

C66xx\_1: GEL Output: Setup Cache...

C66xx\_1: GEL Output: L1P = 32K

C66xx\_1: GEL Output: L1D = 32K

C66xx\_1: GEL Output: L2 = ALL SRAM

C66xx\_1: GEL Output: Setup Cache... Done.

C66xx\_1: GEL Output: Main PLL (PLL1) Setup ...

C66xx\_1: GEL Output: PLL in Bypass ...

C66xx\_1: GEL Output: PLL1 Setup for DSP @ 1000.0 MHz.

C66xx\_1: GEL Output: SYSCLK2 = 333.3333 MHz, SYSCLK5 = 200.0 MHz.

C66xx\_1: GEL Output: SYSCLK8 = 15.625 MHz.

C66xx\_1: GEL Output: PLL1 Setup... Done.

C66xx\_1: GEL Output: Power on all PSC modules and DSP domains...

C66xx\_1: GEL Output: Security Accelerator disabled!

C66xx\_1: GEL Output: Power on all PSC modules and DSP domains... Done.

C66xx\_1: GEL Output: PA PLL (PLL3) Setup ...

C66xx\_1: GEL Output: PA PLL Setup... Done.

C66xx\_1: GEL Output: DDR3 PLL (PLL2) Setup ...

C66xx\_1: GEL Output: DDR3 PLL Setup... Done.

C66xx\_1: GEL Output: DDR begin (1333 auto)

C66xx\_1: GEL Output: XMC Setup ... Done

C66xx\_1: GEL Output:

DDR3 initialization is complete.

C66xx\_1: GEL Output: DDR done

C66xx\_1: GEL Output: DDR3 memory test... Started

C66xx\_1: GEL Output: DDR3 memory test... Passed

C66xx\_1: GEL Output: PLL and DDR Initialization completed(0) ...

C66xx\_1: GEL Output: configSGMIISerdes Setup... Begin

C66xx\_1: GEL Output:

SGMII SERDES has been configured.

C66xx\_1: GEL Output: Enabling EDC ...

C66xx\_1: GEL Output: L1P error detection logic is enabled.

C66xx\_1: GEL Output: L2 error detection/correction logic is enabled.

C66xx\_1: GEL Output: MSMC error detection/correction logic is enabled.

C66xx\_1: GEL Output: Enabling EDC ...Done

C66xx\_1: GEL Output: Configuring CPSW ...

C66xx\_1: GEL Output: Configuring CPSW ...Done

C66xx\_1: GEL Output: Global Default Setup... Done.

1. Here is the result of core0 on the abnormal board,the red text is the error:

C66xx\_0: GEL Output: Setup\_Memory\_Map...

C66xx\_0: GEL Output: Setup\_Memory\_Map... Done.

C66xx\_0: GEL Output: C6678L GEL file Ver is 2.004

C66xx\_0: GEL Output: Global Default Setup...

C66xx\_0: GEL Output: Setup Cache...

C66xx\_0: GEL Output: L1P = 32K

C66xx\_0: GEL Output: L1D = 32K

C66xx\_0: GEL Output: L2 = ALL SRAM

C66xx\_0: GEL Output: Setup Cache... Done.

C66xx\_0: GEL Output: Main PLL (PLL1) Setup ...

C66xx\_0: GEL Output: PLL in Bypass ...

C66xx\_0: GEL Output: PLL1 Setup for DSP @ 1000.0 MHz.

C66xx\_0: GEL Output: SYSCLK2 = 333.3333 MHz, SYSCLK5 = 200.0 MHz.

C66xx\_0: GEL Output: SYSCLK8 = 15.625 MHz.

C66xx\_0: GEL Output: PLL1 Setup... Done.

C66xx\_0: GEL Output: Power on all PSC modules and DSP domains...

C66xx\_0: GEL Output: Security Accelerator disabled!

C66xx\_0: GEL Output: Power on all PSC modules and DSP domains... Done.

C66xx\_0: GEL Output: PA PLL (PLL3) Setup ...

C66xx\_0: GEL Output: PA PLL Setup... Done.

C66xx\_0: GEL Output: DDR3 PLL (PLL2) Setup ...

C66xx\_0: GEL Output: DDR3 PLL Setup... Done.

C66xx\_0: GEL Output: DDR begin (1333 auto)

C66xx\_0: GEL Output: XMC Setup ... Done

C66xx\_0: Trouble Writing Memory Block at 0x21000008 on Page 0 of Length 0x4: (Error -1060 @ 0x21000008) Device is not responding to the request. Reset the device, and retry the operation. If error persists, confirm configuration, power-cycle the board, and/or try more reliable JTAG settings (e.g. lower TCLK). (Emulation package 5.0.872.0)

Global\_Default\_Setup() cannot be evaluated.

target access failed

at \*((unsigned int \*) (0x21000000+0x00000008))=TEMP [c6678l\_dzs.gel:252]

at ddr3\_setup\_auto\_lvl\_1333(0) [c6678l\_dzs.gel:878]

atGlobal\_Default\_Setup\_Silent() [c6678l\_dzs.gel:1578]

atGlobal\_Default\_Setup()