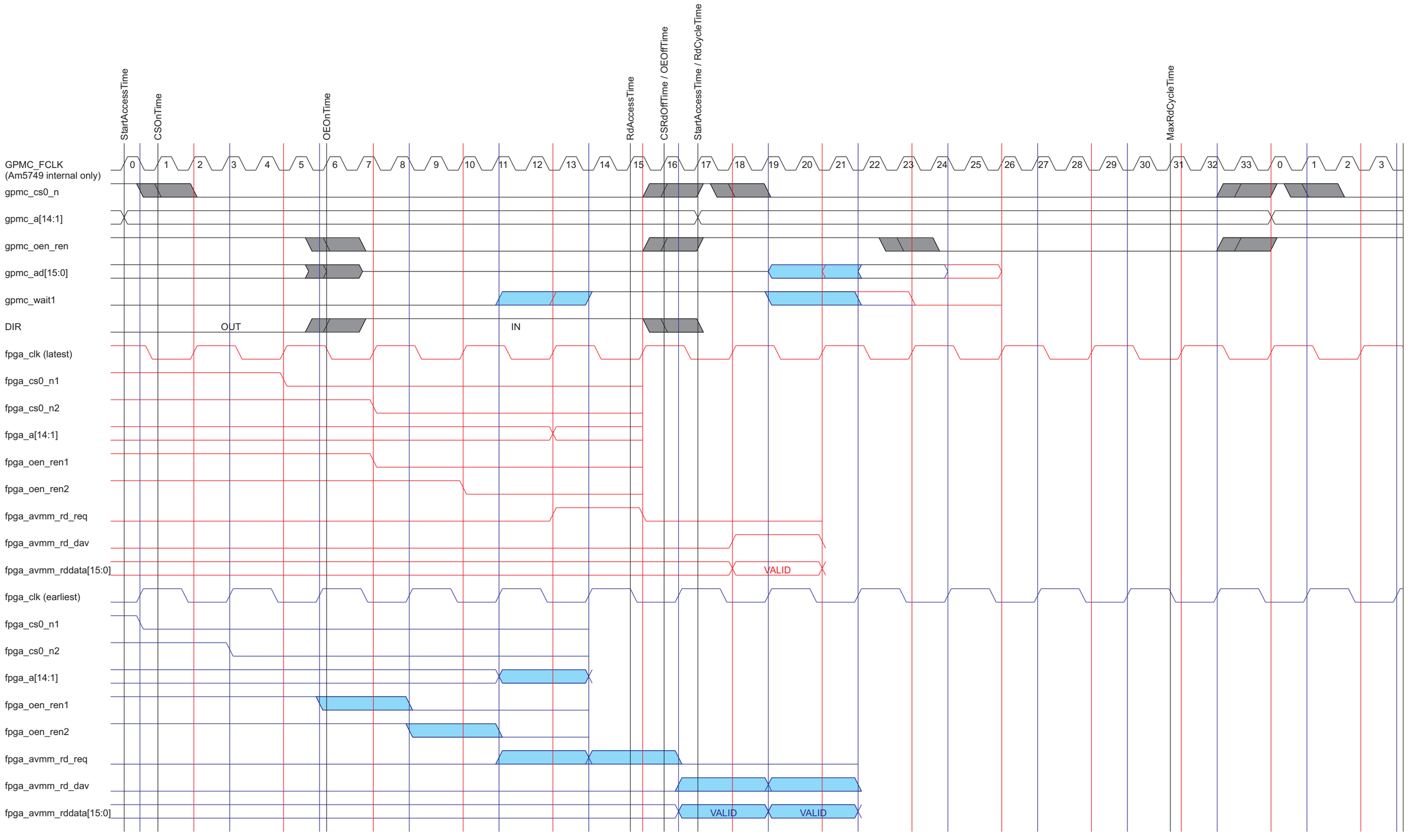
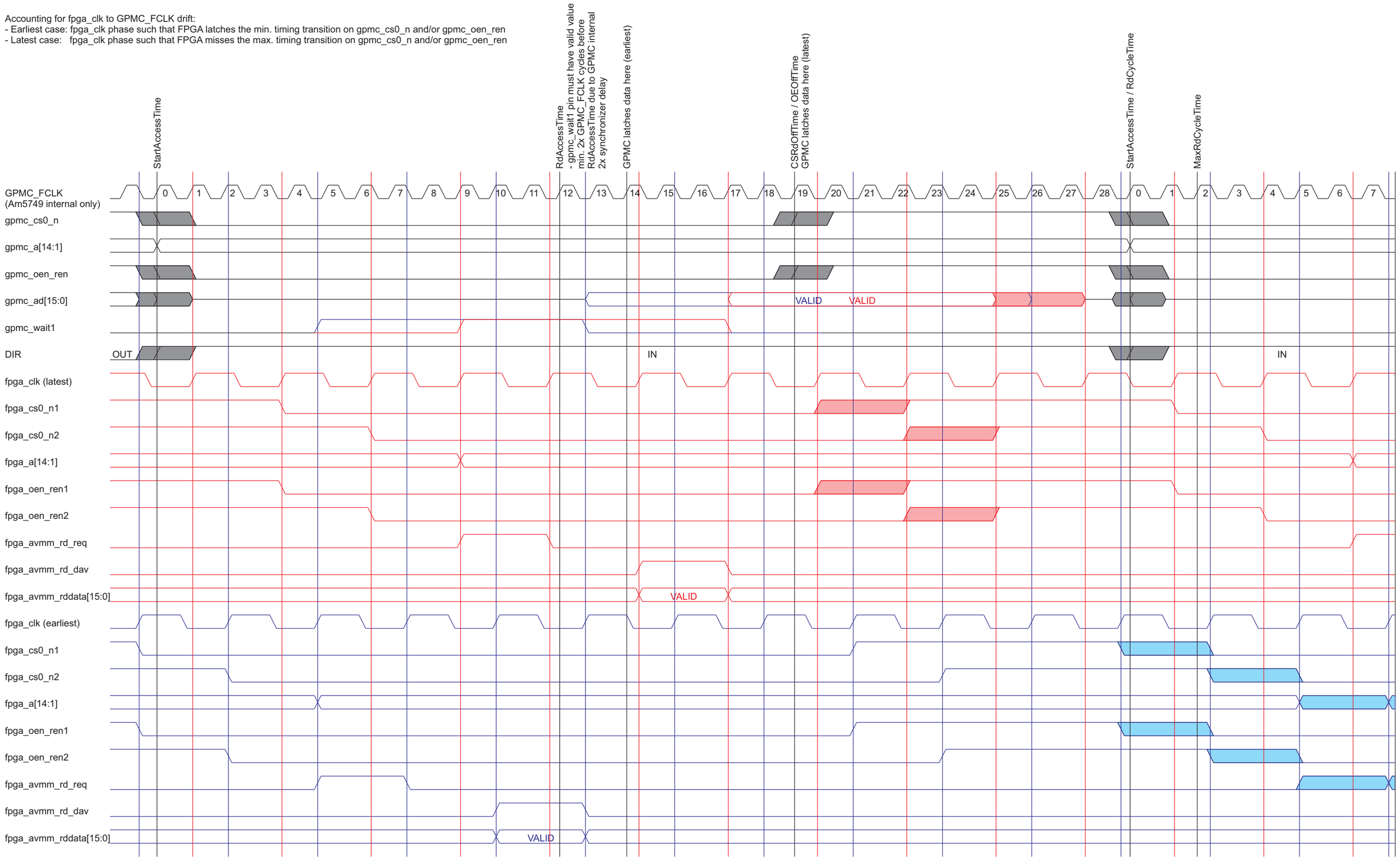
GPMC - Asynchronous Non-Multiplexed NOR Flash - Single Read with GPMC Default Register Settings - IGNORE THIS PAGE
Scale: 2.66mm/ns



GPMC - Asynchronous Non-Multiplexed NOR Flash - Single Read with GPMC Custom Register Settings

Scale: 2.66mm/ns

Accounting for fpga_clk to GPMC_FCLK drift:
- Earliest case: fpga_clk phase such that FPGA latches the min. timing transition on gpmc_cs0_n and/or gpmc_oen_ren
- Latest case: fpga_clk phase such that FPGA misses the max. timing transition on gpmc_cs0_n and/or gpmc_oen_ren



GPMC - Asynchronous Non-Multiplexed NOR Flash - Single Write with GPMC Custom Register Settings
Scale: 2.66mm/ns

Accounting for fpga_clk to GPMC_FCLK drift:
- Earliest case: fpga_clk phase such that FPGA latches the min. timing transition on gpmc_cs0_n and/or gpmc_wen
- Latest case: fpga_clk phase such that FPGA misses the max. timing transition on gpmc_cs0_n and/or gpmc_wen