```
**********************************************
*             PCIe Test Start                *
Enter: E for Endpoint or R for Root Complex
R
*               RC mode                      *
*               RC mode                      *
**********************************************

Version #: 0x0202000d; string PCIE LLD Revision: 02.02.00.13:Sep 21 2018:20:03:
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PCIe Power Up.
PLL configured.
Successfully configured Inbound Translation!
Successfully configured Outbound Translation!
Starting link training...
Link is up.
Checking link speed and # of lanes
Expect 1 lanes, found 1 lanes (PASS)
Expect gen 2 speed, found gen 2 speed (PASS)
Root Complex received data.
RC waiting for 10 of each of 2 types of interrupts
RC got all 20 interrupts
EDMA write 65536 bytes with 184931 cycles
EDMA read 65536 bytes with 198244 cycles
Root Complex DMA received data.
EDMA Test passed.
=== this is not an optimized example ===
Test passed.
```