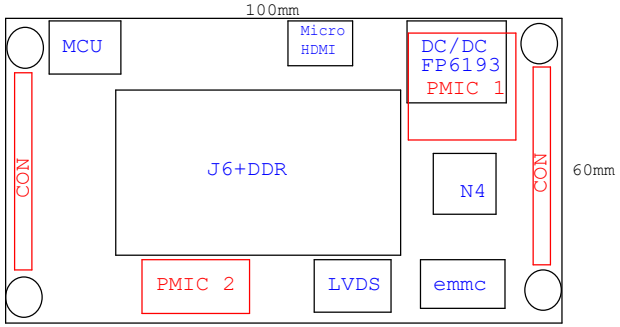


Title	<Title>	
Size A3	Document Number <Doc>	Rev <RevCode>
Date: Thursday, April 19, 2018	Sheet 1 of 14	

CPU board

J6 Entry ES1.0

Data Manual: SPRS960_DRA71x_J6Entry_Aug2016
Package: 17x17mm, 625 BGA-FC, 0.65mm Pitch
Pinlist: J6Entry_Ch3_pinlist_v0.9.xls
Ballmap: J6Entry_pkg_netlist_17mm_v1.0.xlsx
PCB Footprint: J6Entry_DRA71x_ZDN_v4
SCH Symbol: IC_J6Entry_17mm_625BGA_v0.44

GPMC

MEMORY - Nonvoltatile

MEDIA CARDS

VIDEO IN PORT

CAMERA PORT

DISPLAY

HDMI

GPIO

CONTROL

SYSTEM

RTC

CLOCKING

I2C

Debug

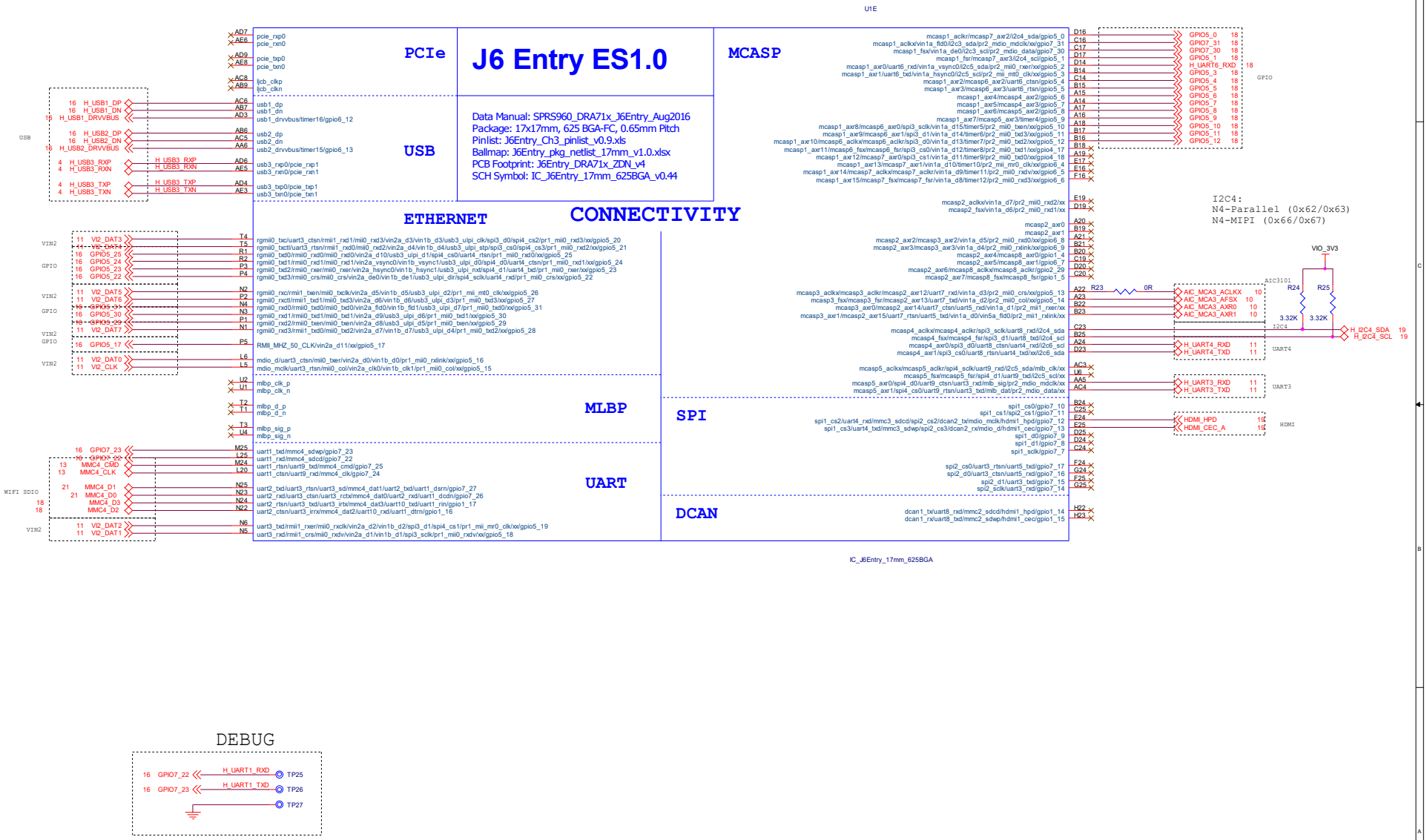
Si Test

IC_J6Entry_17mm_625BGA

I2C1:
BQ32000 (0xD0/0xD1)
LP8733xxRHDRQ1(0x60)
LP8732xxRHDRQ1(0x61)

Title	NU100
Size	C
Document Number	J6E MEM VIP CAM DIS SYS
Rev	0.1
Date:	Thursday, April 19, 2018
Sheet	2 of 14

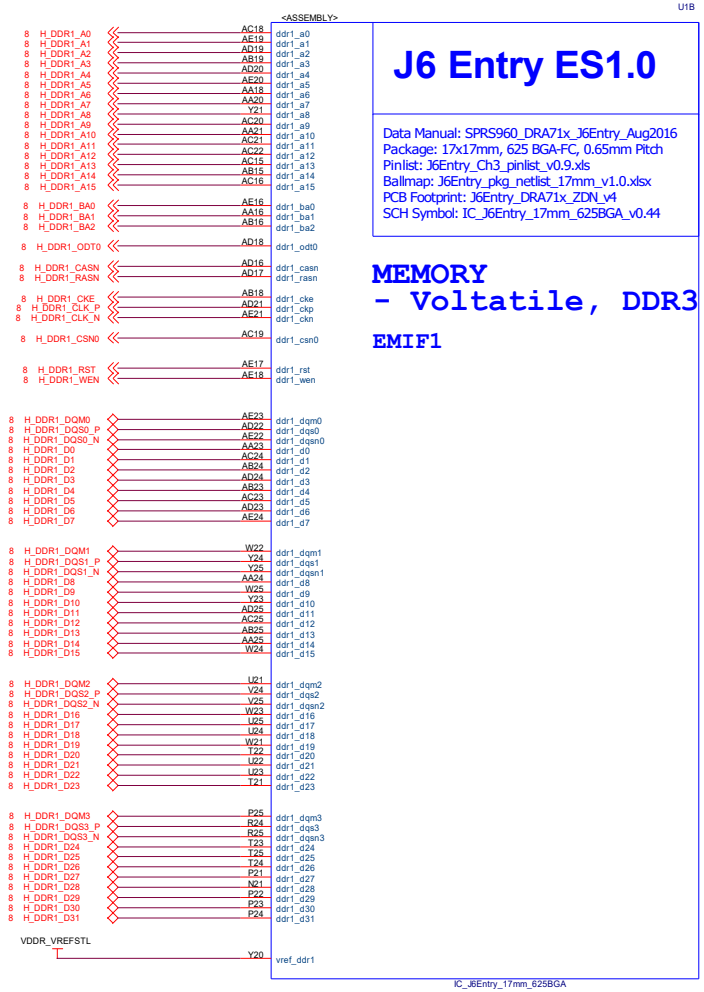
CPU board



DEBUG

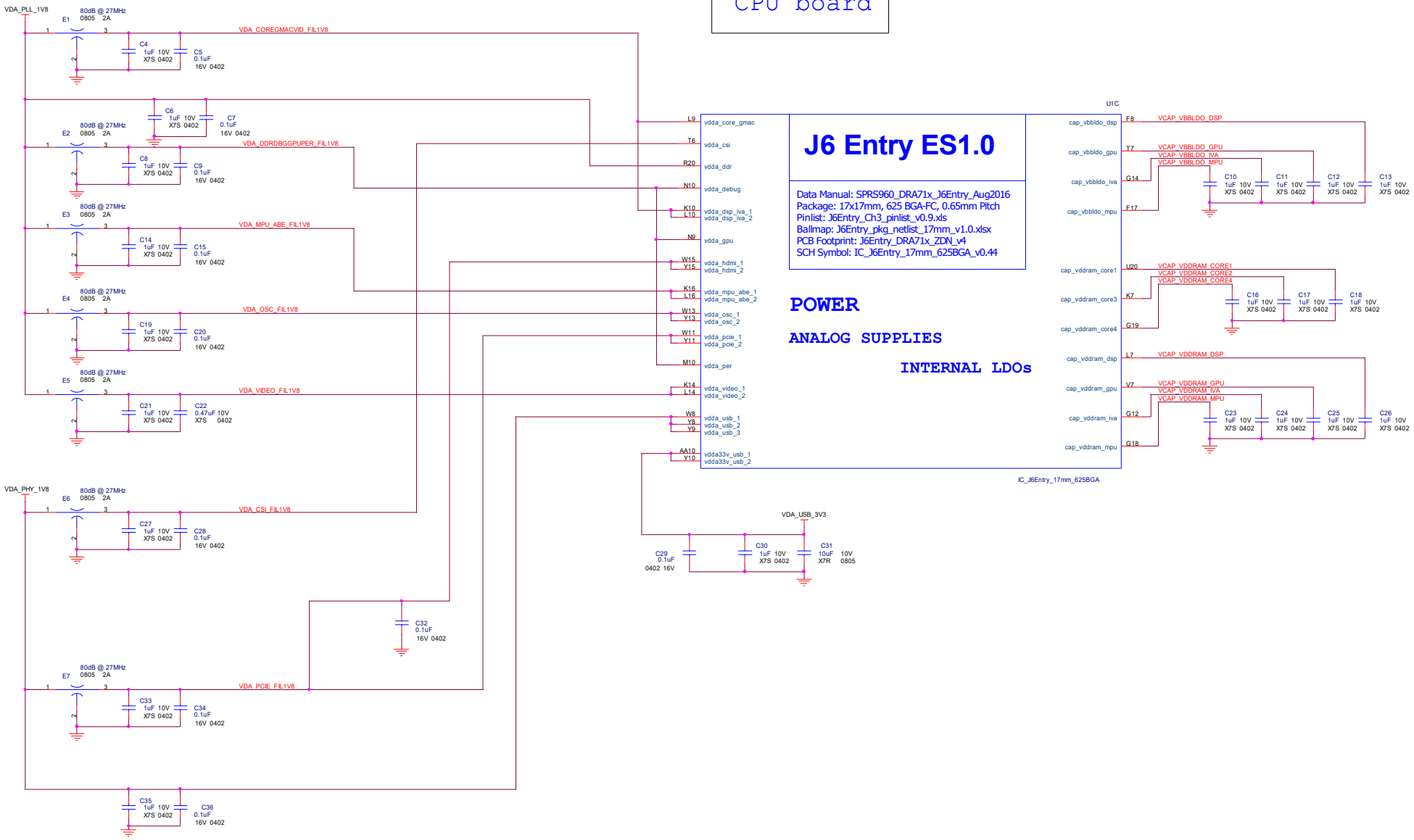
Title	NU100		
Size C	Document Number J6E CNTVY		Rev 0.1
Date: Thursday, April 19, 2018	Sheet 3	of 14	

CPU board



Title	NU100	
Size C	Document Number J6E DDR	Rev 0.1
Date: Thursday, April 19, 2018	Sheet 4 of 14	

CPU board



Title	NU100
Size	C
Document Number	J6E ANA PWR
Rev	0.1
Date:	Thursday, April 19, 2018
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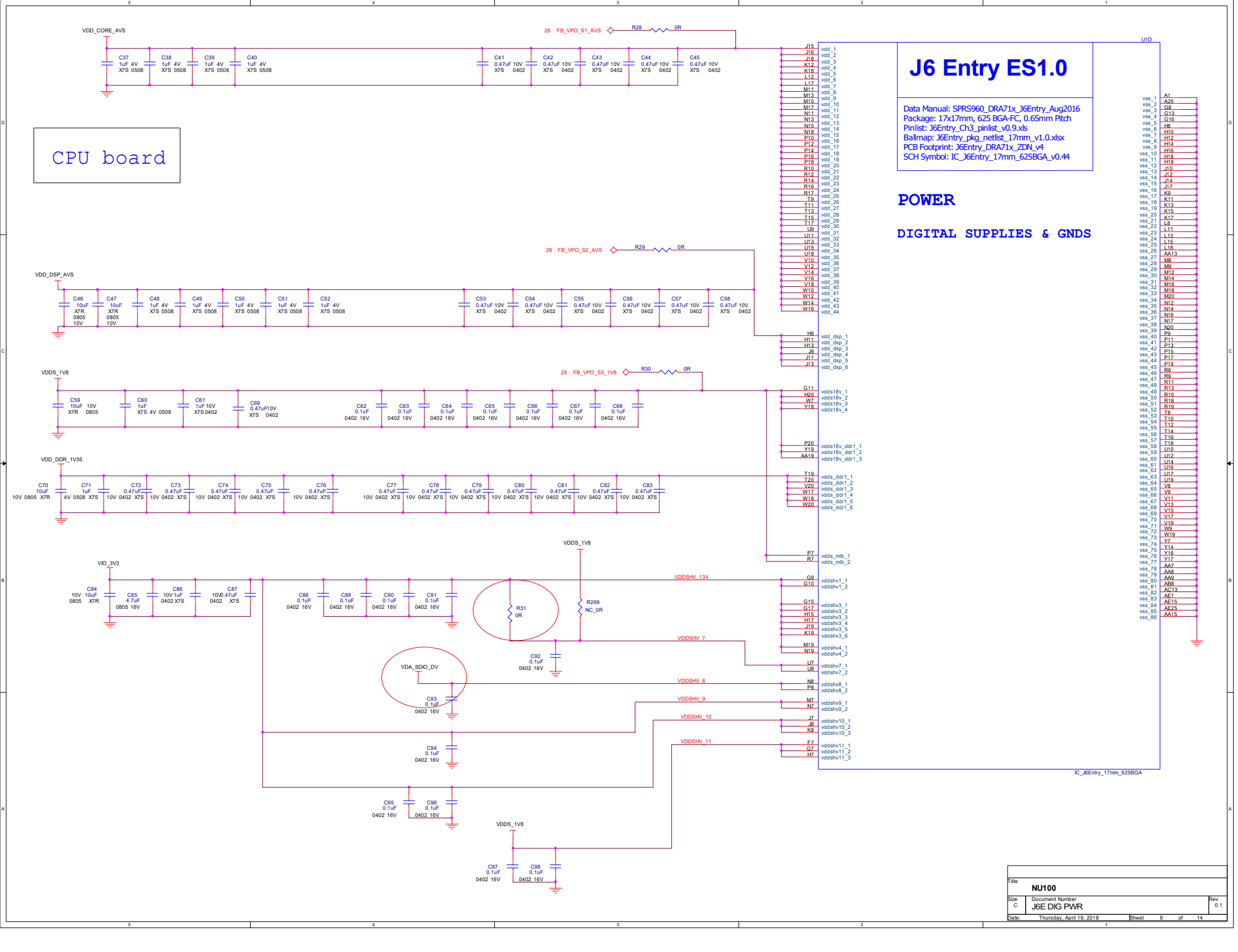
CPU board
J6 Entry ES1.0
Data Manual: SPRS960_DRA71x_J6Entry_Aug2016
Package: 17x17mm, 625 BGA-FC, 0.65mm Pitch
Pinlist: J6Entry_Ch3_pinlist_v0.9.xls
Ballmap: J6Entry_pkg_netlist_17mm_v1.0.xlsx
PCB Footprint: J6Entry_DRA71x_ZDN_v4
SCH Symbol: IC_J6Entry_17mm_625BGA_v0.44
POWER
DIGITAL SUPPLIES & GNDS
VDD_CORE_AVS
28 FB_VPO_S1_AVS
R28 0R
VDD_DSP_AVS
28 FB_VPO_S2_AVS
R29 0R
VDDS_1V8
28 FB_VPO_S3_1V8
R30 0R
VDD_DDR_1V35
VIO_3V3
VDDS_1V8
VDDSHV_134
VDDSHV_7
VDDSHV_8
VDDSHV_9
VDDSHV_10
VDDSHV_11
VDA_SDIO_DV
R31 0R
R269 NC_0R
U1D
IC_J6Entry_17mm_625BGA
Title
NU100
Size C
Document Number J6E DIG PWR
Rev 0.1
Date: Thursday, April 19, 2018
Sheet 6 of 14

CPU board

U2 — MT41K512M16HA-125 AIT:A

U3 — MT41K512M16HA-125 AIT:A

VDDR_VREFSTL

VDD_DDR_1V35

VPO_S4_DDR

Q1 NC_PMV65XP

Q2 2N7002

8 PMIC_REGEN_DDR

DR9

PL-0201 R36 FB_VPO_S4_DDR 28

Terminatoin Resistors

VTT_DDR

Terminatoin Regulator

Q3 PMV65XP

VSYS_3V3

VSW_3V3

Q4 2N7002

TPS51200DRC

U4

R228 NC_0R

TPS51200 Enable/ON input
VIH = 1.7V
VIL = 0.3V

Title	NU100
Size	C
Document Number	DDR3 MEMORY BANK 1
Rev	0.1
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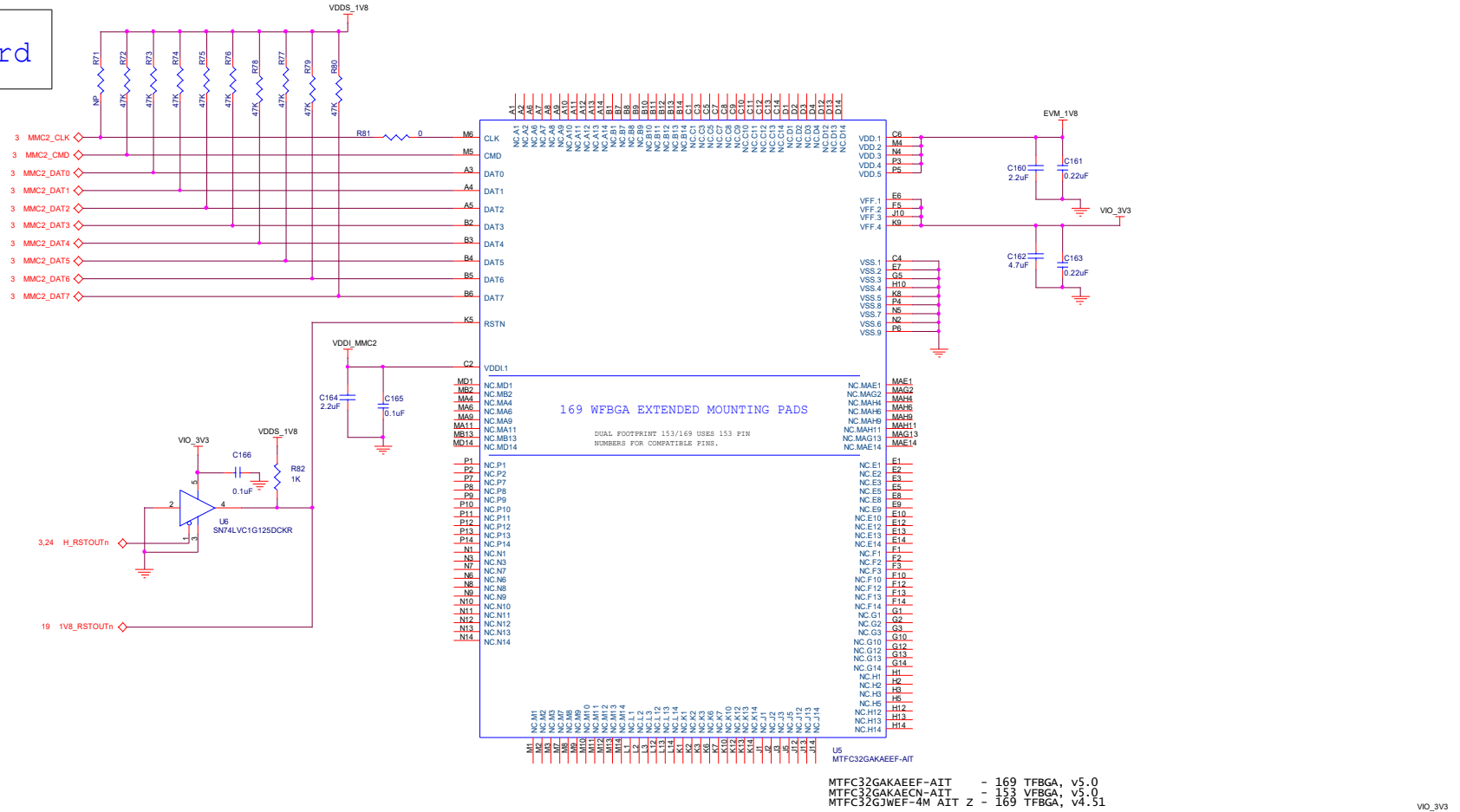
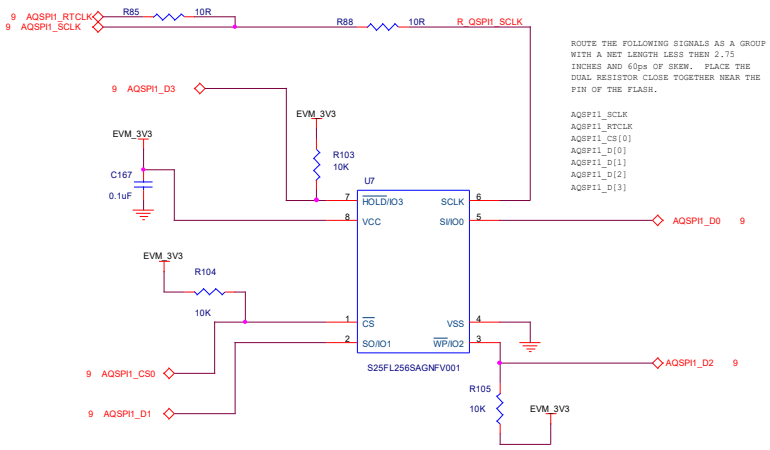
Sheet	7 of 14

CPU board

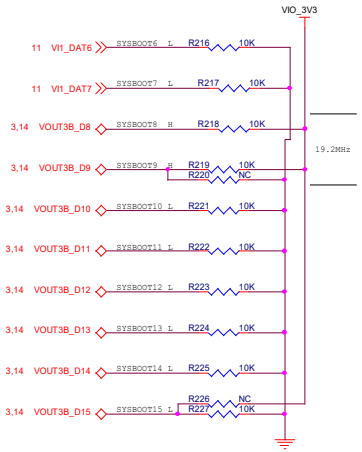


MTFC32GAKAEEF-AIT - 169 TFBGA, v5.0
MTFC32GAKAECN-AIT - 153 VFBGA, v5.0
MTFC32GJWEF-4M AIT Z - 169 TFBGA, v4.51



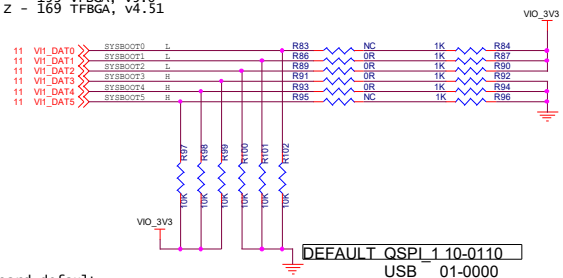
ROUTE THE FOLLOWING SIGNALS AS A GROUP WITH A NET LENGTH LESS THEN 2.75 INCHES AND 60ps OF SKEW. PLACE THE DUAL RESISTOR CLOSE TOGETHER NEAR THE PIN OF THE FLASH.

AQSPI1_SCLK
AQSPI1_RTCLK
AQSPI1_CS[0]
AQSPI1_D[0]
AQSPI1_D[1]
AQSPI1_D[2]
AQSPI1_D[3]



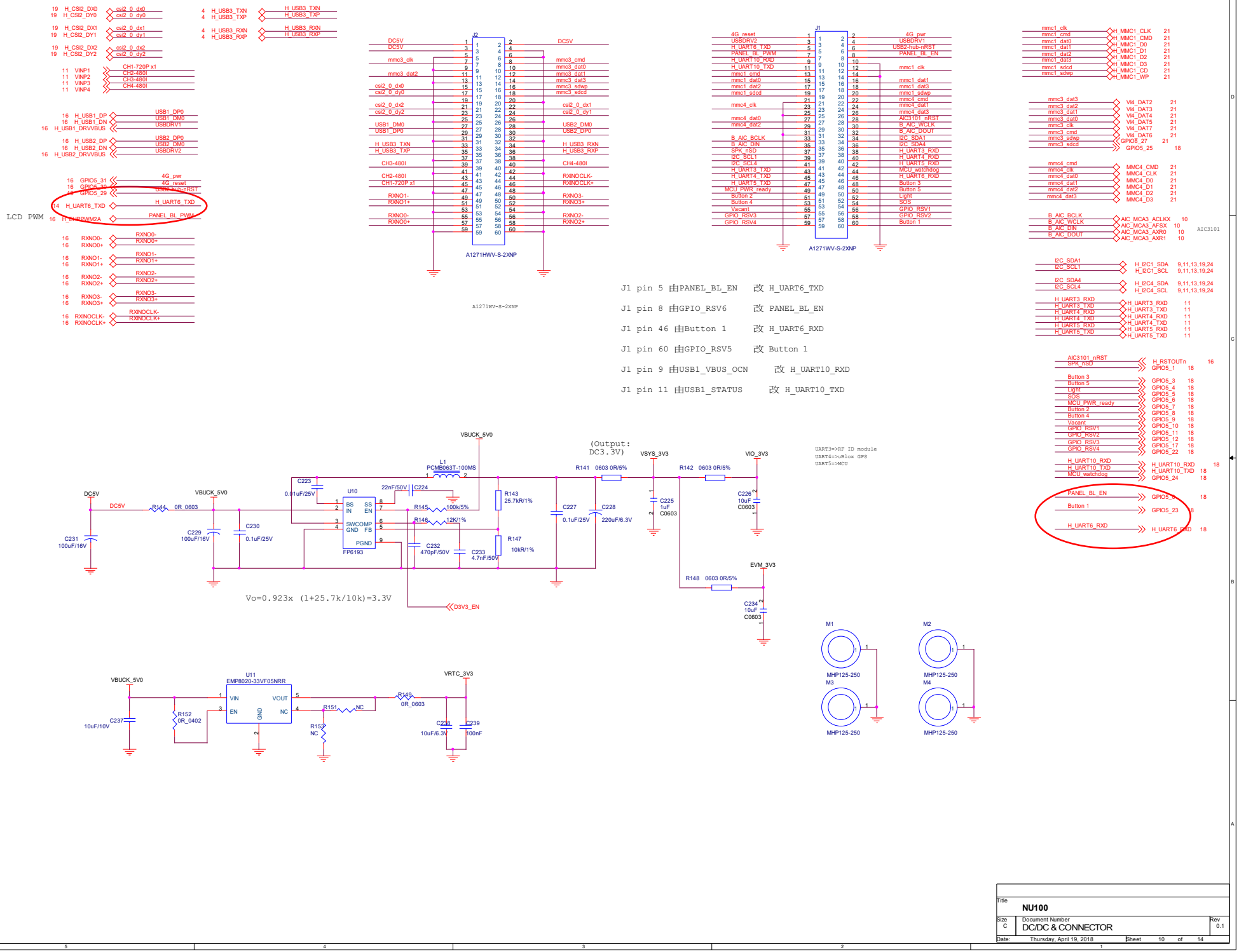
EVM board default
SYSBOOT[15:6]
1000000I 00

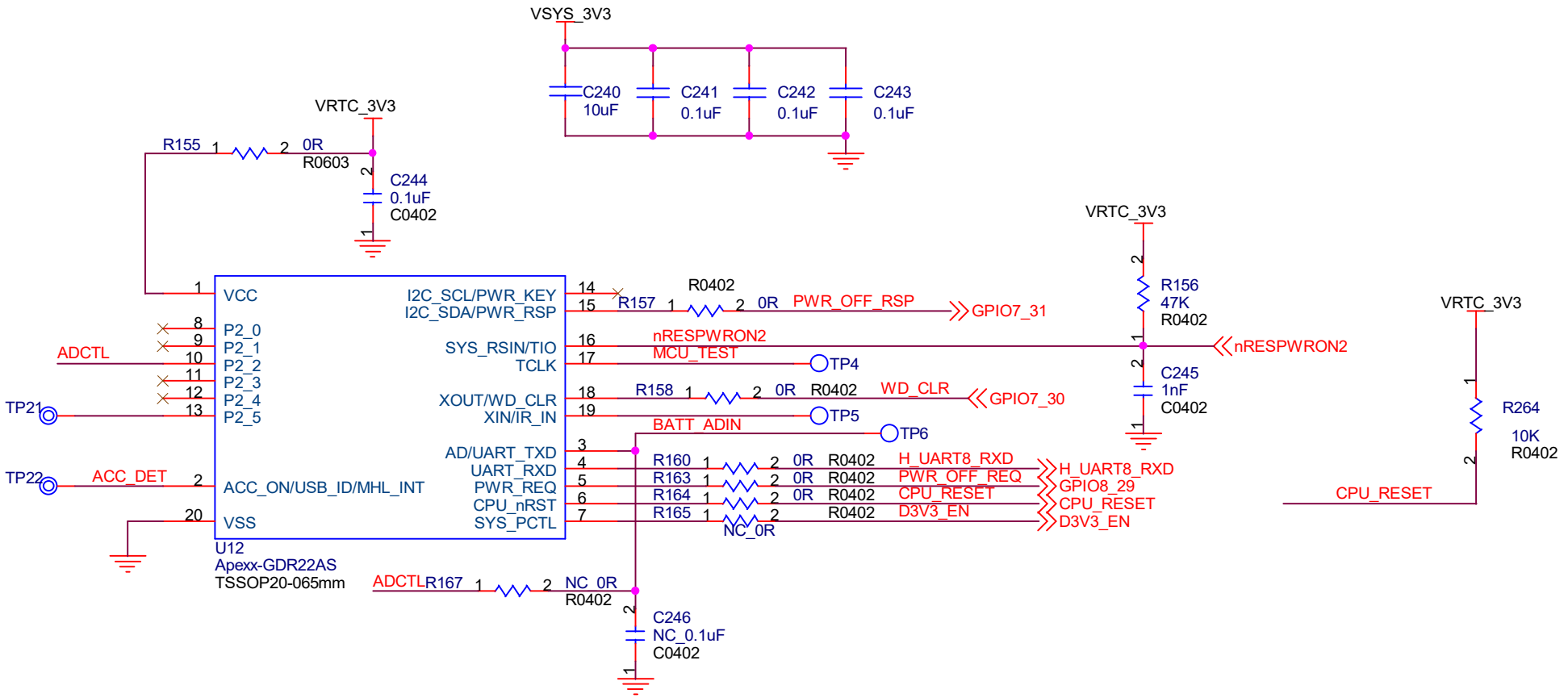
Lcard board default
SYSBOOT[15:6]
00000011 00
SYSCLK=19.2MHz
mmc2_dat[7:0] Pull-down



DEFAULT QSPI_1 10-0110
USB 01-0000
UART 01-0011
eMMC 10-0000 (USB)
eMMC 11-1000
eMMC 11-1011
(BOOT PART)

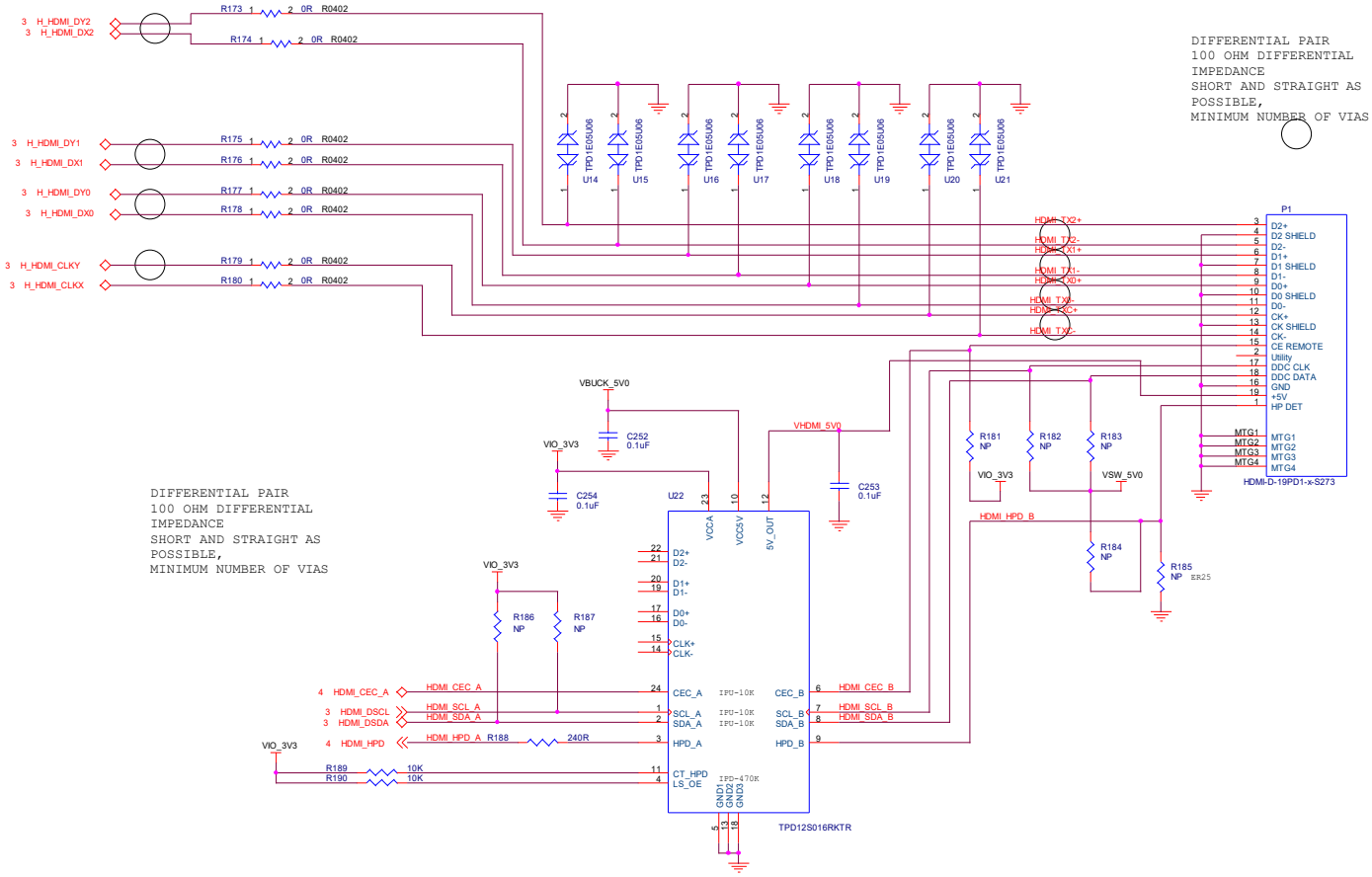
Title	NU100	
Size C	Document Number MEM eMMC	Rev 0.1
Date: Thursday, April 19, 2018	Sheet 8 of 14	


J1 pin 5 由PANEL_BL_EN 改 H_UART6_TXD
J1 pin 8 由GPIO_RSV6 改 PANEL_BL_EN
J1 pin 46 由Button 1 改 H_UART6_RXD
J1 pin 60 由GPIO_RSV5 改 Button 1
J1 pin 9 由USB1_VBUS_OCN 改 H_UART10_RXD
J1 pin 11 由USB1_STATUS 改 H_UART10_TXD
LCD PWM
A1271WV-S-2XNP
Vo=0.923x (1+25.7k/10k)=3.3V
(Output: DC3.3V)
UART3=>RF ID module
UART4=>uBlox GPS
UART5=>MCU
NU100
DC/DC & CONNECTOR
Thursday, April 19, 2018



Title	**NU100**	
Size: A	Document Number: MCU	Rev: 0.1
Date: Thursday, April 19, 2018	Sheet 11 of 14	

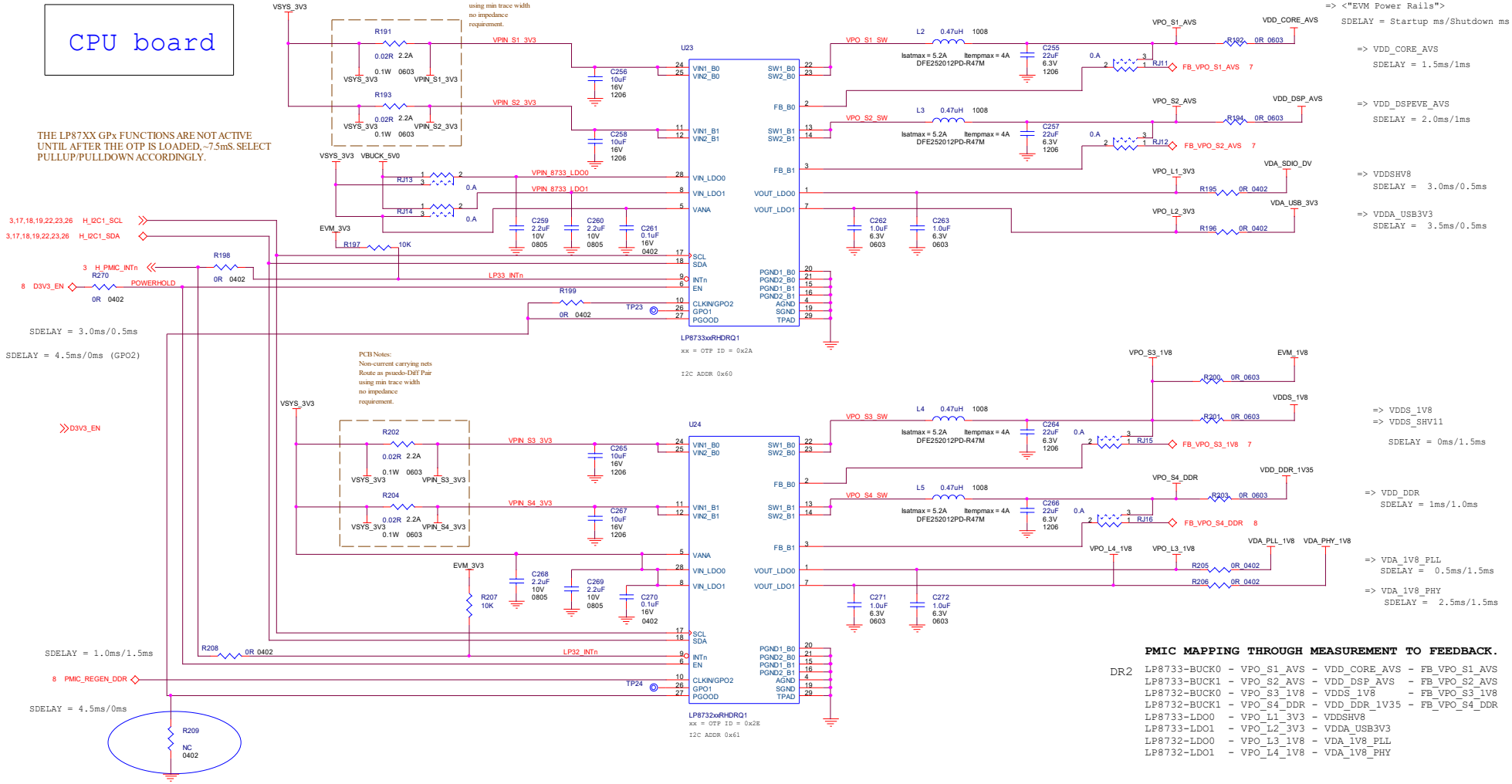
CPU board



Title	NU100		
Size C	Document Number HDMI		Rev 0.1
Date: Thursday, April 19, 2018	Sheet 12 of 14		

CPU board

THE LP87XX GPx FUNCTIONS ARE NOT ACTIVE UNTIL AFTER THE OTP IS LOADED, ~7.5mS. SELECT PULLUP/PULLDOWN ACCORDINGLY.



PMIC MAPPING THROUGH MEASUREMENT TO FEEDBACK.

DR2

```
LP8733-BUCK0 - VPO_S1_AVS - VDD_CORE_AVS - FB_VPO_S1_AVS
LP8733-BUCK1 - VPO_S2_AVS - VDD_DSP_AVS  - FB_VPO_S2_AVS
LP8732-BUCK0 - VPO_S3_1V8 - VDDS_1V8     - FB_VPO_S3_1V8
LP8732-BUCK1 - VPO_S4_DDR - VDD_DDR_1V35 - FB_VPO_S4_DDR
LP8733-LDO0  - VPO_L1_3V3 - VDDSHV8
LP8733-LDO1  - VPO_L2_3V3 - VDDA_USB3V3
LP8732-LDO0  - VPO_L3_1V8 - VDA_1V8_PLL
LP8732-LDO1  - VPO_L4_1V8 - VDA_1V8_PHY
```

Title	NU100	
Size C	Document Number PMIC	Rev 0.1
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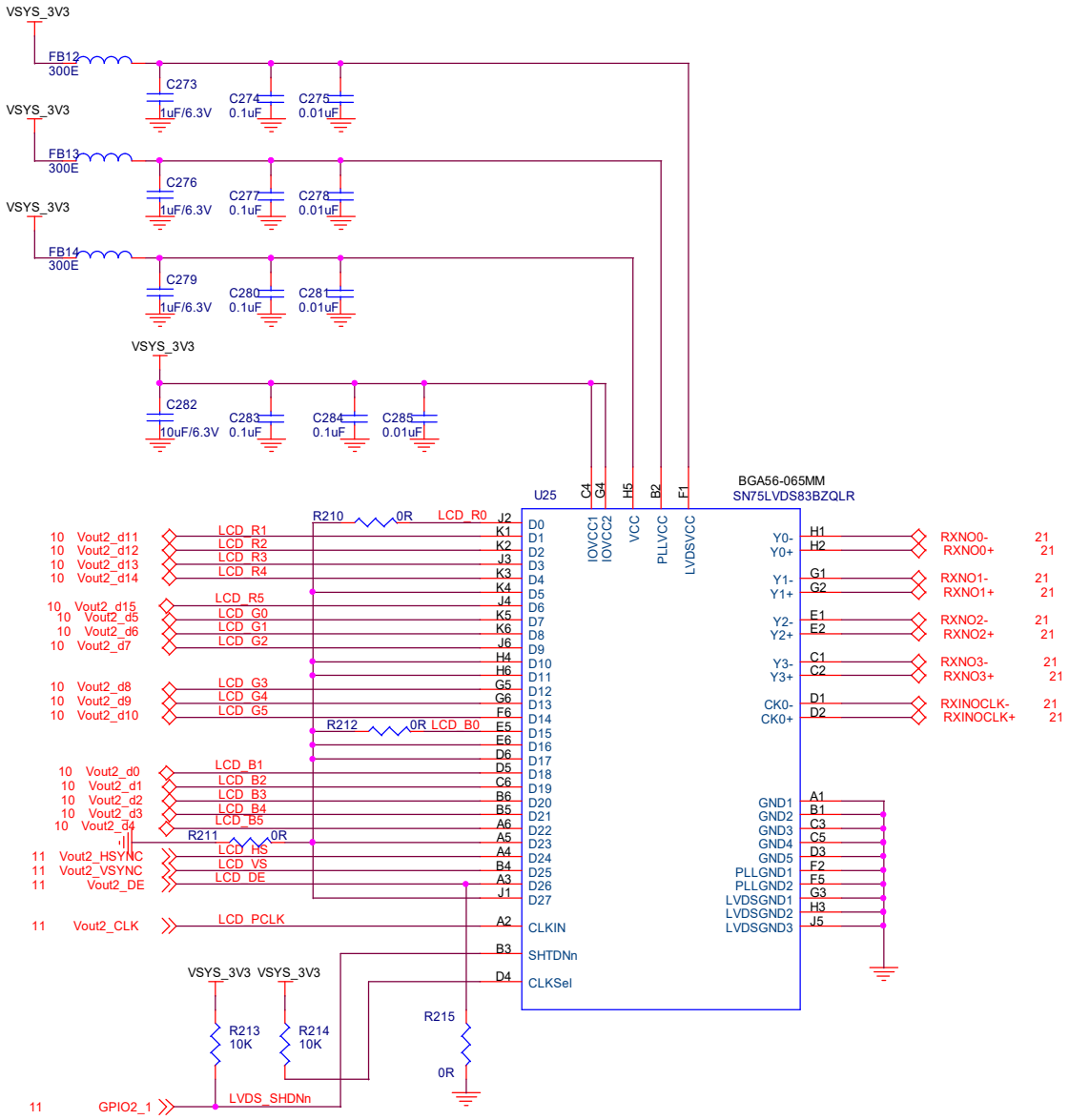

Title	NU100	
Size B	Document Number LVDS	Rev 0.1
Date: Thursday, April 19, 2018	Sheet 14 of 14	