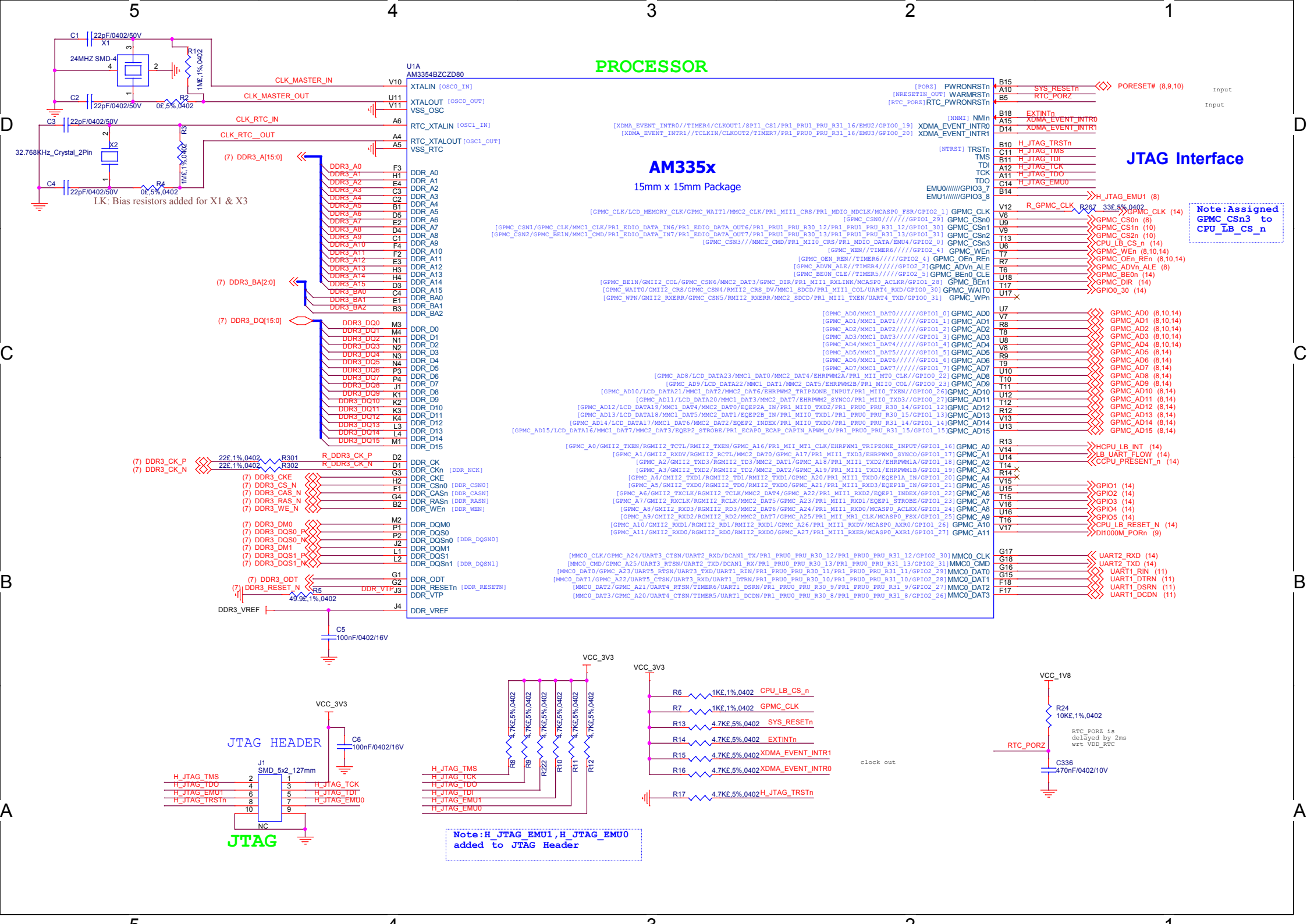
PROCESSOR
U1A
AM3354BZCZD80
AM335x
15mm x 15mm Package
JTAG Interface
JTAG HEADER
JTAG
24MHZ SMD-4
32.768KHz_Crystal_2Pin
LK: Bias resistors added for X1 & X3
CLK_MASTER_IN
CLK_MASTER_OUT
CLK_RTC_IN
CLK_RTC__OUT
(7) DDR3_A[15:0]
(7) DDR3_BA[2:0]
(7) DDR3_DQ[15:0]
(7) DDR3_CK_P
(7) DDR3_CK_N
(7) DDR3_CKE
(7) DDR3_CS_N
(7) DDR3_CAS_N
(7) DDR3_RAS_N
(7) DDR3_WE_N
(7) DDR3_DM0
(7) DDR3_DQS0_P
(7) DDR3_DQS0_N
(7) DDR3_DM1
(7) DDR3_DQS1_P
(7) DDR3_DQS1_N
(7) DDR3_ODT
(7) DDR3_RESET_N
DDR3_VREF
DDR_VTP
VCC_3V3
VCC_1V8
POREST# (8,9,10)
H_JTAG_EMU1 (8)
GPMC_CLK (14)
GPMC_CS0n (8)
GPMC_CS1n (10)
GPMC_CS2n (10)
CPU_LB_CS_n (14)
GPMC_WEn (8,10,14)
GPMC_OEn_REn (8,10,14)
GPMC_ADVn_ALE (8)
GPMC_BE0n (14)
GPMC_DIR (14)
GPIO0_30 (14)
GPMC_AD0 (8,10,14)
GPMC_AD1 (8,10,14)
GPMC_AD2 (8,10,14)
GPMC_AD3 (8,10,14)
GPMC_AD4 (8,10,14)
GPMC_AD5 (8,14)
GPMC_AD6 (8,14)
GPMC_AD7 (8,14)
GPMC_AD8 (8,14)
GPMC_AD9 (8,14)
GPMC_AD10 (8,14)
GPMC_AD11 (8,14)
GPMC_AD12 (8,14)
GPMC_AD13 (8,14)
GPMC_AD14 (8,14)
GPMC_AD15 (8,14)
HCPU_LB_INT (14)
LB_UART_FLOW (14)
CCPU_PRESENT_n (14)
GPIO1 (14)
GPIO2 (14)
GPIO3 (14)
GPIO4 (14)
GPIO5 (14)
CPU_LB_RESET_N (14)
DI1000M_PORn (9)
UART2_RXD (14)
UART2_TXD (14)
UART1_RIN (11)
UART1_DTRN (11)
UART1_DSRN (11)
UART1_DCDN (11)
Note:Assigned GPMC_CSn3 to CPU_LB_CS_n
Note:H_JTAG_EMU1,H_JTAG_EMU0 added to JTAG Header
clock out
RTC_PORZ is delayed by 2ms wrt VDD_RTC

AM335X

15mm x 15mm Package

U1B
AM3354BZCZD80

MII

PMIC_PWR_EN C6 — PMIC_POWER_EN
EXT_WAKEUP C5 — EXT_WAKEUP

B6 AIN0
C7 AIN1
B7 AIN2
A7 AIN3
C8 AIN4
B8 AIN5
A8 AIN6
C9 AIN7

R18 0E,5%,0402 — VREFP B9 — VREFP
A9 — VREFN

R268 33E,5%,0402 — R_SPI_SCLK A17 — SPI0_SCLK [SPI0_SCLK/UART2_RXD/I2C2_SDA/EHRPWM0A/PR1_UART0_CTS_N/PR1_EDIO_SOF/EMU2/GPIO0_2]
(14) SPI_SCLK
(14) SPI_D0/MISO — B17 — SPIO_D0 [SPIO_D0/UART2_TXD/I2C2_SCL/EHRPWM0B/PR1_UART0_RTS_N/PR1_EDIO_LATCH_IN/EMU3/GPIO0_3]
(14) SPI_D1/MOSI — B16 — SPIO_D1 [SPIO_D1/MMC1_SDWP/I2C1_SDA/EHRPWM0_TRIPZONE_INPUT/PR1_UART0_RXD/PR1_EDIO_DATA_IN0/PR1_EDIO_DATA_OUT0/GPIO0_4]
(14) SPI_CS_N — A16 — SPIO_CS0 [SPIO_CS0/MMC2_SDWP/I2C1_SCL/EHRPWM0_SYNCI/PR1_UART0_TXD/PR1_EDIO_DATA_IN1/PR1_EDIO_DATA_OUT1/GPIO0_5]
C15 — SPIO_CS1 [SPIO_CS1/UART3_RXD/ECAP1_IN_PWM1_OUT/MMC0_POW/XDMA_EVENT_INTR2/MMC0_SDCD/EMU4/GPIO0_6]

UART0 Debug Port
(9) UART0_TXD — E16 — UART0_TXD [UART0_TXD/SPI1_CS1/DCAN0_RX/I2C2_SCL/ECAP1_IN_PWM1_OUT/PR1_PRU1_PRU_R30_15/PR1_PRU1_PRU_R31_15/GPIO1_11]
(9) UART0_RXD — E15 — UART0_RXD [UART0_RXD/SPI1_CS0/DCAN0_TX/I2C2_SDA/ECAP2_IN_PWM2_OUT/PR1_PRU1_PRU_R30_14/PR1_PRU1_PRU_R31_14/GPIO1_10]
E18 — UART0_CTSn [UART0_CTSN/UART4_RXD/DCAN1_TX/I2C1_SDA/SPI1_D0/TIMER7/PR1_EDC_SYNC0_OUT/GPIO1_8]
E17 — UART0_RTSn [UART0_RTSN/UART4_TXD/DCAN1_RX/I2C1_SCL/SPI1_D1/SPI1_CS0/PR1_EDC_SYNC1_OUT/GPIO1_9]

(11) UART1_TX — D15 — UART1_TXD [UART1_TXD/MMC2_SDWP/DCAN1_RX/I2C1_SCL//PR1_UART0_TXD/PR1_PRU0_PRU_R31_16/GPIO0_15]
(11) UART1_BRX — D16 — UART1_RXD [UART1_RXD/MMC1_SDWP/DCAN1_TX/I2C1_SDA//PR1_UART0_RXD/PR1_PRU1_PRU_R31_16/GPIO0_14]
(11) UART1_BCTS_N — D18 — UART1_CTSn [UART1_CTSN/TIMER6/DCAN0_TX/I2C2_SDA/SPI1_CS0/PR1_UART0_CTS_N/PR1_EDC_LATCH0_IN/GPIO0_12]
(11) UART1_RTS_N — D17 — UART1_RTSn [UART1_RTSN/TIMER5/DCAN0_RX/I2C2_SCL/SPI1_CS1/PR1_UART0_RTS_N/PR1_EDC_LATCH1_IN/GPIO0_13]

I2C
I2C0_SCL R268 33E,5%,0402 R_I2C0_SCL C16 — I2C0_SCL [I2C0_SCL/TIMER7/UART2_RTSN/ECAP1_IN_PWM1_OUT///GPIO3_6]
I2C0_SDA R269 C17 — I2C0_SDA [I2C0_SDA/TIMER4/UART2_CTSN/ECAP2_IN_PWM2_OUT///GPIO3_5]
Route as differential Pair

USB Interface
(9) USB0_DP — N17 — USB0_DP
(9) USB0_DM — N18 — USB0_DM
USB0_CE M15 — USB0_CE
0E,5%,0402 R19 — USB0_ID P16 — USB0_ID
USB0_DRVVBUS F16 — USB0_DRVVBUS [USB0_DRVVBUS//////GPIO0_18]
VCC_5V — 1.5KE,1%,0402 R20 — USB0_VBUS P15 — USB0_VBUS

USB1_DP R17 — USB1_DP
USB1_DM R18 — USB1_DM
USB1_CE P18 — USB1_CE
USB1_ID P17 — USB1_ID
F15 — USB1_DRVVBUS [USB1_DRVVBUS//////GPIO3_13]
USB1_VBUS T18 — USB1_VBUS

(14) CCPU_LB_INT — C18 — ECAP0_IN_PWM0_OUT [ECAP0_IN_PWM0_OUT/UART3_TXD/SPI1_CS1/PR1_ECAP0_ECAP_CAPIN_APWM_O/SPI1_SCLK/MMC0_SDWP/XDMA_EVENT_INTR2/GPIO0_7]

[GMII1_TXCLK/UART2_RXD/RGMII1_TCLK/MMC0_DAT7/MMC1_DAT0/UART1_DCDN/MCASP0_ACLKX/GPIO3_9] MII1_TXCLK — K18 — MII1_TX_CLK (13)
[GMII1_TXD0/RMII1_TXD0/RGMII1_TD0/MCASP1_AXR2/MCASP1_ACLKR/EQEP0B_IN/MMC1_CLK/GPIO0_28] MII1_TXD0 — K17 — MII1_TXD0 (13)
[GMII1_TXD1/RMII1_TXD1/RGMII1_TD1/MCASP1_FSR/MCASP1_AXR1/EQEP0A_IN/MMC1_CMD/GPIO0_21] MII1_TXD1 — K16 — MII1_TXD1 (13)
[GMII1_TXD2/DCAN0_RX/RGMII1_TD2/UART4_TXD/MCASP1_AXR0/MMC2_DAT2/MCASP0_AHCLKX/GPIO0_17] MII1_TXD2 — K15 — MII1_TXD2 (13)
[GMII1_TXD3/DCAN0_TX/RGMII1_TD3/UART4_RXD/MCASP1_FSX/MMC2_DAT1/MCASP0_FSR/GPIO0_16] MII1_TXD3 — J18 — MII1_TXD3 (13)
[GMII1_TXEN/RMII1_TXEN/RGMII1_TCTL/TIMER4/MCASP1_AXR0/EQEP0_INDEX/MMC2_CMD/GPIO3_3] MII1_TXEN — J16 — MII1_TX_EN (13)
[GMII1_CRS/RMII1_CRS_DV/SPI1_D0/I2C1_SDA/MCASP1_ACLKX/UART5_CTSN/UART2_RXD/GPIO3_1] MII1_CRS — H17 — MII1_CRS (13)
[GMII1_COL/RMII2_REFCLK/SPI1_SCLK/UART5_RXD/MCASP1_AXR2/MMC2_DAT3/MCASP0_AXR2/GPIO3_0] MII1_COL — H16 — MII1_COL (13)

[GMII1_RXCLK/UART2_TXD/RGMII1_RCLK/MMC0_DAT6/MMC1_DAT1/UART1_DSRN/MCASP0_FSX/GPIO3_10] MII1_RXCLK — L18 — MII1_RX_CLK (13)
[GMII1_RXD0/RMII1_RXD0/RGMII1_RD0/MCASP1_AHCLKX/MCASP1_AHCLKR/MCASP1_ACLKR/MCASP0_AXR3/GPIO2_21] MII1_RXD0 — M16 — MII1_RXD0 (13)
[GMII1_RXD1/RMII1_RXD1/RGMII1_RD1/MCASP1_AXR3/MCASP1_FSR/EQEP0_STROBE/MMC2_CLK/GPIO2_20] MII1_RXD1 — L15 — MII1_RXD1 (13)
[GMII1_RXD2/UART3_TXD/RGMII1_RD2/MMC0_DAT4/MMC1_DAT3/UART1_RIN/MCASP0_AXR1/GPIO2_19] MII1_RXD2 — L16 — MII1_RXD2 (13)
[GMII1_RXD3/UART3_RXD/RGMII1_RD3/MMC0_DAT5/MMC1_DAT2/UART1_DTRN/MCASP0_AXR0/GPIO2_18] MII1_RXD3 — L17 — MII1_RXD3 (13)
[GMII1_RXERR/RMII1_RXERR/SPI1_D1/I2C1_SCL/MCASP1_FSX/UART5_RTSN/UART2_TXD/GPIO3_2] MII1_RXERR — J15 — MII1_RXER (13)
[GMII1_RXDV/LCD_MEMORY_CLK/RGMII1_RCTL/UART5_TXD/MCASP1_ACLKX/MMC2_DAT0/MCASP0_ACLKR/GPIO3_4] MII1_RXDV — J17 — MII1_RXDV (13)

[RMII1_REFCLK/XDMA_EVENT_INTR2/SPI1_CS0/UART5_TXD/MCASP1_AXR3/MMC0_POW/MCASP1_AHCLKX/GPIO0_29] MII1_REFCLK — H18 — PHY_RST (13)
[MDIO_CLK/TIMER5/UART5_TXD/UART3_RTSN/MMC0_SDWP/MMC1_CLK/MMC2_CLK/GPIO0_1] MDIO_CLK — M18 — R_MII1_MDC
[MDIO_DATA/TIMER6/UART5_RXD/UART3_CTSN/MMC0_SDCD/MMC1_CMD/MMC2_CMD/GPIO0_0] MDIO_DATA — M17 — MII1_MDIO (13)

[LCD_DATA0/GPMC_A0/PR1_MII_MT0_CLK/EHRPWM2A//PR1_PRU1_PRU_R30_0/PR1_PRU1_PRU_R31_0/GPIO2_6] LCD_DATA0 — R1 — LCD_DATA0 (8)
[LCD_DATA1/GPMC_A1/PR1_MII0_TXEN/EHRPWM2B//PR1_PRU1_PRU_R30_1/PR1_PRU1_PRU_R31_1/GPIO2_7] LCD_DATA1 — R2 — GPMC_A16 (8)
[LCD_DATA2/GPMC_A2/PR1_MII0_TXD3/EHRPWM2_TRIPZONE_INPUT//PR1_PRU1_PRU_R30_2/PR1_PRU1_PRU_R31_2/GPIO2_8] LCD_DATA2 — R3 — GPMC_A17 (8)
[LCD_DATA3/GPMC_A3/PR1_MII0_TXD2/EHRPWM2_SYNCI_O//PR1_PRU1_PRU_R30_3/PR1_PRU1_PRU_R31_3/GPIO2_9] LCD_DATA3 — R4 — GPMC_A18 (8)
[LCD_DATA4/GPMC_A4/PR1_MII0_TXD1/EQEP2A_IN//PR1_PRU1_PRU_R30_4/PR1_PRU1_PRU_R31_4/GPIO2_10] LCD_DATA4 — T1 — GPMC_A19 (8)
[LCD_DATA5/GPMC_A5/PR1_MII0_TXD0/EQEP2B_IN//PR1_PRU1_PRU_R30_5/PR1_PRU1_PRU_R31_5/GPIO2_11] LCD_DATA5 — T2 — GPMC_A20 (8)
[LCD_DATA6/GPMC_A6/Pr1_EDIO_DATA_IN6/EQEP2_INDEX/PR1_EDIO_DATA_OUT6/PR1_PRU1_PRU_R30_6/PR1_PRU1_PRU_R31_6/GPIO2_12] LCD_DATA6 — T3 — GPMC_A21 (8)
[LCD_DATA7/GPMC_A7/PR1_EDIO_DATA_IN7/EQEP2_STROBE/PR1_EDIO_DATA_OUT7/PR1_PRU1_PRU_R30_7/PR1_PRU1_PRU_R31_7/GPIO2_13] LCD_DATA7 — T4 — GPMC_A22 (8)
[LCD_DATA8/GPMC_A12/EHRPWM1_TRIPZONE_INPUT/MCASP0_ACLKX/UART5_TXD/PR1_MII0_RXD3/UART2_CTSN/GPIO2_14] LCD_DATA8 — U1 — LCD_DATA8 (8)
[LCD_DATA9/GPMC_A13/EHRPWM1_SYNCO/MCASP0_FSX/UART5_RXD/PR1_MII0_RXD2/UART2_RTSN/GPIO2_15] LCD_DATA9 — U2 — LCD_DATA9 (8)
[LCD_DATA10/GPMC_A14/EHRPWM1A/MCASP0_AXR0//PR1_MII0_RXD1/UART3_CTSN/GPIO2_16] LCD_DATA10 — U3 — LCD_DATA10 (8)
[LCD_DATA11/GPMC_A15/EHRPWM1B/MCASP0_AHCLKR/MCASP0_AXR2/PR1_MII0_RXD0/UART3_RTSN/GPIO2_17] LCD_DATA11 — U4 — LCD_DATA11 (8)
[LCD_DATA12/GPMC_A16/EQEP1A_IN/MCASP0_ACLKR/MCASP0_AXR2/PR1_MII0_RXLINK/UART4_CTSN/GPIO0_8] CD_DATA12 — V2 — LCD_DATA12 (8)
[LCD_DATA13/GPMC_A17/EQEP1B_IN/MCASP0_FSR/MCASP0_AXR3/PR1_MII0_RXER/UART4_RTSN/GPIO0_9] LCD_DATA13 — V3 — LCD_DATA13 (8)
[LCD_DATA14/GPMC_A18/EQEP1_INDEX/MCASP0_AXR1/UART5_RXD/PR1_MII_MR0_CLK/UART5_CTSN/GPIO0_10] LCD_DATA14 — V4 — LCD_DATA14 (8)
[LCD_DATA15/GPMC_A19/EQEP1_STROBE/MCASP0_AHCLKX/MCASP0_AXR3/PR1_MII0_RXDV/UART5_RTSN/GPIO0_11] LCD_DATA15 — T5 — LCD_DATA15 (8)

[LCD_PCLK/GPMC_A10/PR1_MII0_CRS/PR1_EDIO_DATA_IN4/PR1_EDIO_DATA_OUT4/PR1_PRU1_PRU_R30_10/PR1_PRU1_PRU_R31_10/GPIO2_24] LCD_PCLK — V5
[LCD_VSYNC/GPMC_A8//PR1_EDIO_DATA_IN2/PR1_EDIO_DATA_OUT2/PR1_PRU1_PRU_R30_8/PR1_PRU1_PRU_R31_8/GPIO2_22] LCD_VSYNC — U5
[LCD_HSYNC/GPMC_A9//PR1_EDIO_DATA_IN3/PR1_EDIO_DATA_OUT3/PR1_PRU1_PRU_R30_9/PR1_PRU1_PRU_R31_9/GPIO2_23] LCD_HSYNC — R5 — GPMC_A23 (8)
[LCD_AC_BIAS_EN/GPMC_A11/PR1_MII1_CRS/PR1_EDIO_DATA_IN5/PR1_EDIO_DATA_OUT5/PR1_PRU1_PRU_R30_11/PR1_PRU1_PRU_R31_11/GPIO2_25] LCD_AC_BIAS_EN — R6 — GPIO7 (14)

[MCASP0_AHCLKX/EQEP0_STROBE/MCASP0_AXR3/MCASP1_AXR1/EMU4/PR1_PRU0_PRU_R30_7/PR1_PRU0_PRU_R31_7/GPIO3_21] MCASP0_AHCLKX — A14 — USER_RESET (9)
[MCASP0_ACLKX/EHRPWM0A//SPI1_SCLK/MMC0_SDCD/PR1_PRU0_PRU_R30_0/PR1_PRU0_PRU_R31_0/GPIO3_14] MCASP0_ACLKX — A13 — BUZ (9)
[MCASP0_FSX/EHRPWM0B//SPI1_D0/MMC1_SDCD/PR1_PRU0_PRU_R30_1/PR1_PRU0_PRU_R31_1/GPIO3_15] MCASP0_FSX — B13 — RTC_REST# (10)
[MCASP0_AXR0/EHRPWM0_TRIPZONE_INPUT//SPI1_D1/MMC2_SDCD/PR1_PRU0_PRU_R30_2/PR1_PRU0_PRU_R31_2/GPIO3_16] MCASP0_AXR0 — D12 — RTC_INT (10)
[MCASP0_AHCLKR/EHRPWM0_SYNCI_O/MCASP0_AXR2/SPI1_CS0/ECAP2_IN_PWM2_OUT/PR1_PRU0_PRU_R30_3/PR1_PRU0_PRU_R31_3/GPIO3_17] MCASP0_AHCLKR — C12
[MCASP0_ACLKR/EQEP0A_IN/MCASP0_AXR2/MCASP1_ACLKX/MMC0_SDWP/PR1_PRU0_PRU_R30_4/PR1_PRU0_PRU_R31_4/GPIO3_18] MCASP0_ACLKR — B12 — RUN_LED# (11)
[MCASP0_FSR/EQEP0B_IN/MCASP0_AXR3/MCASP1_FSX/EMU2/PR1_PRU0_PRU_R30_5/PR1_PRU0_PRU_R31_5/GPIO3_19] MCASP0_FSR — C13 — CPU_WDT_CLR (10)
[MCASP0_AXR1/EQEP0_INDEX//MCASP1_AXR0/EMU3/PR1_PRU0_PRU_R30_6/PR1_PRU0_PRU_R31_6/GPIO3_20] MCASP0_AXR1 — D13 — SW_RESET# (10,14)

EEPROM

U2
24LC64-I/SN

VCC_3V3
C7 100nF/0402/16V

8	VCC	A0	1
7	WP	A1	2
6	SCL	A2	3
5	SDA	GND	4

I2C0_SCL
I2C0_SDA

(10) I2C0_SCL — I2C0_SCL — 4.7KE,5%,0402 — R21
(10) I2C0_SDA — I2C0_SDA — 4.7KE,5%,0402 — R22 — VCC_3V3

VCC_3V3
Place Close to AM335x — R272 4.7KE,5%,0402
MII1_MDIO
R_MII1_MDC — 33E,5%,0402 R271 — MII1_MDC (13)
Place Close to AM335x