

MCASP1_AXR1/PR2_MII_MT0_CLK
MCASP1_AXR8/PR2_MII0_TXEN

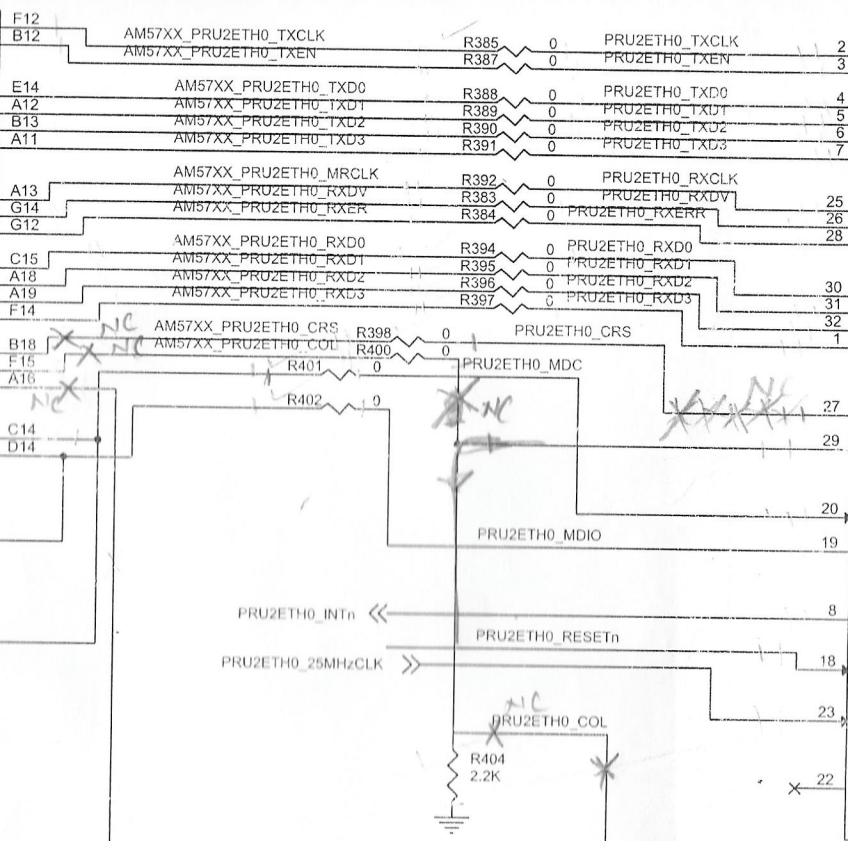
MCASP1_AXR12/PR2_MII0_TXD0
MCASP1_AXR11/PR2_MII0_TXD1
MCASP1_AXR10/PR2_MII0_TXD2
MCASP1_AXR9/PR2_MII0_TXD3

CASP1_AXR13/PR2_MII_MR0_CLK
MCASP1_AXR14/PR2_MII0_RXDV
MCASP1_AXR0/PR2_MII0_RXER

MCASP2_AXR2/PR2_MII0_RXD0
MCASP2_FSX/PR2_MII0_RXD1
MCASP2_ACLKX/PR2_MII0_RXD2
MCASP1_AXR15/PR2_MII0_RXD3

MCASP3_ACLKX/PR2_MII0_CRS
MCASP3_FSX/PR2_MII0_COL
MCASP2_AXR3/PR2_MII0_RXLINK

ASP1_ACLKX/PR2_MDIO_MDCLK
MCASP1_FSX/PR2_MDIO_DATA



U42

TX_CLK
TX_EN

TXD_0
TXD_1
TXD_2
TXD_3

RX_CLK
RX_DV
RX_ERR

RXD_0
RXD_1
RXD_2
RXD_3

CRS
COL

MDC
MDIO

PWRDNn/INTn

RESET_N

X1
XO

Note: MDIO Address =