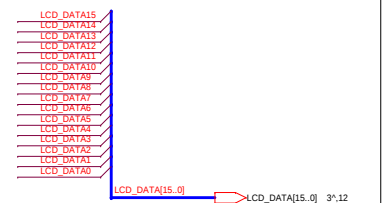
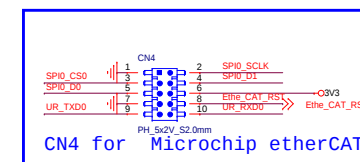
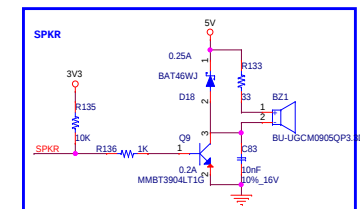
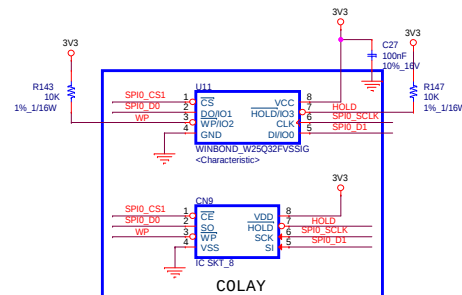




LCD_DATA[15:0] terminals are respectively SYSBOOT[15:0] inputs, latched on the rising edge of PWRONRSTn.

GEMAC_CPSW/RMII1 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCZ BALL [4]
rmii1_crs_dv	RMII Carrier Sense / Data Valid	I	H17
rmii1_refclk	RMII Reference Clock	I/O	H18
rmii1_rxd0	RMII Receive Data bit 0	I	M16
rmii1_rxd1	RMII Receive Data bit 1	I	L15
rmii1_rxer	RMII Receive Data Error	I	J15
rmii1_txd0	RMII Transmit Data bit 0	O	K17
rmii1_txd1	RMII Transmit Data bit 1	O	K16
rmii1_txen	RMII Transmit Enable	O	J16



GEMAC_CPSW/RMII2 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCZ BALL [4]
rmii2_crs_dv	RMII Carrier Sense / Data Valid	I	T13, T17
rmii2_refclk	RMII Reference Clock	I/O	H16
rmii2_rxd0	RMII Receive Data bit 0	I	V17
rmii2_rxd1	RMII Receive Data bit 1	I	T16
rmii2_rxer	RMII Receive Data Error	I	U17
rmii2_txd0	RMII Transmit Data bit 0	O	V15
rmii2_txd1	RMII Transmit Data bit 1	O	R14
rmii2_txen	RMII Transmit Enable	O	R13



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