Designing With the THS1206 High-Speed Data Converter

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ABSTRACT

This application report is intended as a guide in the use of the digital and analog portions of the THS1206 A/D converter. On the digital portion, it discusses the main timing features to explain the requirements for initialization and operation. Two interface examples are presented where the THS1206 is connected to digital signal processors TMS320C54x and TMS320C6201. On the analog portion, it offers a discussion of the options to drive the THS1206 analog input. The system layout considerations presented will help achieve optimum system performance.

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1 Introduction

The THS1206 is a low-power, 12-bit, 6-MSPS analog-to-digital converter (ADC). Its main features include four analog inputs, which are switched from sampling to hold mode simultaneously, fast speed, high resolution, and high data throughput. These features make the THS1206 very attractive in radar, imaging, high-speed acquisition, communications, and control applications. The THS1206, with its programmable interface, is designed to be compatible with multiple processors on the market. A fast data throughput to the connected processor is achieved with an integrated FIFO.

2 THS1206 Block Diagram

Figure 1 shows the THS1206 block diagram. The analog-to-digital converter (ADC) is built as a multistage pipelined architecture using output error correction logic to assure code integrity over the full operating temperature range. The ADC has 12 bits of resolution and a maximum conversion rate up to 6 MSPS (megasamples per second). The main feature of the analog portion of the THS1206 is its four analog input stages, which are simultaneously switched from sampling to hold mode. These stages can be selected individually and configured as single-ended, as differential inputs, or as a combination of both. This feature makes the device attractive for use in control applications as well as in conversion of I/Q-modulated signals. The phase relation between the analog inputs is important in these applications. An internal reference voltage (1.5 V or 3.5 V) is provided to reduce the amount of external components. However, an external-reference voltage can also be chosen to match the dc-accuracy of the application. The common-mode voltage of the internal reference is available at REFOUT. If this output is used as a system reference signal, it can be utilized to bias single-supply operational amplifiers, or to set the common-mode voltage at the output of a transformer for use in the analog input path.

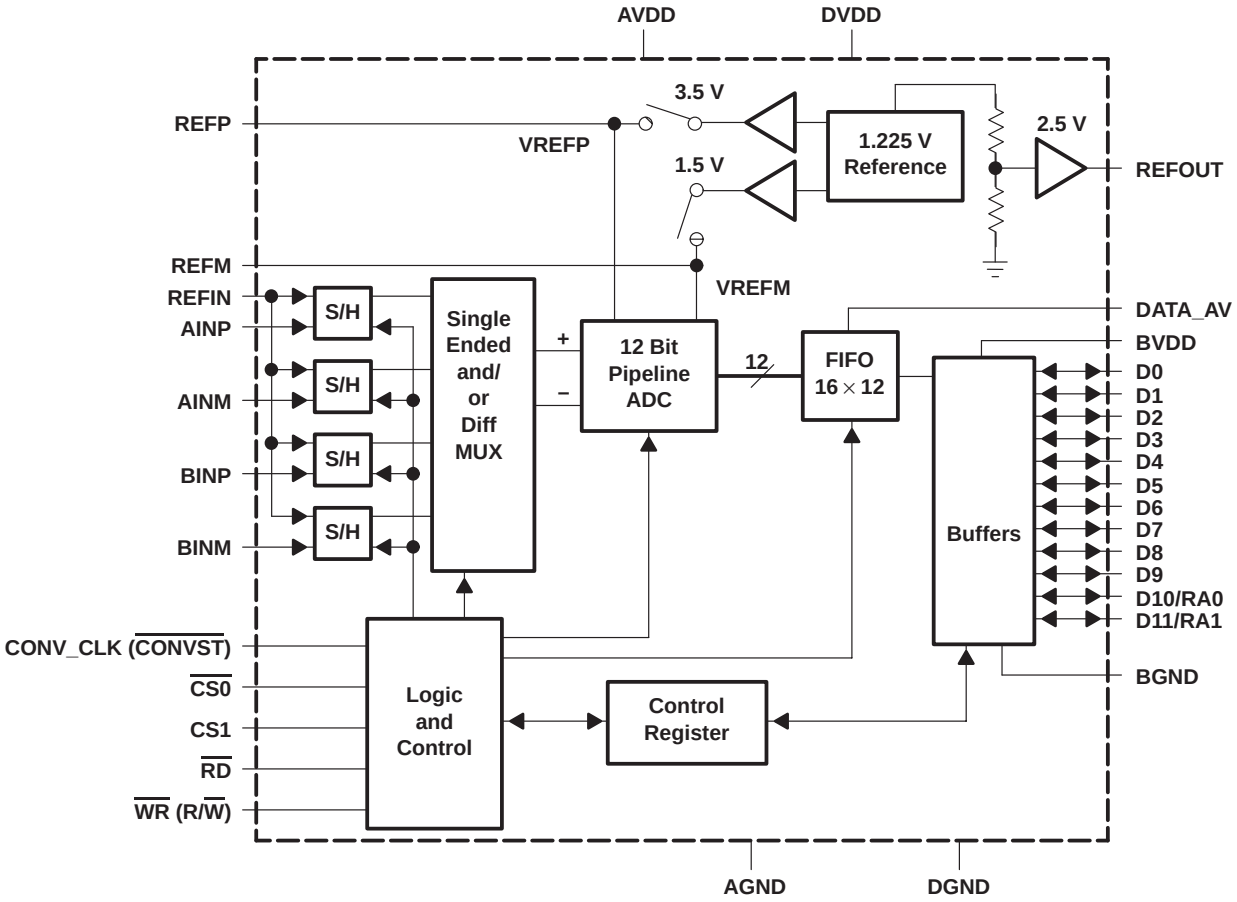

Figure 1. THS1206 Block Diagram

Another important feature of the THS1206 is its 16-word 12-bit FIFO. The FIFO takes the load off the processor connected to the ADC. Data can be transferred in bust mode, greatly improving the data throughput to the processor. The THS1206 interface to the processor is very flexible and can be configured, offering the possibility of glueless interface to modern processors. The digital conversion result is provided in parallel data format via data bus pins D0 – D11.

Two different conversion modes can be selected: single and continuous. In the single-conversion mode, a single simultaneous conversion of up to four analog input channels can be initiated by the single-conversion start signal ($\overline{\text{CONVST}}$). The conversion clock in the single-conversion mode is generated internally using a clock oscillator circuit. The single-conversion mode is specifically used in control applications. In the continuous-conversion mode, an external clock signal is applied to the CONV_CLK input of the THS1206. The internal clock oscillator is switched off in this mode. The continuous-conversion mode is specifically used in applications where a block of data must be converted from analog to digital format, for example when a window of 2048 words is used in a fast fourier transformation (FFT). Two internal control registers are used to configure the conversion modes of the THS1206.

3 Reset and Initialization

The THS1206 contains two internal control registers (control register 0 and 1). These registers are required to configure the THS1206 to the desired mode and to reset the device. The THS1206 should be reset at the beginning of initialization. Reset is performed by writing 0x401h to control register 1. Control registers 0 and 1 are 10-bits wide and can be accessed via the THS1206 parallel data bus D0 to D11. Tables 1 and 2 show the individual bits of control registers 0 and 1. The THS1206 data sheet presents a description of each bit.

Table 1. Control Register 0 (CR0)

Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TEST1	TEST0	SCAN	DIFF1	DIFF0	CHSEL1	CHSEL0	PD	MODE	VREF

Table 2. Control Register 1 (CR1)

Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBACK	OFFSET	BIN/2s	R/W	DATA_P	DATA_T	TRIG1	TRIG0	OVFL/FRST	RESET

Upper bits D10 and D11 are used for the control register address, whereas the control register value is contained in data bits D0 to D9 during the write process. Table 3 shows the control register addressing.

Table 3. Control Register Addressing

D0 – D9	D10/RA0	D11/RA1	ADDRESSED CONTROL REGISTER
Desired register value	0	0	Control Register 0 (CR0)
Desired register value	1	0	Control Register 1 (CR1)

Data bit D11/RA1 is reserved and should always be zero.

The THS1206 should be initialized in the following sequence:

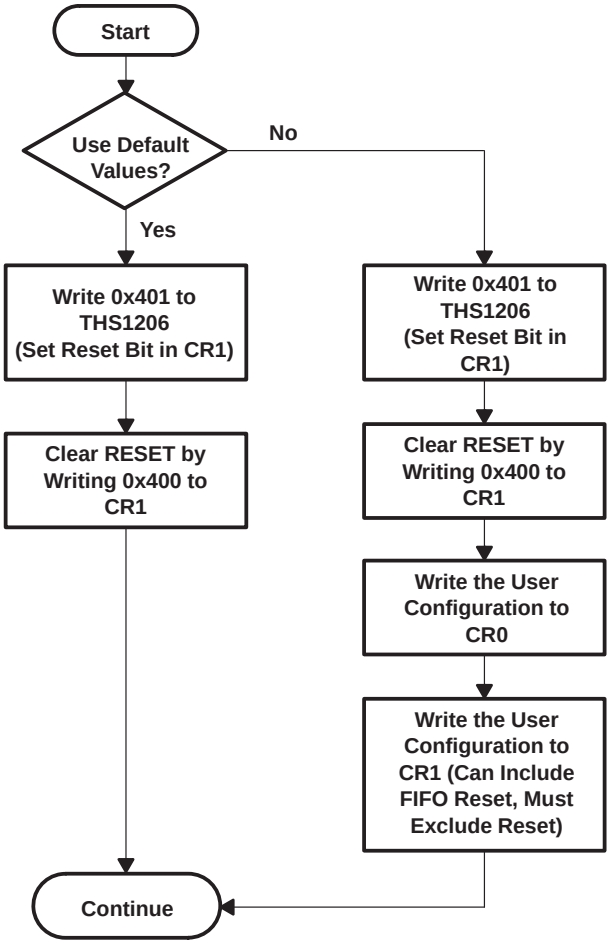

Figure 2. THS1206 Initialization

The default values are defined in the data sheet.

4 Integrated FIFO

The THS1206 has an integrated FIFO which is organized as a circular buffer in order to achieve the higher data throughputs required by today's processors. This circular buffer can store up to 16 samples. A new sample is written to the FIFO with every falling edge of the conversion clock (CONV_CLK). The FIFO has a flexible and configurable design, and it allows overwriting. This last feature can be particularly interesting in applications where data must be collected at certain intervals. The data read by the processor should always be the latest data, which is assured by the special circular buffer structure. Overwriting during the relevant intervals is prevented by fast reading the stored data.

Figure 3 shows the structure of the THS1206 FIFO. It is arranged so that sample reading takes place asynchronously to the sampling clock CONV_CLK.

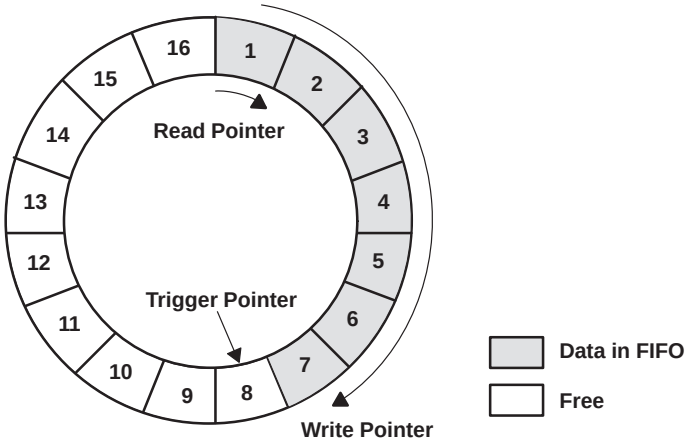

Figure 3. The FIFO as a Circular Buffer

Samples are automatically written to the FIFO. Write, read, and trigger pointers are used to control the writing and reading processes. The read pointer always points to the next location to be read. The write pointer always points to the location which contains the last written sample. With a selection of multiple analog input channels, the converted values are written to the circular buffer in a predefined sequence (autoscan mode). In this way, the channel information for the reading processor is continuously maintained.

A specific storage depth (trigger level) must be selected for the circular buffer. When this level is reached, the THS1206 signals the connected processor via the digital output DATA_AV (data available) that a block of conversion values is ready to be transferred. The block size to be read is always equal to the setting of the trigger level; this is important in order to maintain the channel information when multiple channels are selected. Table 4 shows the trigger levels available with each particular number of analog inputs selected.

Table 4. FIFO Trigger Level

BIT 3 TRIG1	BIT 2 TRIG0	TRIGGER LEVEL FOR 1 CHANNEL	TRIGGER LEVEL FOR 2 CHANNELS	TRIGGER LEVEL FOR 3 CHANNELS	TRIGGER LEVEL FOR 4 CHANNELS
0	0	01	02	03	04
0	1	04	04	06	08
1	0	08	08	09	12
1	1	14	12	12	Reserved

Let’s consider a specific example where all four analog input channels (AINP, AINM, BINP and BINM) are selected and the trigger level is set to 8. The samples are written to the FIFO according to the autoscan mode. The signal DATA_AV becomes active when the write pointer reaches the trigger pointer. Using DATA_AV as an interrupt, the processor is immediately able to read the eight-word block and the trigger pointer will be incremented by 8 (see Figure 4). If the processor can not read the data immediately, new samples are written to the FIFO and the trigger and read pointers stay at the same location. Thus, when the write pointer returns to location 1, the four oldest data samples in the FIFO are overwritten. At this time, the read pointer and the trigger pointer are incremented by the number of selected channels (four in this example) in order to maintain the channel information.

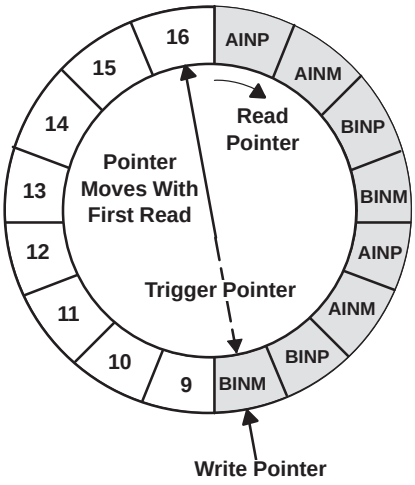

Figure 4. Example With Four Analog Inputs and a Trigger Level of 8

The programmable storage depth allows for adjustment to different processors. This technique strongly reduces the burden on the processor. The THS1206 data is transferred in batches by means of the integrated FIFO and its control logic. This represents the optimum use of the interface between the THS1206 and the processor.

A problem may be found with timely transfer of samples from the A/D processor when the conversion rate is above 1 MSPS. The data is normally transferred from the A/D converter to the processor during an interrupt-service routine (ISR). However, the maximum speed is somehow limited, as every processor exhibits a latency time (the time required for first possible access during the ISR). The latency time can amount to as much as a hundred nanoseconds, depending on the particular processor and on its frequency. The resulting speed is thereby limited to 1 MHz to 2 MHz. This creates the problems of selecting data, which is controlled via an interrupt from a fast A/D converter, and of further processing this data afterwards. Figures 5 and 6 give a more detailed explanation of this issue.

Figure 5 shows a measurement taken with the THS1206 connected to the TMS320C542 DSP, which has a cycle time of 25 ns. The clock signal CONV_CLK is set to 2 MHz in this example. The resultant DSP latency time due to the interrupt service routine within the DSP (time from DATA_AV falling edge to RD falling edge) is approximately 400 ns. This means that the DSP will not be able to read the data from the THS1206 within one CONV_CLK cycle if the processor has to jump into an interrupt service routine for every conversion value.

The FIFO incorporated in the THS1206 allows the processor to read the conversion values in a burst. Data reading in burst mode increases the data throughput, because the latency time of the processor is seen only once per burst.

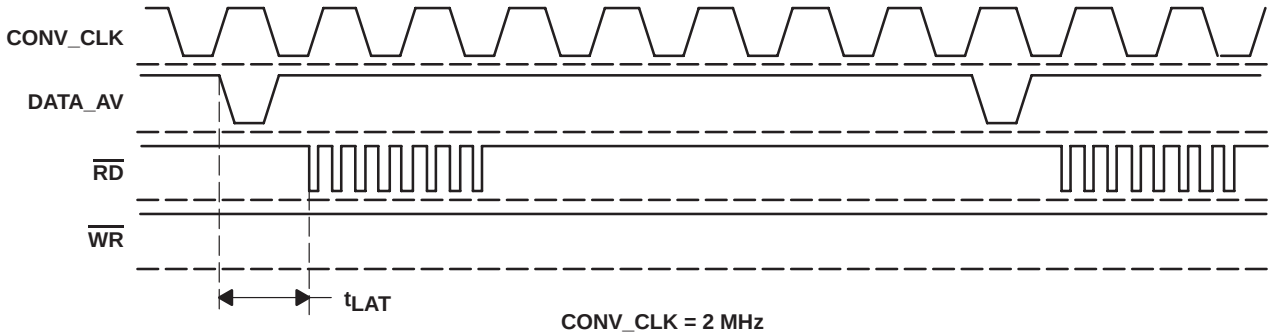

Figure 5. Reading the FIFO Data in a Burst at 2 MSPS

Figures 5 illustrates an example of burst reading of the THS1206 FIFO data. The FIFO trigger level is set to 8 in this example. This means that signal DATA_AV becomes active after writing eight values to the FIFO. Therefore, the processor must read eight values from the THS1206 within one ISR. In order to achieve the required data throughput from the THS1206 to the DSP, the DSP must be able to read all the samples before the next DATA_AV becomes active. This 2-MHz sampling frequency is only possible if reading occurs in a burst. Therefore, this approach increases the maximum data throughput.

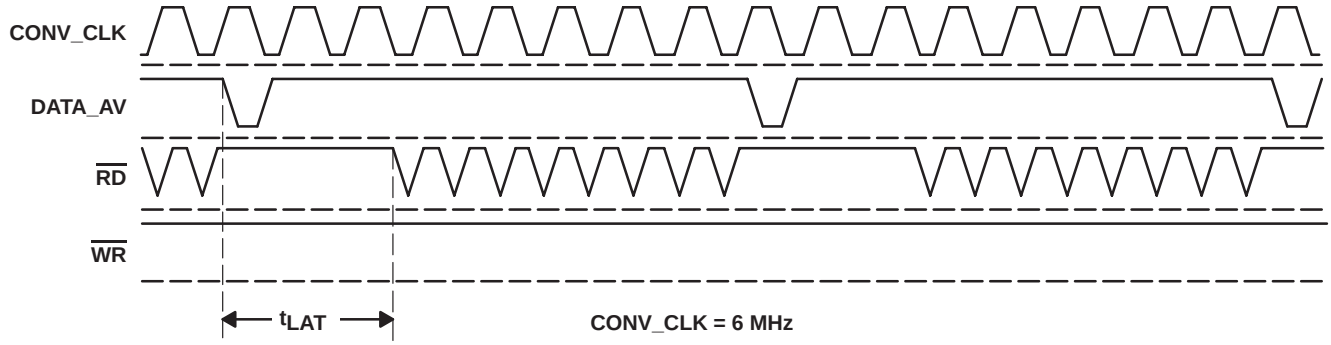

Figure 6. Reading the FIFO Data in a Burst at 6 MSPS

Figure 6 shows a measurement taken with the same THS1206 to TMS320C542 DSP interface, but using a sampling frequency of 6 MSPS. It can be observed that the processor is just able to catch the block of data between of two DATA_AV signals, which is a requirement in order to read the data from the ADC. This roughly determines the maximum data throughput between the THS1206 and the TMS320C542, with 25 ns cycle time for this mode of operation. Typically, a trigger level of 8 (9 for three analog input channels) is the best choice for an optimized data transfer rate.

5 FIFO Reset

A reset of the FIFO is typically performed when configuring the THS1206 during the last step of the initialization routine. A reset can also be performed at any other time, and it is particularly recommended when the ADC is only active during a specific time frame so that an overflow within the FIFO occurs. An example of this is the continuous reading of a block of data (such as 4K of data for a FFT) over a given period of time. Before the THS1206 starts on a new block of data, a reset should be initiated in order to reset the internal FIFO pointer and the DATA_AV signal.

6 Autoscan Mode

The autoscan mode is required in order to achieve channel integrity. In a multichannel operation, data is always written to the FIFO in a predefined sequence. Therefore, the processor always has to read a specific number of samples equal to the trigger level (TL) selected in order to have the channel information.

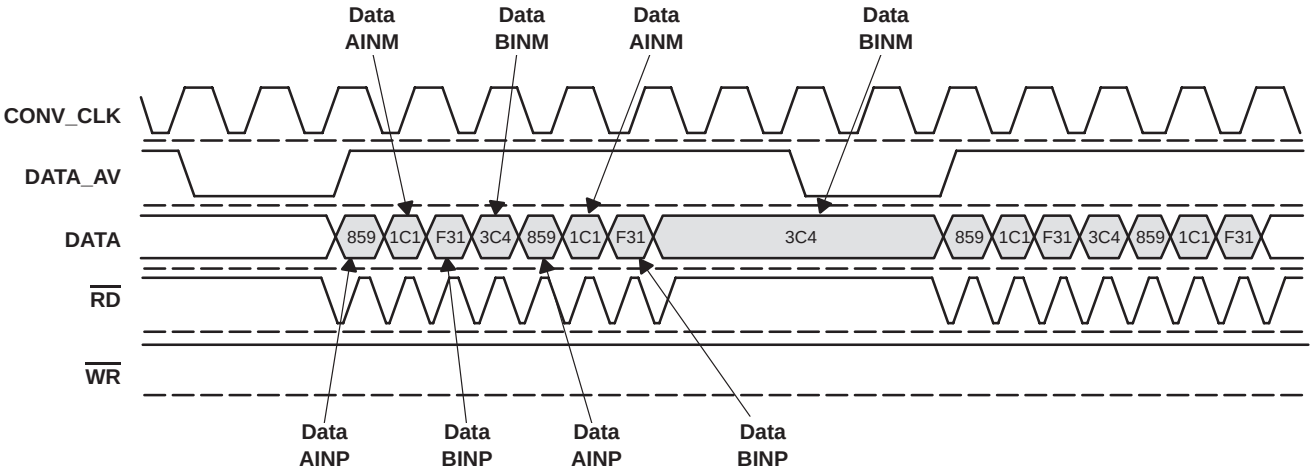

Figure 7. Autoscan Mode for TL = 8 and Four Analog Inputs

Using four analog input channels and a trigger level of eight as an example, the processor has to read within each interrupt service routine, as illustrated in Figure 7. The first data read after DATA_AV becomes active belongs to channel AINP. This remains valid as long as the processor reads a number of times equal to the trigger level (TL) for every activation of DATA_AV.

7 Control Signal DATA_AV

DATA_AV (data available) can be used as a control signal to indicate the processor that data is ready to be read from the FIFO. DATA_AV can be programmed in a flexible way. This section gives detailed information on the possible configurations and on the behavior of DATA_AV after reset and during operation.

DATA_AV becomes active when the write pointer associated with the FIFO reaches the trigger pointer. Since the write pointer is incremented with every clock cycle, there is a relation between the conversion clock CONV_CLK and signal DATA_AV. The number of clock cycles until the signal DATA_AV becomes active is equal to the selected trigger level (TL). This relationship remains true as long as the processor can read the data from the THS1206 on time.

However, the behavior is different after reset of the THS1206. The first conversion value is written to the FIFO with a delay (latency) caused by the pipeline architecture and the reset architecture of the THS1206. DATA_AV becomes active 7 + TL conversion clock cycles after reset.

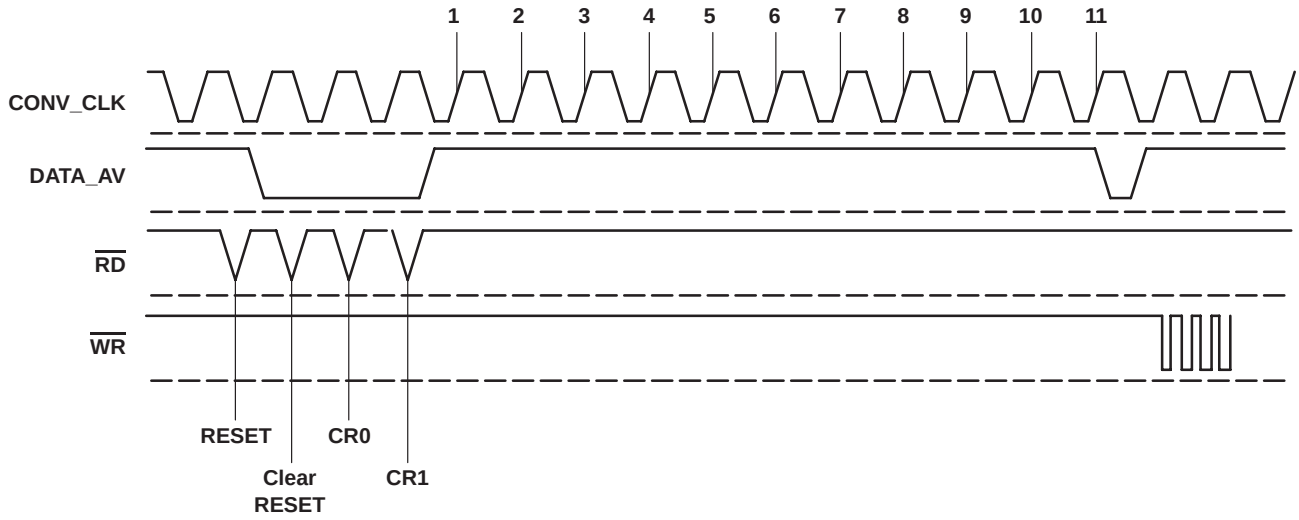

Figure 8. DATA_AV (In Active-Low, Pulse Configuration) After Reset

Figure 8 shows the timing of the signal DATA_AV after reset. The trigger level in this example is set to 4. Therefore, it takes 7 + TL = 11 conversion clock cycles until DATA_AV first becomes active after reset. It can be seen in Figure 8 that signal DATA_AV goes into its default mode, which is active high pulse, immediately after reset. DATA_AV is therefore switched to low level after reset. DATA_AV goes into the configured mode (active low pulse here) right after being configured through control register 1. DATA_AV is typically connected to a processor interrupt input. Therefore, it is important to disable the interrupt during the THS1206 initialization routine; if this is not done, the processor jumps into an interrupt service routine (ISR).

DATA_AV becomes active during operation after the processor has been able to read the stored data and the FIFO write pointer reaches the trigger pointer again. This can also be seen in Figure 8, where the processor is able to read the data immediately after DATA_AV has become active.

8 Configuration of DATA_AV

Control signal DATA_AV (data available) is typically connected to a processor interrupt input. These inputs are edge or level sensitive. DATA_AV can be adjusted to different kinds of interrupt inputs. The possible settings using Bits 4 and 5 are shown in Table 5.

Table 5. Configuration of DATA_AV

BIT 5 DATA_P	BIT 4 DATA_T	DATA_AV TYPE
0	0	Active low level
0	1	Active low pulse
1	0	Active high level
1	1	Active high pulse

9 DATA_AV in Pulse Mode

In pulse mode, control signal DATA_AV is activated with the rising edge of the conversion clock if the trigger condition is satisfied. DATA_AV becomes inactive with the next falling edge of the conversion clock. Therefore, the pulse width is equal to half a clock cycle of the conversion clock. The next activation of DATA_AV will not happen until the processor has read the block of data with a block size equal to the trigger level TL. This is shown in Figure 9 for signal DATA_AV in the pulse mode and active-low configuration. The trigger level TL is set to 8 in this example.

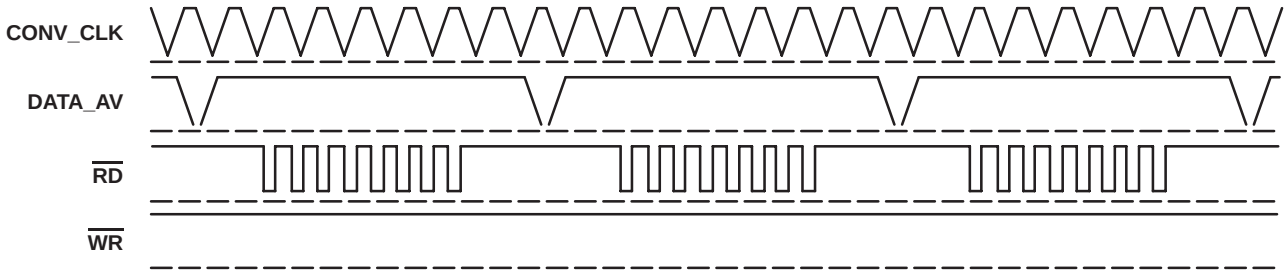

Figure 9. Timing of DATA_AV in Pulse Mode

The timing in this mode changes only if the first read in a block occurs before the falling edge of the conversion clock. In this case, the falling edge of the first fast signal read forces DATA_AV to become inactive earlier, instead of waiting for the CONV_CLK. This behavior is shown in Figure 10.

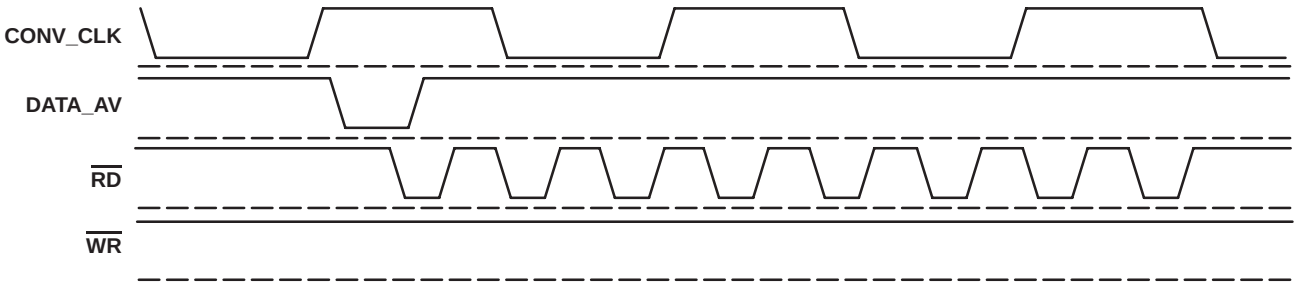

Figure 10. Timing of DATA_AV in Pulse Mode With Early Read

10 DATA_AV in Static Mode

In the static mode, DATA_AV becomes active with the rising edge of the conversion clock. It switches back to inactive mode as soon as the processor starts the first read operation. The next activation of DATA_AV will not occur until the block of data has been read, The block size is equal to the trigger level TL. This is shown in Figure 11 for the signal DATA_AV in the static mode and active-low configuration. The trigger level TL is set to 8 in this example.

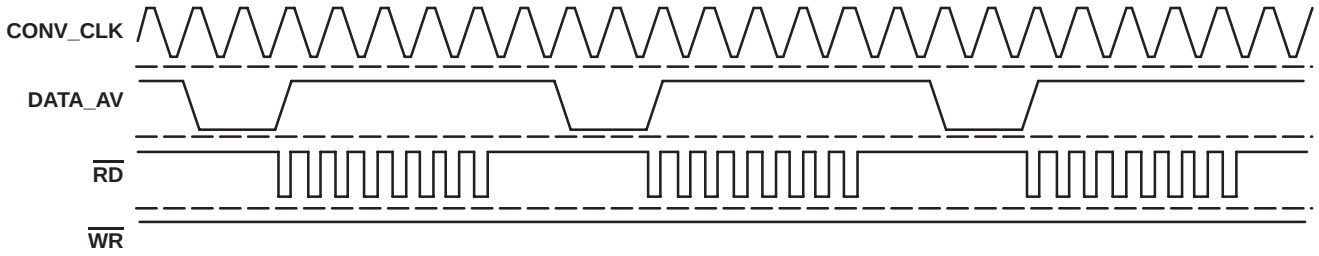

Figure 11. Timing of DATA_AV in Static Mode

11 Continuous-Conversion Mode

The THS1206 offers two different conversion modes: continuous and single. These modes can be programmed using bit 1 of control register 0. The continuous-conversion mode is of particular interest in applications where a block of data is required for signal analysis. An example of this is the FFT (fast fourier transformation). Typically, a set of data with more than 1000 (1024, 2048, 4096) values will be used in a Cooley-Tukey radix-2 algorithm.

The THS1206 operates in the continuous-conversion mode with a free-running external clock with a 50% duty cycle applied to the digital input CONV_CLK. A new conversion is continually initiated with every falling edge of the clock signal. The converted values are written to the FIFO with a latency of 5 clock cycles. This latency results from the pipeline architecture of the analog-to-digital converter. Figure 12 shows the latency time $t_{d(pipe)}$ and the general timing with selection of just one analog input channel. Control signal DATA_AV is shown in this figure for trigger levels of 1 and 4. The resulting maximum conversion rate with one analog input channel is 6 MSPS.

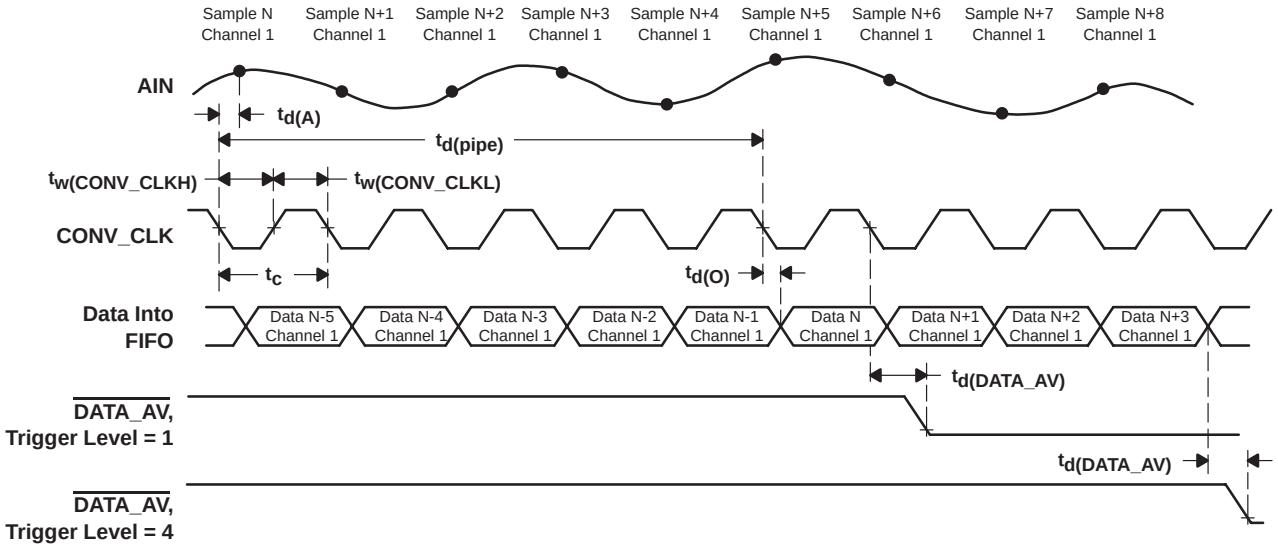

Figure 12. Timing of Continuous-Conversion Mode (One-Channel Operation)

Figure 13 shows the timing of the continuous-conversion mode with four analog input channels selected. The maximum throughput rate in this mode is 1.5 MSPS per channel. Every fourth falling edge of the conversion clock simultaneously switches the four sample and hold stages from the sample mode to the hold mode. The conversion of the four analog inputs is performed sequentially afterwards.

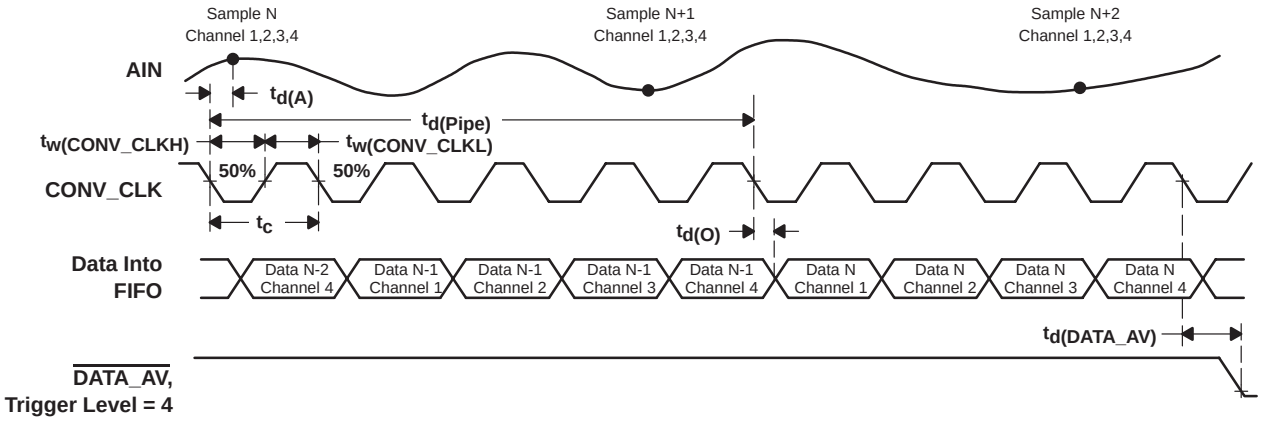

Figure 13. Timing of Continuous-Conversion Mode (Four-Channel Operation)

A new sample is written to the FIFO with every falling edge of the conversion clock. It becomes necessary to maintain the channel information when more than one analog input channel is selected. The converted values are written to the FIFO in a predefined sequence according to the autoscan mode. The processor always has the channel information. The timing of the DATA_AV signal is shown here for a trigger level of 4.

12 Single-Conversion Mode

The single-conversion mode performs a single conversion of the selected analog input channels. The single-conversion mode can be selected with bit 1 of control register 0. A pulse on the $\overline{\text{CONVST}}$ input initiates the conversion. At the falling edge of $\overline{\text{CONVST}}$, the sample and hold stages of the selected analog inputs are simultaneously placed into hold mode, and conversion of the selected analog input channels is started sequentially. The conversion clock is generated internally using an internal clock oscillator circuit. The trigger level can be selected from Table 4. Control signal DATA_AV displays the same behavior as in the continuous-conversion mode. Figure 14 shows the timing of the single-conversion mode. Up to four analog input channels can be selected and sampled simultaneously.

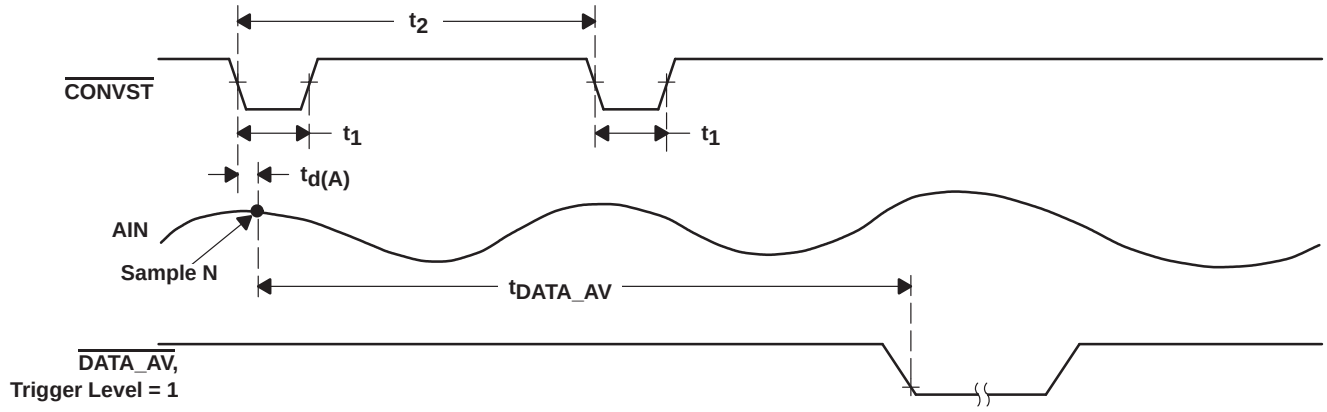

Figure 14. Timing of Single-Conversion Mode

In Figure 14, the time (t_2) between consecutive starts of single conversions depends on the number of analog input channels selected. The individual timing parameters are specified in the data sheet.

The single-conversion mode is of particular interest in control applications, where it is especially important to preserve the relative phase information between the selected analog input channels. The initiation of the conversion (switching from sampling to hold modes) is controlled by an external signal which can be applied to the $\overline{\text{CONVST}}$ (conversion start) input.

13 Reference Voltage

The THS1206 provides two internal reference voltages to the analog-to-digital converter: VREFP (the upper 3.5-V reference voltage) and VREFM (the lower 1.5-V reference voltage). It is important to bypass the external reference pins REFP and REFM with a 10-µF tantalum capacitor to AGND in order to stabilize the reference voltages. In addition to the internal references, the THS1206 provides a 2.5-V external reference output voltage (REFOUT). This reference voltage can be used to bias the operational amplifiers to bring their output voltage into the input range of the THS1206. This signal can also be used to bias the center tap of a transformer. In this case, REFOUT sets the common-mode voltage for the secondary side of the transformer. REFOUT should be bypassed with a 10-µF tantalum capacitor to AGND.

An external reference voltage can be chosen in order to fulfill the dc requirements. This option should be programmed via the internal control register. The external references should be applied to REFP and REFM.

14 Read-Back Mode

The content of control registers 0 and 1 can be read back if bit 9 of control register 1 is set to 1. This mode is especially important during the debug phase of system development in order to ensure successful writing to the THS1206. The DATA_AV signal is disabled in this mode. The content of the two control registers is alternately placed on the data bus while continuously reading, beginning with the content of control register 0. The initialization routine must be performed again in order to bring the THS1206 back to the normal conversion mode.

15 Test Mode

The THS1206 provides a test mode where the analog-to-digital converter digitizes a specific reference voltage instead of an analog input voltage. The test mode can be programmed via bits 8 and 9 of control register 0. Table 6 shows the different modes. It is possible to select the upper reference voltage V_{REFP}, the lower reference voltage V_{REFM}, or the common-mode output voltage of both reference voltages.

Table 6. Test Modes of the THS1206

BIT 9 CR0	BIT 8 CR0	OUTPUT RESULT
0	0	Normal mode
0	1	V_{REFP}
1	0	$[(V_{REFM}) + (V_{REFP})]/2$
1	1	V_{REFM}

These test modes can be used during the debugging phase to verify the THS1206 conversion result and the interface to the processor. The conversion result in the test mode is always in binary data format, regardless of the selection of output data format (bit 7 in control register 1). Therefore, the conversion result should be in the proximity of 4095 for VREFP, 2047 for (VREFP-VREFM)/2, and 0 for VREFM.

The conversion is based on the reference voltage selected: either internal or external. This option must be configured via the internal control register.

The DATA_AV signal is disabled in this test mode. This means that the conversion value of the test voltage can be read from the processor independent of any control signal. However, this means that in the test mode the DATA_AV signal can not be used as a control signal to cause the processor to jump to an interrupt service routine.

16 Overflow Flag

An overflow flag set to 1 indicates that the FIFO data was overwritten before the processor was able to read it. This feature can be useful during debugging and development phases were the processor software must be tested. Such tests can be conducted as indicated in the following example. The application demands the processing of 4,096 digital values. It must be ensured that FIFO overflow does not occur during the conversion process. The overflow condition can be checked immediately after the 4,096 values have been read in order to ensure that the processor is sufficiently fast to read all the data. The THS1206 should be programmed into the read-back mode to read the overflow bit. Since the conversion clock is still running, the procedure must be sufficiently fast to prevent an overflow during the test. The initialization routine should be performed again to bring the THS1206 back to normal conversion mode. The overflow flag is set back to 0 during the initialization routine.

17 Equivalent Analog Input Schematic

The THS1206 analog input consists of a differential sample and hold amplifier. This architecture allows the ADC to be configured to single-ended or to differential configurations. Figure 15 is a schematic of the equivalent THS1206 analog input in single-ended mode. The architecture is similar in differential mode, with REFIN replaced by AINM and CH changed to 800 fF.

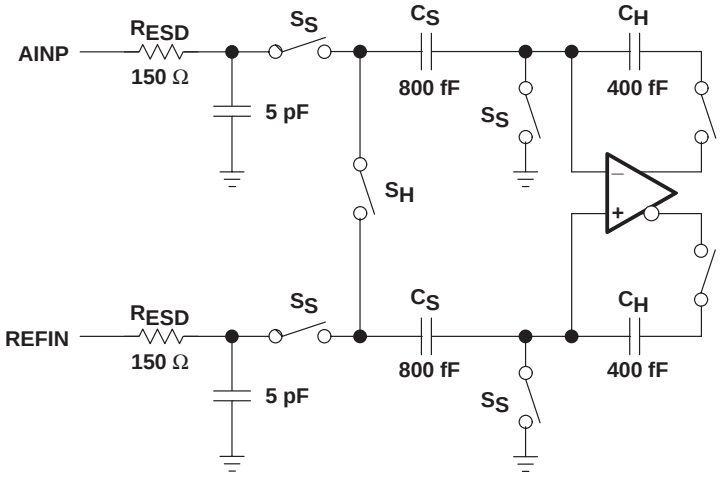

Figure 15. Equivalent Analog Schematic

The input sees a fixed 150-Ω series ESD resistor and a fixed 5-pF capacitor to analog ground. The analog input signal is sampled with the C_S capacitors, while the S_S switches are closed and the S_H switches are open. During hold mode, the S_H switches are closed, the S_S switches are open, and the charge of the sampling capacitors is transferred to the hold capacitors and becomes available at the output of the amplifier.

18 Analog Input Configuration

The THS1206 features four analog input channels. These channels can be configured for either single-ended or differential operation. Figure 16 shows a simplified model with a single-ended configuration selected for channel AINP. The reference voltages for the ADC itself are VREFP and V_{REFM} (either internal or external reference voltages). The analog input voltage ranges from V_{REFM} to V_{REFP}. This means that V_{REFM} defines the minimum voltage, and V_{REFP} defines the maximum voltage that can be applied to the ADC. The internal reference source provides the voltage V_{REFM} of 1.5 V and the voltage V_{REFP} of 3.5 V (see the Reference Voltage section). The resulting analog input voltage swing of 2 V can be expressed by:

$$V_{REFM} \leq AINP \leq V_{REFP} \quad (1)$$

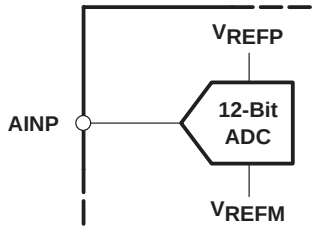

Figure 16. Single-Ended Input Stage

In many applications a differential operation is required to attain a better signal-to-noise ratio. Figure 17 shows a simplified model of analog inputs AINM and AINP, which are configured for differential operation. The differential mode is recommended because it offers benefits in performance over the single-ended mode. However, the THS1206 offers two differential analog inputs in this mode, while the single-ended mode offers four analog inputs. Common-mode noise and common-mode voltages can be rejected using a differential analog input architecture. Further details on both modes are given below.

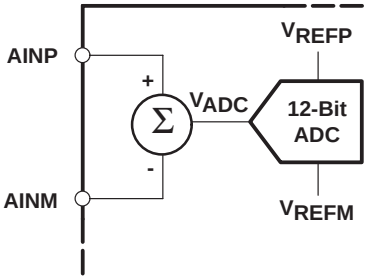

Figure 17. Differential Input Stage

In contrast to the single-ended configuration, it can be seen that the voltage VADC applied at the input of the ADC is the difference between the AINP and AINM inputs. The voltage VADC can be calculated as follows:

$$VADC = |AINP - AINM| \quad (2)$$

The advantage of single-ended operation is that the common-mode voltage:

$$V_{CM} = \frac{AINM + AINP}{2} \quad (3)$$

can be rejected in the differential configuration if the analog input satisfies the following conditions:

$$AGND \le AINM,\ AINP \le AV_{DD} \quad (4)$$

$$1\ V \le V_{CM} \le 4\ V \quad (5)$$

18.1 Single-Ended Mode

The THS1206 can be configured for single-ended operation using dc or ac coupling. In either case the THS1206 input should be driven by an operational amplifier that does not degrade the performance of its ADC. Because the THS1206 operates from a single 5-V supply, it is necessary to level-shift ground-based bipolar signals to comply with its input requirements. This can be achieved with dc and ac couplings. Application examples will be shown for both methods.

18.2 DC Coupling

An operational amplifier can be configured to shift the signal level according to the THS1206 analog input voltage range. This voltage range extends from 1.5 V to 3.5 V. An op amp can be used as shown in Figure 18.

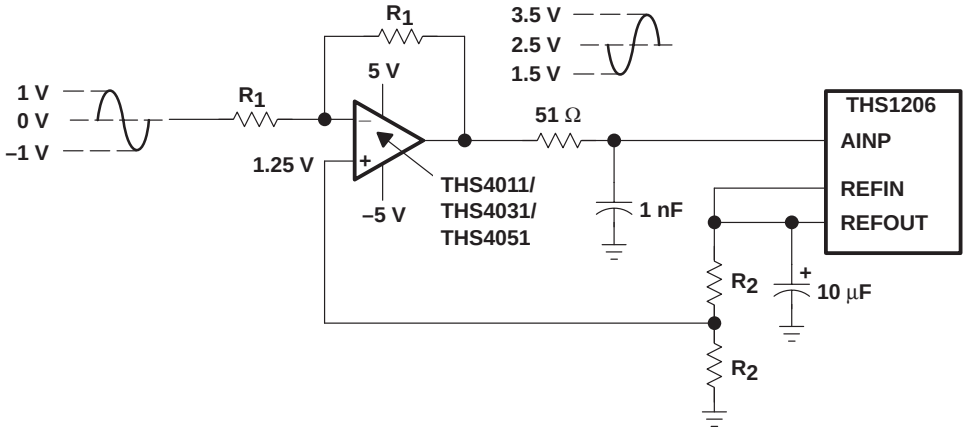

Figure 18. Level Shift for DC-Coupled Input

Figure 18 shows an application example where an analog input signal range of –1-V to 1-V is shifted by an op amp to the analog input range of the THS1206 (1.5 V to 3.5 V). The op amp is configured as an inverting amplifier with a gain of –1. The required 1.25 Vdc voltage at the noninverting input is derived from the THS1206's 2.5-V output reference REFOUT by using a resistor divider. Therefore, the op amp output voltage will be centered at 2.5 V. The 10-μF tantalum capacitor is required to bypass REFOUT. REFIN should be directly connected to REFOUT in single-ended mode. The use of ratio-matched, thin-film resistor networks minimizes gain and offset errors. A resistor value of 10 kΩ is recommended, since REFOUT is capable of delivering 250 μA. The RC filter (with R = 51 Ω and C = 1 nF) at the output of the op amp improves the THS1206 dynamic performance.

Texas Instruments provides a wide range of high speed operational amplifiers which best fit the THS1206. The THS4051 is an excellent choice for high-speed applications. It has a high slew rate of 200 V/μs and an extremely-low distortion of only –87 dB at ± 5-V supply voltage. For higher dc precision requirements, the THS4031 is a good choice with its maximum input offset voltage of only 2 mV. Other parameters include an extremely low distortion of –90 dB and a slew rate of 80 V/μs at ± 5-V supply voltage.

18.3 AC-Coupled Input

Figure 19 shows an analog input ac-coupled to the THS1206. Capacitor C_1 is placed in series with the input of the op amp for ac-coupling. The analog signal is shifted by biasing the noninverting input of the amplifier with the THS1206's REFOUT signal.

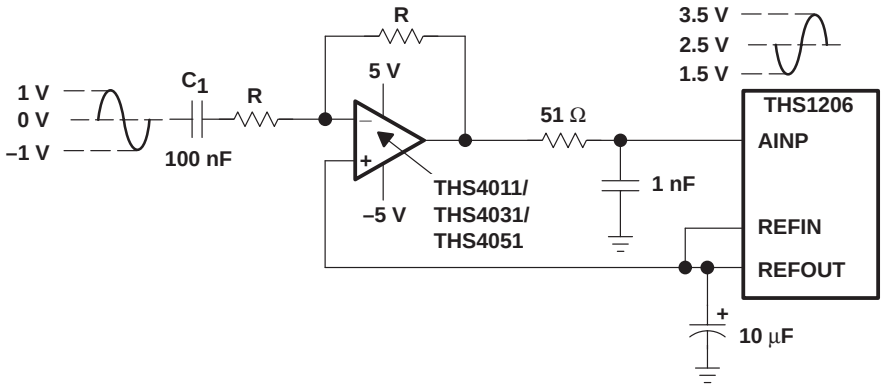

Figure 19. AC-Coupled Input

18.4 Differential Mode

In the differential mode of operation, a differential analog signal is applied to the differential input of the THS1206. A conversion from a single ended to a differential signal is required in most cases. This can be achieved in different ways: using two operational amplifiers configured to provide a differential output, or using an operational amplifier to provide a differential input as well as a differential output.

An RF transformer with a center tap on the secondary side provides an alternative to the operational amplifier. The use of the RF transformer is advantageous at the higher frequencies in terms of total harmonic distortion (THD) and spurious free dynamic range (SFDR). The center tap of the transformer can be used to shift the differential signal to the common-mode level required. In contrast to the operational amplifier, the analog signal is ac-coupled automatically when using an RF-transformer.

Figure 20 shows an RF-transformer used to generate a differential signal from a single-ended signal. The center tap of the secondary is connected to REFOUT of the THS1206. Therefore, the common-mode level of the analog signal is tied to REFOUT, which is 2.5 V. The RC filter (with R = 51 Ω and C = 1 nF) in front of the analog input of the THS1206 op amp improves the noise performance.

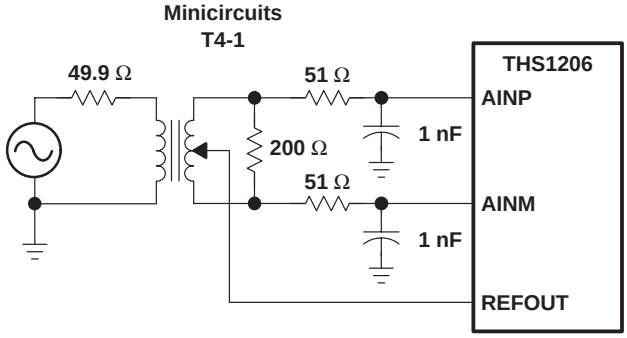

Figure 20. Single-Ended to Differential Conversion by Transformer

19 Layout Considerations

The layout of a mixed signal design must fulfill the digital and analog signal requirements. In purely digital systems, the signals to be transmitted from one point (device) to the other are solely high- and low-levels. Very fast edges (up to 200 ps/V) can occur with high-speed devices. These fast edges cause very high current spikes on the supply voltage. In analog systems it is most important to transceive signals without distortion, noise, ripple, or crosstalk. In mixed signal systems the challenge is to avoid coupling from the noisy digital portion to the sensitive analog area, especially with the increasing processor clock rates. The analog portion must be decoupled from the digital portion. Using the THS1206 as an example, the weight of one LSB (least significant bit) in the single-ended mode is less than 500 μV, indicating that any interference from the processor can easily exceed this value. It becomes especially important to review some of the basic rules in order to make the analog side of a mixed signal design less sensitive to any digital activity in the system.

The mixed signal design requires the use of a multilayer board to minimize the influence of the noisy digital part into the analog part, especially at higher speed and resolution. Figure 21 shows an example of a four-layer board. The multilayer board allows for separation of the analog and digital sections of the system.

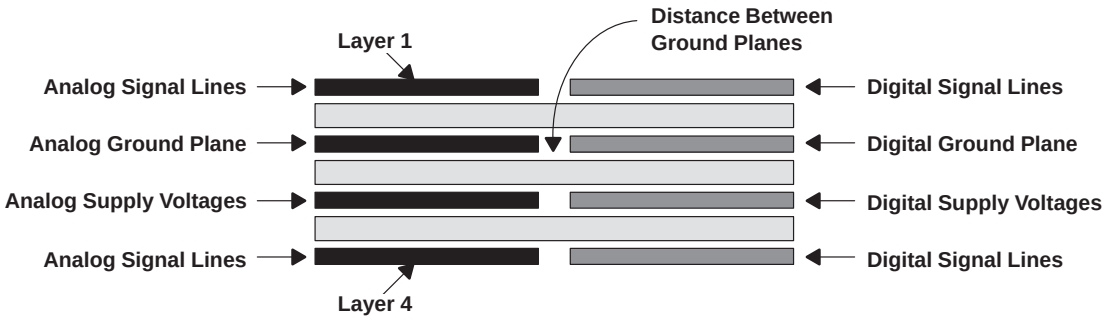

Figure 21. Mixed-Signal Four-Layer Board

The second layer provides separate analog and digital ground planes. The first and fourth layers are used for the analog and digital signal lines. The analog signal lines are laid over the analog ground plane, and the digital signal lines are laid over the digital ground plane. The analog signal lines should be as short as possible, not too dense, and parallel to other lines. The area between signal lines can be filled by extending the ground area connected to the ground plane. This provides further shielding and reduces the sensitivity to coupling and crosstalk, especially important with analog signals. The third layer provides the analog and digital supply voltages. The two adjacent ground and supply line planes form an extremely-low inductive decoupling capacitor. This design results in the best decoupling between analog and digital signal lines.

Figure 22 illustrates the recommendations for ground-plane splitting on the THS1206. Splitting of the ground plane is done directly below the THS1206 so that all digital pins are beyond the digital ground plane, and the analog pins are beyond the analog ground plane. The split between ground planes should be separated by at least 3 mm to minimize the capacitance between these planes.

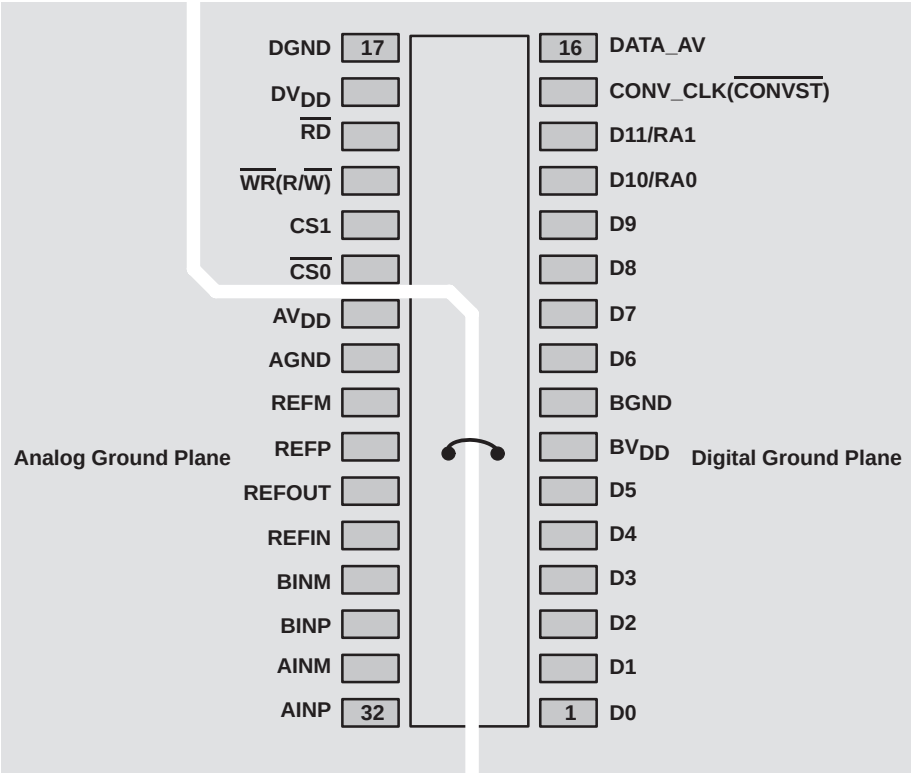

Figure 22. Recommendation for Ground Planes

All analog components and analog signal lines should be placed above the analog ground plane. All digital components and digital signal lines should be placed above the digital ground plane. The analog and digital ground planes should only be connected together at one point. It is recommended to not have more than one connection between ground planes in order to avoid ground loops which can heavily disturb the overall system performance. There are different solutions to the ground plane connection. One option is a connection directly below the ADC, as shown in Figure 22. A second option is to connect at the system power supply. It is best to implement multiple ground connection options during the prototype phase. The best connection for the final board can be determined during this evaluation.

The power supply for a mixed signal design is also a main factor on system performance. This is particularly important for the analog-to-digital converter, which is typically provided with separate analog and digital supply pins. To minimize the interference between the digital and analog systems, separate supply voltages should be provided for the analog and digital portions. However, in many applications it is possible to find a common supply for a mixed-signal design. In this case it becomes necessary to decouple the analog and digital supply voltages from the common supply voltage. The decoupling of the analog and digital supplies should be implemented using LC-filtering (10 μF, 10 mH) as illustrated in Figure 23. The inductor prevents the propagation of high-frequency interference between the digital and analog sides. The decoupling capacitor maintains a stable supply voltage as a protection against the occurrence of current spikes, especially from the digital side of the system.

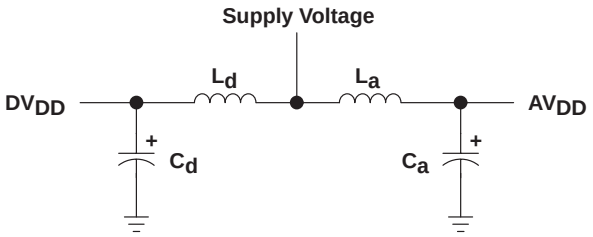

Figure 23. Common Supply for a Mixed Signal Design

The THS1206 provides separate supply pins for the analog side (AV_{DD}, AGND), for the digital side (DV_{DD}, DGND), and for the buffer unit (BV_{DD}, BGND) of the device. The buffer has its own supply pins to minimize noise interference to the sensitive analog area during switching of the relatively-strong buffer. AV_{DD} should come from the analog supply, and DV_{DD} and BV_{DD} should come from the digital supply. Every supply should have its own decoupling. This filtering is very important because the digital supply for the THS1206 comes from the common digital supply voltage.

The analog portion of the THS1206 should be decoupled from the noisy digital supply voltage. This is typically done by using a 10-µF tantalum capacitor in parallel with a 100-nF ceramic capacitor. The tantalum capacitor takes care of the lower-frequency disturbing components, while the ceramic capacitor takes care of the higher-frequency disturbing components. New tantalum capacitors are available with similarly good behavior at both low and high frequencies (for example, the Siemens™ B45196E3106). The use of a ceramic capacitor in parallel with a tantalum capacitor has now become unnecessary. In addition to the capacitor, a 10-µH inductor should be used to provide further filtering. This bypassing example is shown in Figure 24. The bypass capacitors should be placed as close as possible to the THS1206 supply pins.

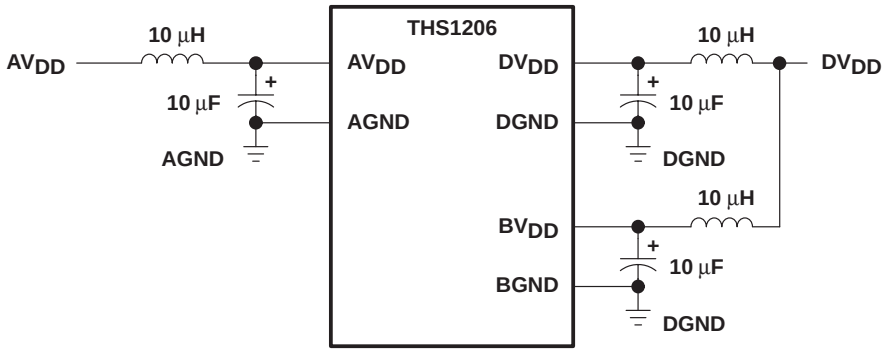

Figure 24. Use of Bypassing With The THS1206

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20 Parallel Interface

Interfacing an A/D or a D/A converter to a digitial signal processor (DSP) requires exact analysis of the timing relationship between the two devices. It is relatively simple to connect A/D and D/A converters equipped with a standard serial interface. However, the connection becomes more complex with converters that have a parallel interface: the timing between individual signals and the address bus must be carefully checked. In the case of parallel interface, there can be many ways to build an interface.

The THS1206, which contains a 12-bit wide parallel data bus, provides a very flexible and simple DSP interface. Some of its important features are a configurable read and write input ($\overline{WR}$, R/$\overline{W}$) and a programmable control signal DATA_AV. Modern processors have either a combined read-write output (R/$\overline{W}$), or separate outputs for reading and writing ($\overline{RD}$ and $\overline{WR}$). The THS1206 can be connected to both types of processors without any external logic devices. The write access is required to reset and configure the THS1206 to the desired operation mode. The read access transfers conversion samples from the THS1206 to the DSP.

Reading from the THS1206 is triggered by an internal $\overline{RD}_{int}$ signal, which is generated by the logical combination of external signals $\overline{CS0}$, CS1, and $\overline{RD}$ (see Figure 25). This signal strobes the words out of the FIFO and enables the output buffers. The last external signal (either $\overline{CS0}$, CS1, or $\overline{RD}$) to become valid makes $\overline{RD}_{int}$ active while the write input ($\overline{WR}$) is inactive. The first one of these external signals to switch to inactive state deactivates $\overline{RD}_{int}$ again.

Writing to the THS1206 is controlled by internal signal $\overline{WR}_{int}$, which is generated by the logical combination of external signals $\overline{CS0}$, CS1, and $\overline{WR}$. This signal strobes the control words into control registers 0 and 1. The last external signal (either $\overline{CS0}$, CS1, or $\overline{WR}$) to become valid activates $\overline{WR}_{int}$ while the read input (RD) is inactive. The first one of these external signals switching to its inactive state deactivates $\overline{WR}_{int}$ again.

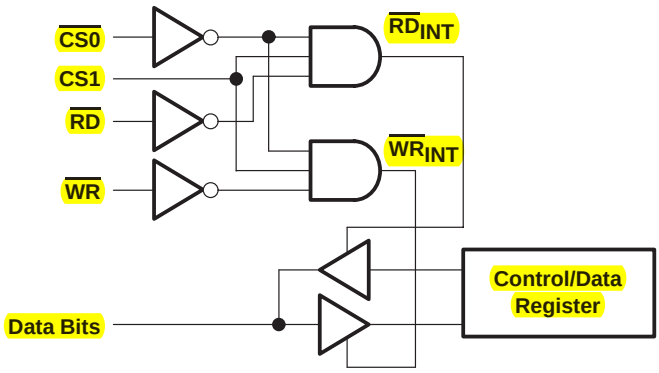

Figure 25. Logical Combination of $\overline{CS0}$, CS1, $\overline{RD}$, and $\overline{WR}$

21 Interfacing the THS1206 to the TMS320VC5402

Figure 26 illustrates an example where the THS1206 is connected to a TMS320VC5402 digital signal processor. The processor controls the reading and writing via the combined output R/$\overline{W}$. The THS1206 programmable write input $\overline{WR}$ is therefore configured as a combined read and write input (R/$\overline{W}$). The $\overline{RD}$ input has to be pulled to high level in this operating mode. The THS1206 is selected via the two chip select inputs $\overline{CS0}$ and CS1. Selection of the I/O peripheral is controlled via output $\overline{IOSTRB}$ of the TMS320VC5402, which is connected to input $\overline{CS0}$. Address line A14 is connected to input CS1 to select the THS1206.

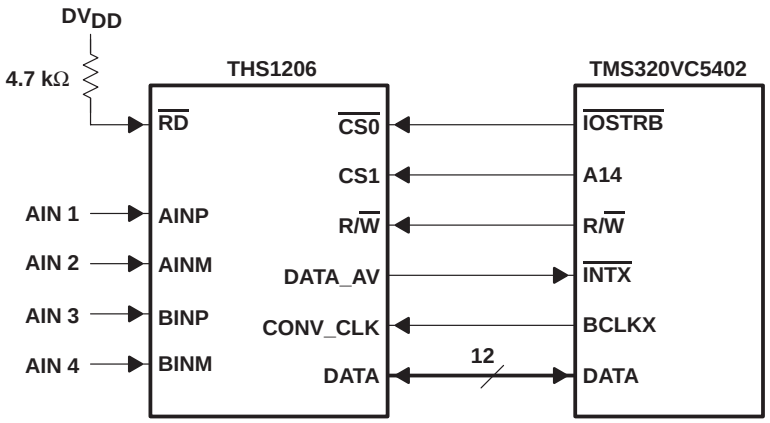

Figure 26. Interfacing the THS2106 to the TMS320VC5402

The THS1206 data bus (D0–D11) is directly connected to the TMS320VC5402 data bus. D0–D11 of the THS1206 can be connected to the lower data bits D0–D11 or to the higher data bits D4–D15 of the TMS320VC5402. This choice should be application dependent. In this example, the conversion clock is generated by the TMS320VC5402 serial port. Signal BCLKX can be programmed to provide a clock signal with a 50% duty cycle. To attain the best dynamic performace it is recommended to use a low-jitter external clock source. The clock source jitter has a significant impact on noise performance. The converted data is read by the TMS320VC5402 and then triggered via an interrupt ($\overline{\text{INTX}}$) connected to DATA_AV.

Figure 27 shows the timing diagram for a write to the THS1206 based on the interface shown in Figure 26. The data is latched into the THS1206 with the rising edge of $\overline{\text{IOSTRB}}$. The data setup (t_{su}) and hold time (t_h) of the THS1206 have to be aligned with the timing for a *parallel I/O port write* of the TMS320VC5402.

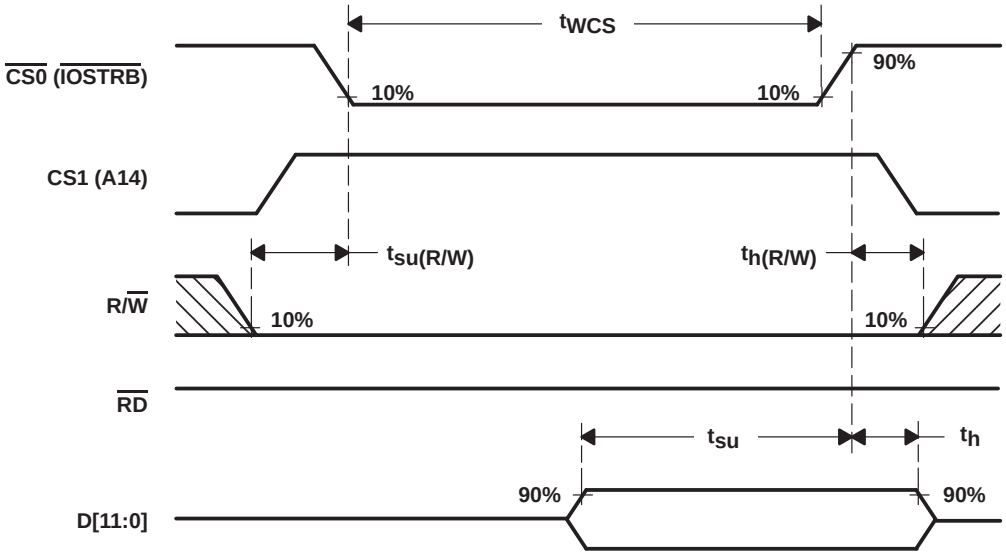

Figure 27. Write Access to the THS1206 ($\overline{\text{CS0}}$-$\overline{\text{IOSTRB}}$-Controlled)

If the setup time for the processor data is too small, the timing between peripheral and processor must be adjusted. This adjustment is done from the TMS320VC5402 by programming of internal wait states.

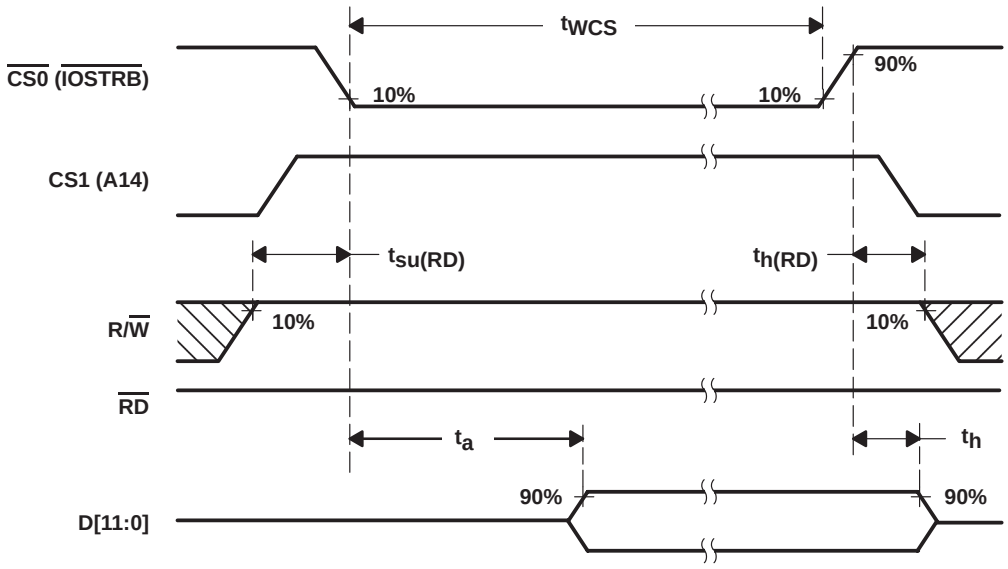

Figure 28. Read Access to the THS1206 ($\overline{CS0}$-$\overline{IOSTRB}$-Controlled)

Figure 28 shows the THS1206 read timing diagram based on the interface to the TMS320VC5402. The data to be read from the THS1206 is latched into the TMS320VC5402 with the rising edge of $\overline{IOSTRB}$. The data access (t_a) and hold (t_h) times of the THS1206 must be aligned with the timing of the TMS320VC5402 *parallel I/O port write*. The timing should be adjusted if the access time of the peripheral is too high. This adjustment is done from the TMS320VC5402 by programming of internal wait states.

22 Interfacing the THS1206 to the TMS320C6211

Figure 29 shows the THS1206 connected to a TMS320C6211 digital signal processor. The processor controls reading and writing via outputs $\overline{ARE}$ and $\overline{AWE}$, respectively. The THS1206 is configured with a write input $\overline{WR}$ and a read input $\overline{RD}$. The THS1206 A/D converter is selected via control output $\overline{CE1}$. The THS1206 is addressed via address line EA20.

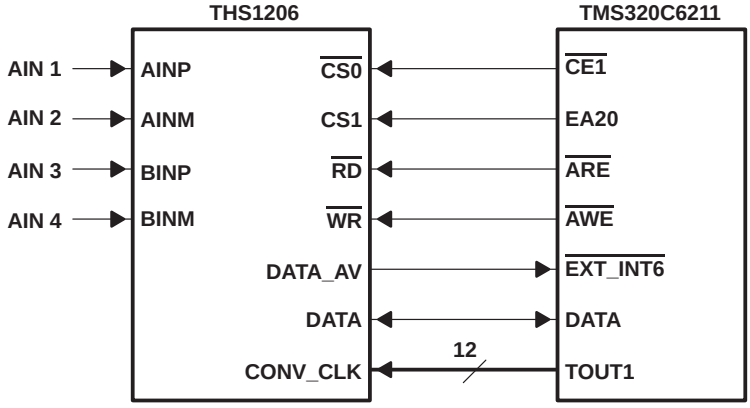

Figure 29. Interfacing the THS1206 to the TMS320C6211

The THS1206 data bus (D0–D11) is directly connected to the TMS320C6211 data bus. In this example, the conversion clock is generated by timer1, which can be configured to provide a clock signal with a 50% duty cycle. The use of a low-jitter external clock source is recommended to attain the best dynamic performance. Clock source jitter has a significant impact on noise performance. The converted data is read by the TMS320C6211 under control of an interrupt ($\overline{\text{EXT\_INT6}}$) connected to DATA_AV.

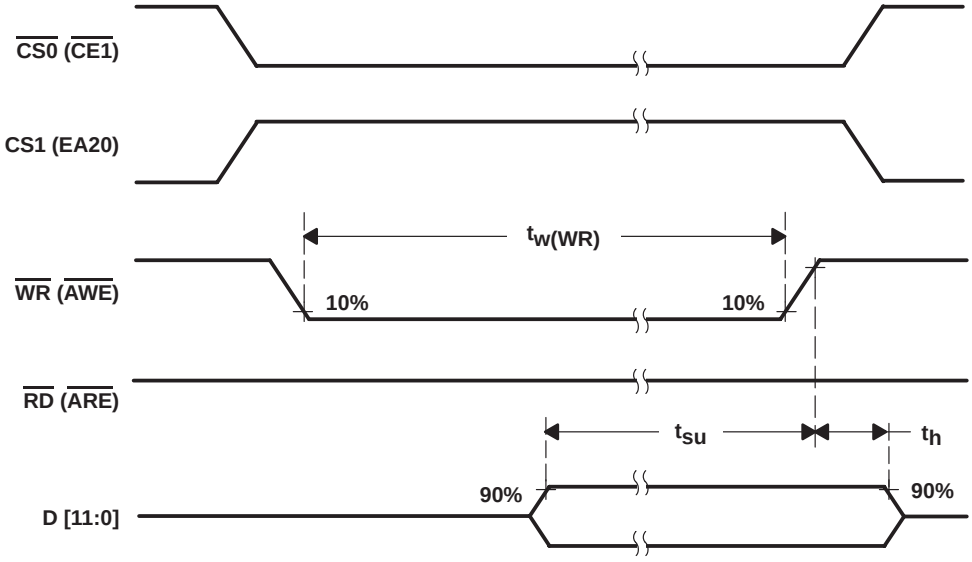

Figure 30. Write Access to the THS1206 ($\overline{\text{WR}}$-$\overline{\text{AWE}}$-Controlled)

Figure 30 shows the THS1206 write timing diagram for an interface to the TMS320C6211. The data is latched into the THS1206 with the rising edge of $\overline{\text{AWE}}$. The THS1206 data setup (t_{su}) and hold (t_h) times must be compared with the *asynchronous memory write timing* of the TMS320C6211. If the setup and hold times for the TMS320C6211 data are too small, the timing between the peripheral and the processor should be adjusted. This adjustment can be done easily on the TMS320C6211 by programming of internal wait states for the setup and for the hold times.

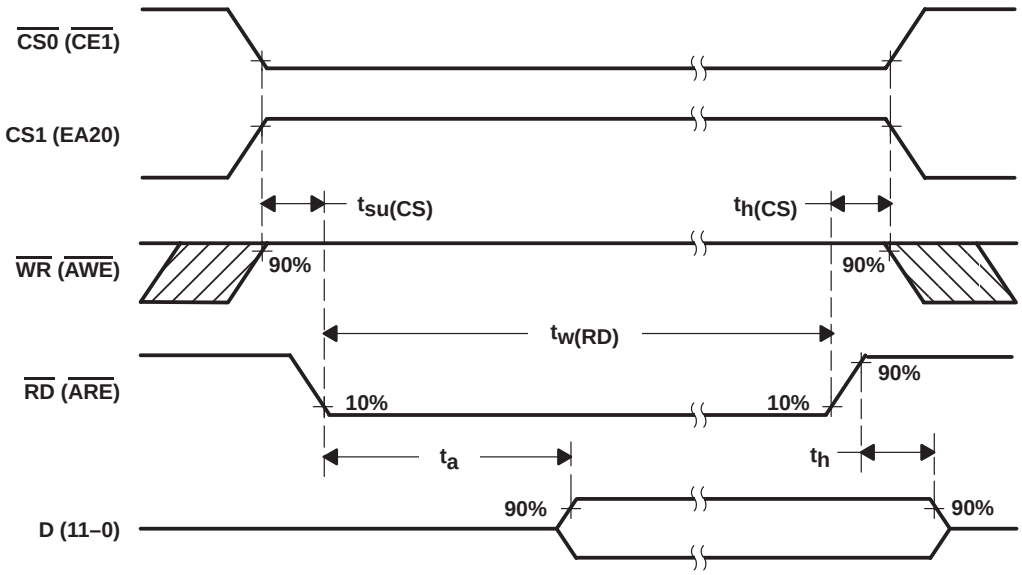

Figure 31. Read Access to the THS1206 (RD-ARE-Controlled)

Figure 31 shows the read timing diagram of the THS1206 based on an interface to the TMS320C6211. The data to be read from the THS1206 is latched into the TMS320C6211 with the rising edge of ARE. The data access (t_a) and hold time (t_h) of the THS1206 should be aligned with the TMS320C6211 *asynchronous memory read timing*. If the access time of the peripheral is too high, the timing should be adjusted. This adjustment is done from the TMS320C6211 by programming of internal wait states.

23 Summary

This application report describes the criteria applied in designing a system using the THS1206 high-speed data converter. The THS1206, with its 12-bit data bus and 6-MSPS conversion rate, is an analog-to-digital converter especially designed to operate with digital signal processors (DSP). The THS1206 features make it especially attractive in radar, high-speed data acquisition, communications, and control applications. The main features of the THS1206 are its four analog inputs which can be switched from sampling to hold mode simultaneously and its integrated FIFO which incresases the maximum data throughput between ADC and processor.

The report explains the initialization and operation of the THS1206. Two examples show the THS1206 connected to digital signal processors TMS320VC5402 and TMS320C6201. A discussion on different options to drive the analog input of the THS1206 is also included. Layout considerations offer hints on achieving the best system performance.

24 References

1. Texas Instruments, THS1206 data sheet, literature number SLAS217C
2. Texas Instruments, *Data Acquisition Circuits* data sheet, literature number SLAD001A
3. Texas Instruments, TMS320C6211 data sheet, literature number SPRS073A
4. Texas Instruments, TMS320VC5402 data sheet, literature number SPRS079D
5. Texas Instruments, Analog Applications, literature number SLYT005
6. Texas Instruments, Analog Applications Journal, literature number SLYT010
7. Texas Instruments, Electrostatic Discharge application note, literature number SSYA008
8. Texas Instruments, Selecting an Amplifier for a Data Converter, literature number SLOA035
9. Texas Instruments, Linear Design Seminar 1999, literature number SLYD016

25 Glossary

AC	Alternating current
ADC	Analog-to-digital converter
DC	Direct current
DSP	Digital signal processor
FIFO	Firt-in first-out
RF	Radio frequency
SFDR	Spurious free dynamic range
THD	Total harmonic distorsion
TL	Trigger level

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