Application Note

AM625/AM623 and AM62A7/AM62A3 Schematic Design and Review Checklist

TEXAS INSTRUMENTS

EP Processors MPU

ABSTRACT

This application note summarizes the design guidelines that are recommended to be followed by the board designers using AM625 / AM623 and AM62A7 / AM62A3 family of processors. The guidelines includes possible device configurations and care about for interfacing different processor peripherals to external devices.

Additionally links are provided for product pages, collaterals, FAQs and other common reference documents that could help the designers optimize the efforts during board design.

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Trademarks

1 Introduction

This document applies to the devices listed below. Product related documentation is available on the product pages available at each link.

1.1 AM62x Family of Devices

1.1.1 AM625

- AM6254 / AM6252 / AM6251

1.1.2 AM623

- AM6234 / AM6232 / AM6231

1.2 AM62Ax Family of Devices

1.2.1 AM62A7

This is a test of adding more content.

- AM62A74

1.2.2 AM62A7-Q1

- AM62A74-Q1

1.2.3 AM62A3

- AM62A34 / AM62A32 / AM62A31

1.2.4 AM62A3-Q1

- AM62A34-Q1 / AM62A32-Q1

2 Related Collaterals

2.1 Hardware Design Guide

2.1.1 AM625/AM623

For an overview about board design approach, see the *Hardware Design Guide for AM625 / AM623 Devices*.

A number of documents relevant to the selected device are available on the product folder page.

The below links summarizes the collaterals that could be referred when starting a custom design.

[FAQ] AM625: AM625 Custom board design – Collaterals to Get started

[FAQ] AM623: AM623 Custom board design – Collaterals to Get started

2.1.2 AM62A7 / AM62A3

For an overview about board design approach, see the *Hardware Design Guide for AM62A7 / AM62A3 Devices*.

A number of documents relevant to the selected device are available on the product folder page.

The below links summarizes the collaterals that could be referred when starting a custom design.

[FAQ] AM62A7 and AM62A7-Q1 Custom board design – Collaterals to Get started

[FAQ] AM62A3 and AM62A3-Q1 Custom board design – Collaterals to Get started

3 Device Selection

3.1 Data Sheet

For selecting the device variant, features, package (ALW/AMC/AMB), and speed grade, see the *Functional Block Diagram* and *Device Comparison* section of the device-specific processor data sheet.

3.2 Peripheral Instance Naming Convention

For naming the peripherals and instance, the device-specific TRM is generic, and the device-specific data sheet tends to be specific.

In the data sheet a suffix number is assigned even when there is only one instance, so any documents that reference the name will not need to change from device to device.

3.3 Device Ordering and Quality

For Ordering and quality information for the selected device, see the links below:

AM625-Ordering & quality

AM623-Ordering & quality

AM62A7-Ordering & quality

AM62A7-Q1-Ordering & quality

AM62A3-Ordering & quality

AM62A3-Q1-Ordering & quality

4 Power Architecture

For power management architecture, see the TI Power management web page.

In addition, WEBBENCH designer tools WEBBENCH designer tools provide a visual interface that delivers a complete power application.

4.1 Generating Supply Rails

The required supply rails for the selected processor can be generated using discrete or integrated power architecture.

Use of discrete architecture provides flexibility in device selection. Designer has to take care of the setting the output voltage, selecting the device that can source the required load current and sequencing the supplies.

Use of integrated power architecture simplifies processor specific power supply design.

The PMIC can control the supply sequencing so that meets the requirements of the processor during start-up. PMIC can also properly control the sequencing during shut-down as long as the properly powered up and functional.

Along with the PMIC, additional DC/DC converters and LDOs are used to generate the additional on-board supplies required for operation of other connect devices.

4.1.1 AM625 / AM623

For generating the required on board supply rails choose any of the below options.

4.1.1.1 PMIC (Power Management IC)

The TPS65219 PMIC is recommended for an integrated AM625 / AM623 power architecture. This space and cost optimized architecture is designed to power the processor and the principal peripherals.

For the full application note and operational details, see the *Powering the AM625 / AM623 with the TPS65219 PMIC*.

4.1.1.1.1 Additional Reference

For more information, see the listed section of the device-specific processor data sheet: *Device Connection and Layout Fundamentals*, *Power Supply* and *Power Supply Designs*.

4.1.1.2 Discrete Power

The alternate approach of generating the supply rails is discrete power architecture. This can be achieved by DC/DC converters and LDOs. The power sequence has to be managed using external logic.

For more information, see the *Discrete Power Solution for AM625 / AM623*.

4.1.1.2.1 DC/DC Converter

The DC/DC Converters such as TPS62826, LM61460-Q1 or similar can be used.

4.1.1.2.2 LDO

The LDOs such as TPS74518, TLV7103318, TLV75518 or similar can be used.

4.1.2 AM62A7 / AM62A3

4.1.2.1 PMIC (Power Management IC)

The TPS6593-Q1 PMIC is recommended for an integrated AM62A7 / AM62A3 power architecture. This space and cost optimized architecture is designed to power the processor and the principal peripherals.

For implementation, see the *Starter Kit SK-AM62A-LP EVM* schematic.

4.2 Power Management

4.2.1 Load Switch

Load Switches can be used to turn on and off a specific sub-systems powered by the same supply instead of using multiple DC/DC converters or LDOs to generate the same supply. In some systems, there is a strict power-up/down sequence that must be followed. Load switches simplifies the implement power sequencing to meet the power-up/down requirements.

In PMIC based power architecture, the load switch must be enabled by the PMIC to comply with the processor power sequencing requirements. The PMIC GPIO used to control the load switch depends on the PMIC part number used.

The Load switches such as TPS22965, TPS22918, TPS22902, TPS22946 or similar can be used.

5 General Recommendations

As you are creating the schematics for your project here are a few recommendation and guidelines to be aware.

5.1 Processor Performance Evaluation Module (EVM)

Processor (hardware) performance evaluation platforms (EVM) are not considered to be a reference design. They are evaluation platforms and may not represent a proper system implementation. In many cases, the EVMs are partially or completely designed before the processor is released for fabrication. This is done so the hardware platform is available when first silicon arrives. It is possible to learn new device requirements during processor bring-up and bench validation. If so, these new requirements may not be accounted for in the hardware evaluation platform. Therefore, TI expects customers to carefully review and follow all requirements defined in the device-specific data sheet, silicon errata, and TRM when designing their system.

The hardware development platforms were not designed to be comprehensive of specific system requirements, like radiated emissions, noise susceptibility, thermal management, and so forth.

5.2 EVMs Versus Data sheet

During evaluation or the board design, in case of any discrepancy between the device-specific TI EVMs and the processor data sheet, always follow the data sheet. Despite the best efforts by the designer, the EVMs may contain errors that still function but are not completely aligned with the data sheet specification. Therefore, the EVM designs can not be considered as reference designs and reviewed before reuse.

5.2.1 Notes About Component Selection

The EVM components selection may not be the most optimized. Review the BOM to optimize the component selection based on the board design and application requirements.

Design calculations, review and testing is recommended to be performed before finalizing the components value and ratings.

5.2.1.1 Series Termination

The recommended value for the series termination resistor is simply a starting point for designers that should be verified by making sure the step function that occurs on this pin is not near mid-supply. The board designer needs to understand the functioning of the peripheral and the associated risks to select the appropriate value based on their specific PCB implementation.

5.2.1.2 Parallel Termination

Provisioning for parallel terminations and the termination values are based on the pin connectivity recommendations, recommendations for improved processor performance, based on relevant interface requirements or standards and are also based on the EVM implementation when standards or requirements for the interfaces are not available.

EVM values can be used as starting point and designers can choose the appropriate pull values based on their specific PCB implementation.

5.2.1.3 External ESD Protection

Provide provision for an external ESD protection is required if any of the processor I/O is connected to an external connector, since internal ESD protection devices were not designed to handle the system level ESD requirements.

5.2.2 Additional Information

The below links summarizes the considerations designers have to be familiar when reusing TI EVM design files while designing custom board.

[FAQ] AM625 or AM623 Custom board hardware design - Reusing TI EVM design files.

[FAQ] AM62A7 or AM62A3 Custom board hardware design - Reusing TI EVM design files.

5.3 Before You Begin The design

5.3.1 Documentation

Make sure you use the latest version of the documentation, example the device-specific data sheet, TRM, silicon errata and other design collaterals.

Documentation search Tips: Try searching the documentation for words such as: "must", "require", "do not", "shall", "note", "pin connectivity" and so forth. Important criteria for the device typically contains one or more of these words. This is an easy way to make sure you have not missed anything important.

Being updated Tips: On Ti.com, device product folder page, there is an "Alert me about changes to this product" button. Registering here enables automatic notification of device document changes.

5.3.2 Processor Pinout Verification

Designer must check the below implementation before starting the detailed design.

- Verify the processor pin labels correspond to the correct pin numbers mentioned in the data sheet pin attributes section.
- Verify the supply voltages connected to the processor power pins are withing the recommended range.
- All the pins of the processor (grouped into functions and having separate symbol blocks) are shown in the schematics to minimize tool related and functional errors.
- Most of the processor I/Os are turned off by default and external pull resistors may be required to hold inputs of any attached device in a valid logic state until software initializes the I/Os.
- All Reserved pins of the processor, must be left unconnected (do not connect signal traces/test points to these device balls).
- Any processor pad/pin that has a trace connected and not used, recommended to terminate with pullup/ pulldown resistor.
- For performance improvement consider implementing external voltage, current or temperature monitoring.

5.3.2.1 Verification of Unused Processor Pins

For specific connectivity guidance on certain unused processor pins or interfaces, see the *Pin Connectivity requirements* section of the device-specific processor data sheet.

It should be okay to leave any unused pin that does not have a special requirement mentioned in the pin connectivity section unconnected.

5.3.3 Peripheral Instance Naming

We try to assign a suffix number even when there is only one instance so any documents that reference the name will not need to change from device to device. There could be some exceptions. For example, the USB power rails may not have a suffix if the device has two USB ports and the power rails are shared by both ports.

We typically start with a suffix of “0”. For the CPSW3G port names, port “0” is the internal (third) port on the switch.

5.3.4 Processor Related Queries and Clarifications

For queries and clarifications related to processor selection and features, use the TI E2E forum. E2E can be used to ask a new question or refer to related questions that have been answered.

6 Processor (AM625 / AM623 and AM62A7 / AM62A3) Specific Recommendations

6.1 Common (Processor Start-Up) Connection

6.1.1 Power Supply

Follow the recommendations listed below:

- The power requirement for each supply rail varies based on the interfaces used and the operating environment. Power requirements must be determined using the power model and the supply rails are required to be rated for the required power with margin.
- The maximum current draw of all processor supply rails can be estimated using the *PET (Power Estimation Tool)*. If the outputs from the selected power architecture powers other on-board peripheral devices, the maximum current draw of these devices needs to be included.
- Check if the current capabilities of the selected power architecture including PMIC, DC/DC converters and LDOs meet the maximum demand of all devices that are attached and recommended to consider some additional margin for design variances.
- Check if the recommended power supply sequence is followed. Proper power supply sequencing in correlation with resets and clocks is required. For the recommended power sequencing requirements, see the device-specific processor data sheet.

6.1.1.1 Supplies for Core and Peripherals

For proper operation, all power pins (balls) must be supplied with the supply voltages specified in the *Recommended Operating Conditions* section of the device-specific processor data sheet. VDDS_OSC0, VDDA_MCU and CAP_VDDS_MCU need to be always connected. 0.75 V/0.85 V can be connected to the VDD_CORE supporting performance or supply rail optimization.

Dynamic supply voltage scaling on VDD_CORE is not supported.

For more information, see the *Recommended Operating Conditions* table and *Power Sequencing* section of the device-specific processor data sheet.

Processor contain multiple analog power pins that provide power to sensitive analog circuitry like PLLs, OLDI (AM625 / AM623), USB, CSI, and so forth. These must be attached to filtered power sources.

6.1.1.2 Supply for I/O Groups

The processor includes up-to nine dual-voltage I/O domains, where each domain provides power supply to a fixed set of I/Os. Each I/O power domain can be connected to 3.3 V or 1.8 V, which determines a common operating supply voltage for the entire set of I/Os. All signals connected to these domains must operate from the same power supply source that is being used to power the respective VDDSHVx supply rail. Unless specified the processor buffers are not failsafe.

The supply pins designated as CAP_VDDSx [x=0-6], CAP_VDDS_CANUART, CAP_VDDS_MCU are available for connecting the capacitors to internal LDOs. These pins must always be connected via a 1-µF capacitor and the other pin of the capacitors are connected to VSS. Output supply voltage level for these pins are 1.8 V + 10% (1.98 V max). Check if the selected capacitor has ESR less than 0.8 Ω and PCB connectivity loop inductance is less than 1.5-nH.

Note

The supply voltage for the VDDSHVx supply rail must be present before any supply voltage is applied to the associated I/Os. All VDDSHVx supplies and the I/O supply caps must be connected even if the associated I/Os are not used.

6.1.1.3 Supply for eFuse ROM Programming (VPP)

It is very important for the processor eFuse ROM programming supply (VPP) to remain in the Recommended Operating Condition (ROC) range during eFuse programming. An LDO powered from a higher voltage supply is recommended because the LDO will be able to compensate for the voltage drop through its series pass transistor and maintain the correct operating voltage during the high current transients. Local bulk capacitors are likely needed near the VPP pin to assist the LDO transient response. Using a FET as a switch or Load switch to source the VPP pin from a fixed 1.8 V supply can be problematic due to the high current transient. The VPP implementation is recommended to be characterized to ensure the processor VPP pin never drops below the min ROC value.

6.1.1.4 Supply Connection When Partial I/O (Low Power Mode) Configuration is Used

Check VDD_CANUART and VDDSHV_CANUART power supply connection when Partial I/O (low power mode) is used. For more information, see the *Recommended Operating Conditions* table in the device-specific processor data sheet.

VDD_CANUART shall be connected to the same power source as VDD_CORE and VDDSHV_CANUART shall be connected to any valid I/O power supply when not using Partial I/O.

6.1.1.5 Additional Information

Check if 0 Ω resistors or ferrite beads in line with the core and other supply rails on the board are placed.

Placement of 0 Ω resistors or ferrite beads in line with the core and other supply sections are recommended for initial PCB prototype builds. Placement of ferrite beads provides a filtered supply. This helps during board bring-up and debug to isolate the supply or measure current. Current measurement is the purpose of these resistors in the EVM.

Note that the implementation of these resistors adds inductance and resistance.

6.1.2 Capacitors for Power Supply Rails

6.1.2.1 AM625/AM623

Ensure the required PDN analysis has been performed, and the required number of decoupling and bulk capacitors have been provided for all the power supply rails including the Dual-voltage I/O supply rails.

Place the decoupling capacitors as close as possible to the supply pins. Larger bulk caps can be placed further away.

Use low ESL capacitors and mount them with shortest possible traces to keep the mounting inductance low. For more information, see the *Sitara Processor Power Distribution Networks: Implementation and Analysis*.

The bulk and decoupling capacitors values from the EVM can be used as a reference when PDN analysis is not available.

6.1.2.2 AM62A7 / AM62A3

To optimize the processor performance mainly the increased DDR performance, Feedthrough (3-terminal) capacitors are used (SK-AM62A-LP).

3-terminal capacitors minimizes the loop inductance and help optimizes the number of power supply capacitors used.

6.1.2.3 Additional Information

When any of the processor peripherals (Camera Serial interface (CSI-Rx), DDR Subsystem (DDRSS) and Two USB 2.0 Ports) are not used, it is recommended to connect the relevant supply pins to VSS.

If boundary scan is required, connect Camera Serial interface (CSI-Rx) supply pins to the relevant supply voltage.

For more information, see the *Pin Connectivity Requirements* section of the device-specific processor data sheet.

6.1.3 Processor Clock

6.1.3.1 Clock Inputs

6.1.3.1.1 High Frequency Oscillator (MCU_OSC0_XI/ MCU_OSC0_XO)

A clock source is required to be connected to the MCU_OSC0_XI for proper operation of the processor.

Select a 25 MHz crystal or clock source. All discrete components used to implement the oscillator circuit must be placed as close as possible to the MCU_OSC0_XI and MCU_OSC0_XO pins. For the crystal, the load capacitance selected is required to be in the range recommended in the *MCU_OSC0 Crystal Circuit Requirements* table of the device-specific processor data sheet.

6.1.3.1.2 Low Frequency Oscillator (WKUP_LFOSC0_XI/ WKUP_LFOSC0_XO)

Use of WKUP_LFOSC0 is optional, depending on the system requirements.

Select a 32.768 kHz crystal or clock source. All discrete components used to implement the oscillator circuit must be placed as close as possible to the WKUP_LFOSC0_XI and WKUP_LFOSC0_XO pins. For the crystal, the load capacitance selected is required to be in the range recommended in the *WKUP_LFOSC0 Crystal Electrical Characteristics* table of the device-specific processor data sheet.

If WKUP_LFOSC0_XI/ XO is not being used:

- XI is recommended to be connected directly to VSS
- XO is recommended to be left unconnected

For more information, see the *WKUP_LFOSC0 Not Used* section of the device-specific processor data sheet.

6.1.3.1.3 EXT_REFCLK1 (External Clock Input to Main Domain)

EXT_REFCLK1 clock pin is routed to clock muxes as one of the selectable input clock source to the Timer modules (DMTIMER/WDT), DMTIMER in Security Subsystem (SMS), MCAN and CPTS (Time Stamping Module). If an application needs a specific clock frequency to be fed to these modules then they have an option to use the EXT_REFCLK1 (for example: time synchronization or for clock quality reasons).

6.1.3.2 Clock Outputs

The I/O pins CLKOUT0 and WKUP_CLKOUT0 can be configured as clock output. The clock output can be used as clock source for the attached devices (Ex: Ethernet PHY). WKUP_CLKOUT0 is a buffered output of the high frequency oscillator HFOSC0 available during power-up as default.

6.1.4 Processor Reset

6.1.4.1 Reset Input

MCU_PORz is the MCU Domain cold reset input to the processor. MCU_PORz is recommend to be pulled low during the supply ramp and oscillator start-up. Follow the recommended MCU_PORz reset timing requirement in the power-up Sequencing diagram of the specific processor data sheet.

For MCU_PORz, a 3.3 V input can be applied, but the input thresholds are still a function of the 1.8 V I/O supply voltage (VDDS_OSC0).

Terminate MCU_RESETz and RESET_REQz signals as per the *Pin Connectivity Requirements* section of the device-specific processor data sheet.

6.1.4.2 Reset Status Output

Status outputs PORz_OUT is the Main Domain POR status output and RESETSTATz is the Main Domain warm reset status output.

RESETSTATz can be used to reset on board memories with reset functionality (eMMC, OSPI, Boot mode) or SD Card power switch. The PORz_OUT can be used to latch the configurations during power-up including Ethernet PHY pin strap configurations.

Terminations (pulldown) are recommended for PORz_OUT and RESETSTATz outputs to assert the reset for the attached devices.

6.1.4.3 Additional Information

The MCU_PORz must meet the timing requirements (with respect to the supply ramp) and must be held low during supply ramp and sequencing.

The inputs that are used to configure the processor boot (BOOTMODExx inputs) must be held in the desired known state to select the appropriate boot mode as defined in the device-specific TRM, until after the rising edge of the MCU_PORz.

The system may contain other devices that require bootstrap configurations, for example, Ethernet PHYs. External pull resistors may need to be used for all such pins, depending on availability of internal terminations or device recommendation.

6.1.5 Configuration of Boot Modes

Boot mode inputs do not have internal pullup or pulldown resistors that are active during power-up and reset. External terminations (pullup/pulldown) must be used to set the boot mode.

If dip switches are used, it is recommended to use a resistor divider ratio of 470 Ω (pullup) and 47 kΩ (pulldown) for improved performance.

If dip switch is not used, recommended to use a standard resistor (same value for pullup or pulldown) value Ex: 4.7 kΩ or 10 kΩ since either a pullup or pulldown resistor is used for improved noise performance.

Boot mode pins marked as Reserved or not used must not be left floating and are recommended to be terminated (pullup or pulldown).

It is recommended to add provision for pullup and pulldown resistors for all the boot mode pins for design flexibility and future enhancement.

Based on the application a buffer that is only driven when reset is active can be used to present the boot configuration to the processor.

If the processor I/Os is configured as an output during normal operation, a series resistor to limit the buffer current is recommended, see the device-specific EVM.

6.1.5.1 Boot Mode Isolation Buffers Use Case and Optimization

In the EVM, the 16 boot mode pins Bootmode[15:00] are asserted through two buffers (isolation buffers). The isolation buffers ensure that SYSBOOT pulls (boot mode configured using resistors) are controlling the level of the signals when the boot mode signals are being latched (around the PORz_OUT rising edge) by the processor. Since boot mode signals are often used for other functions beyond reset and are connected to other devices, they need to be isolated from other connected peripherals so that those peripherals do not conflict with the intended boot mode configuration (signal levels).

The buffers are enabled only when PORz_OUT is driven low by the processor. After PORz_OUT goes high, the buffer outputs are Hi-Z so the signals are not pulled up or down by the boot mode resistors.

When the buffers are used, a series resistor (around 1 kΩ) is recommended for protection (to limit the sink current) of the buffer.

For optimizing the design and BOM cost, these buffers can be omitted depending on the use case. The boot mode pull resistor values can be selected so that they do not affect the operation of attach devices.

Provision for pullup and pulldown resistors on every boot mode pin are recommended for debugging. Only populate pullup or pulldown per boot mode pin.

6.1.5.2 Bootmode Selection

For configuring the bootmode, see the *ROM Code Boot Modes* table in the *Initialization* chapter of the device-specific TRM.

6.1.5.2.1 Note About USB Boot Mode

USB0 interface supports boot. When the USB0 is configured for DFU boot mode, supply of 3.3 V (permanent or switched) is not recommended to be connected to the USB0_VBUS pin. No permanent supply (equivalent to the divider value) is allowed to be connected to the USB0_VBUS.

A 5 V supply from the host (switched) connected through the USB connector (or similar) is recommended to be connected to the device through the voltage divider as per the device-specific data sheet recommendations. The Zener diode could be removed and a 20 kΩ resistor could be substituted for the 16.5 kΩ and 3.5 kΩ resistors if your system will never apply a VBUS potential greater than 5.5 V.

6.1.5.3 Additional Information

The Main Domain POR status output (PORz_OUT) can be used as an enable signal for any boot mode buffers on signals that are also used for I/O. If the I/O pins associated with boot mode inputs are redefined for another signal function during operation, these I/Os must be released and set back to the proper levels to select the boot mode whenever the processor enters the cold reset state. This problem occur when an external device attempts to drive the boot mode signals.

When using Ethernet Boot and RGMII: design must implement a PHY that enables RGMII_ID mode on the PHY RX data path and disables RGMII_ID mode on the TX data path by default (the processor implements RGMII_ID on the TX channel). The processor ROM is PHY agnostic and will not programmatically enable/ disable RGMII_ID mode on attached PHYs. Typically, this is accomplished via pin strapping on the PHY.

Select a Ethernet PHY with capability to set the RGMII internal TX delay through pin strap, see the devie-specific EVM. For more information, see the advisory *i2329 MDIO: MDIO interface corruption (CPSW and PRU-ICSS)* of the device-specific Errata.

6.2 JTAG and EMU for Debug

JTAG and EMU are not used

For configuring the JTAG and EMU signals, see the *Pin Connectivity Requirements* section of the device-specific processor data sheet.

JTAG and EMU are used

Terminate EMU0, EMU1, TDI, TCK, TMS & TRSTn signals as per the *Pin Connectivity Requirements* section of the device-specific processor data sheet.

It is recommended to connect to a Series termination (22 Ω) on the TDO (close to processor pin) signal. An external ESD protection is recommended for all JTAG and EMU signals when the signals are connected to an external connector.

6.2.1 Additional Information

During board design, TI recommends provisioning at least a minimal JTAG port connected to test points or a header footprint to support early prototype debugging. JTAG component footprints can be DNI in the production version of the board, if desired.

Clock and signal buffering are required whenever the JTAG interface connects to more than one device. Clock buffering is strongly recommended even for single device implementations. For implementation, see the device-specific EVM.

If trace operation is needed, the TRC_x signals must be connected to the emulation connector. All TRC_x signals are pin-muxed with other signals. If the trace connections are needed, the connections for GPMC interface can not be used. Routes for TRC_x signals used for trace must be short and skew matched. Trace signals are on a separate power domain, VDDSHV3, and can be at a different supply voltage from the other JTAG signals. For more recommendations on TRC/EMU routing, see the *Emulation and Trace Headers Technical Reference Manual*. A similar summary of this information is available at *XDS Target Connection Guide*.

If boundary scan is required, the EMU0/1 pins must be directly connected to the JTAG connector.

To ensure a proper implementation of the JTAG interface, see the *Emulation and Trace Headers Technical Reference Manual* and the *XDS Target Connection Guide*.

7 Processor Peripherals

7.1 Supply Connections for I/O Groups

The processor includes nine dual-voltage I/O domains (VDDSHVx [x=0-6], VDDSHV_MCU and VDDSHV_CANUART). Each domain provides power to a fixed set of I/Os. Each I/O domain is required to be connected to 3.3 V or 1.8 V during power-up.

VDDSHV4, VDDSHV5, and VDDSHV6 were designed to support power-up, power-down, or dynamic supply voltage change without any dependency on other supply rails. This capability is required to support UHS-I SD Cards.

7.2 Memory Interface (DDR4, LPDDR4, MMCSD (eMMC/SD/SDIO), OSPI/QSPI and GPMC)

7.2.1 DDR Subsystem (DDRSS)

7.2.1.1 DDR4

7.2.1.1.1 AM625/AM623

For implementation guidelines, see the *AM625 / AM623 DDR Board Design and Layout Guidelines*.

For implementation examples and termination values, see the device-specific EVM.

7.2.1.1.1.1 Configuration

The allowed device configurations are 1 X 16-bit or 2 X 8-bit. 1 X 8-bit device configuration is not a valid configuration.

7.2.1.1.1.2 Routing Topology and Terminations

When a single device is used (1 X 16-bit), follow the Point-to-Point routing topology.

- VTT terminations may not be required for address and control signals.
- Terminations (2 X R (value=Zo) and a filter capacitor connected to the center of two resistors and VDDS_DDR (DDR PHY IO supply)) are recommended for CKp, CKn (differential clock) signals.
- The reference voltage (VDDS_DDR/2) for the device can be generated using resistor divider (value 1 kΩ, 1%) with decoupling capacitor connected across both the resistors and additional decoupling capacitors connected near to the device VREFCA.
- Adding VTT termination for a single device on the address and control signals, is an acceptable approach.

When two devices are used (2 X 8-bit), follow the Fly-by routing topology.

- External terminations for address, control and clock signals are required.
- An LDO with capability to Sink/Source the current is recommended to generate the VTT termination voltage.
- The reference voltage (VDDS_DDR/2) for the device can be obtained from LDO with decoupling capacitor connected to ground.

7.2.1.1.1.3 Signals Termination and Calibration Resistors

Provide terminations (pulldown) for DDR0_RESET0_n (DDRSS Reset), DDR_TEN (test enable) and CKE (optional clock enable) and termination (pullup) for DDR_ALERTn close to device pins.

Provide calibration resistors for DDR0_CAL0 (close to processor pin) and ZQn (n=0..1, close to device pin/s). Use 1% tolerance resistors.

7.2.1.1.1.4 Capacitors for the Power Supply Rails

Provide adequate bulk and decoupling capacitors on the DDR supply rails for both the AM625/AM623 processor as well as the DDR4 device. For more information, see the device-specific EVM.

7.2.1.1.1.5 Data Bit or Byte Swapping

During the design in case bit swapping is required, bit swaps within a data byte, and swapping of byte 0/1 are supported. Address bit swapping is not supported. For more information, see the *Bit Swapping* section of *AM625 / AM623 DDR Board Design and Layout Guidelines*.

The bit swapping changes are required to be updated in the schematics.

7.2.1.1.2 AM62A7 / AM62A3

Currently Not Supported.

7.2.1.2 LPDDR4

7.2.1.2.1 AM625/AM623

For implementation guidelines, see the *AM625 / AM623 DDR Board Design and Layout Guidelines*.

For implementation examples and termination values, see the device-specific EVM.

7.2.1.2.1.1 Configuration

The allowed device configuration is 1 X 16-bit. For more information, see the *LPDDR4 Device Implementations Supported* section of *AM625 / AM623 DDR Board Design and Layout Guidelines*.

7.2.1.2.1.2 Routing Topology and Terminations

The CK and ADDR_CTRL routing topologies are point-to-point.

The data line topology is always point-to-point for LPDDR4 implementations, and is broken up into different byte lanes.

Terminations are not required to be provided on the board for the address/control bus of the LPDDR4 configuration. All termination is handled internally (on-die). Thus, VTT supply and terminations are not required.

7.2.1.2.1.3 Signals Termination and Calibration Resistors

Provide termination for DDR0_RESET0_n (close to device pin).

Provide calibration resistors for ODT_CA_A..B (close to device pins), DDR0_CAL0 (close to processor pin) and ZQn (n=0..1, close to device pin/s). Use 1% tolerance resistors.

7.2.1.2.1.4 Capacitors for the Power Supply Rails

Provide adequate bulk and decoupling capacitors on the DDR supply rails for both the AM625 / AM623 processor as well as the LPDDR4 device. For more information, see the device-specific EVM.

7.2.1.2.1.5 Data Bit or Byte Swapping

During the design in case bit swapping is required,bit swaps within a data byte, and swapping of byte 0/1 are supported. Address bit swapping is not supported.

The bit swapping changes are required to be updated in the schematics.

7.2.1.2.2 AM62A7 / AM62A3

For implementation guidelines, see the *AM62A7 / AM62A3 DDR Board Design and Layout Guidelines*.

For implementation examples and termination values, see the device-specific EVM.

7.2.1.2.2.1 Configuration

The allowed device configuration is 1 X 32-bit or 1 X 16-bit. 1 X 8-bit configuration is not a valid configuration. For more information, see the *LPDDR4 Device Implementations Supported* section of *AM62A7 / AM62A3 DDR Board Design and Layout Guidelines*.

7.2.1.2.2.2 Routing Topology and Terminations

When a 32-Bit, Single-Rank/Dual-Rank LPDDR4 is used, follow Balanced 'T' Topology routing for Address, CKE and CK signals.

When a 16-Bit, Single-Rank LPDDR4 is used, follow the point-to-point topology. Terminate the other Data strobe pins (DDR0_DQS2..3 and DQS2..3_n) as per the *AM62A7 / AM62A3 DDR Board Design and Layout Guidelines* recommendation.

The data line topology is always point-to-point for LPDDR4 implementations, and is broken up into different byte lanes.

Terminations are not required to be provided on the board for the address/control bus of the LPDDR4 configuration. All termination is handled internally (on-die). Thus, VTT supply and terminations are not required.

7.2.1.2.2.3 Signals Termination and Calibration Resistors

Provide termination for DDR0_RESET0_n (close to device pin).

Provide calibration resistors for ODT_CA_A..B (close to device pins), DDR0_CAL0 (close to processor pin) and ZQn (n=0..1, close to device pin/s). Use 1% tolerance resistors.

7.2.1.2.2.4 Capacitors for the Power Supply Rails

Provide adequate bulk and decoupling capacitors on the DDR supply rails for both the AM62A7 / AM62A3 processor (including Three-terminal capacitors) as well as the LPDDR4 device. For more information, see the device-specific EVM.

7.2.1.2.2.5 Data Bit or Byte Swapping

During the design in case bit swapping is required, bit swaps within a data byte, and swapping across bytes is not supported. Address and control bit swapping is not supported.

For more information, see the *Channel, Byte, and Bit Swapping* section of *AM62A7 / AM62A3 DDR Board Design and Layout Guidelines*.

The bit swapping changes are required to be updated in the schematics.

7.2.2 MMCSD (Multi-Media Card/Secure Digital)

The processor includes three MMCSD instances. The MMCSD Host Controller provides an interface to 1x eMMC (8-bits) and 2x SD/SDIO (4-bits) instances.

7.2.2.1 MMC0 - Embedded Multi-Media Card (eMMC) Interface

Review the below implementations. For implementation (when specific recommendations are not available) examples and termination values, see the device-specific EVM.

For more information, see the *MMC0 - eMMC/SD/SDIO Interface* section of the device-specific processor data sheet.

7.2.2.1.1 I/O Power Supply

The MMC0 interface of the processor is powered by the VDDSHV4 Dual-voltage I/O supply.

VDDSHV4 supports power-up, power-down, or dynamic supply voltage change without any dependency on other supply rails.

Same supply rails required to be connected to VDDSHV4 and I/O supply rail of the attached device.

VDD (core) of the eMMC device can be powered from an independent supply rail.

7.2.2.1.2 Reset

It is recommended to Implement the reset logic using Dual input AND gate. One of the AND gate input is controlled by processor general purpose input/output (GPIO) pin. Terminate the AND gate input using pullup connected to the specific I/O domain supply voltage. The other input of the AND gate can be the Main Domain warm reset status output (RESETSTATz) Signal.

In case an ANDing logic is not used and the processor reset status output is used directly to reset the attach devices, ensure the I/O levels of the attach device match the processor I/O level or use a level translator to match the levels.

7.2.2.1.3 Signals Termination

Provide the following terminations:

- Provide provision for external terminations (pullup) for the data lines (DAT0:7) connected to the peripheral specific dual I/O supply rail. Depending on the terminations available internal to the attach device, populate the terminations. To start with, populate terminations for DAT0 and DNI the other data lines terminations.
- Provide a series termination (0 Ω) (close to processor pin) and an external termination (parallel) for MMC0_CLK (pulldown), CMD pin (pullup) and DS pin (pulldown) close to the device.

7.2.2.1.4 Capacitors for the Power Supply Rails

Check if required bulk and decoupling capacitors have been provided for the processor I/O supply rail (VDDSHV4) and the attached device.

Follow the device-specific EVM implementation whenever recommendations are not available.

7.2.2.1.5 Additional Information

The MMC0_CLK pin is internally configured to operate as a clock output and clock input simultaneously. A series resistor may be required to resolve any signal distortion that occurs on the source end of the signal trace (may cause the MMC0_CLK input buffer to see false clock transitions).

Note

There could be implementation difference in the eMMC Controller and PHY IPs used on different processors families. Pay special attention on the interface including terminations when migrating to a different processor family.

It is recommended to review the device-specific data sheet, TRM, and following the termination recommendations for the device-specific processor family and attached device.

EVM implementation can be followed as required.

7.2.2.2 MMC0 – Secure Digital (SD) Card Interface

The CD and WP pins are not available on MMC0 interface. This can be used to interfaces with fixed SDIO devices (not removable). Fore more information, see the *MMC0 - eMMC/SD/SDIO Interface* section of the device-specific processor data sheet.

7.2.2.3 MMC1 / MMC2 – Secure Digital (SD) Card Interface

Review the below implementations. For implementation (when specific recommendations are not available) examples and termination values, see the device-specific EVM.

For more information, see the *MMC1/MMC2 - SD/SDIO Interface* section of the device-specific processor data sheet.

7.2.2.3.1 I/O Power Supply

The MMC1 and MMC2 interfaces of the processor are powered by the VDDSHV5 and VDDSHV6 Dual-voltage I/O supplies respectively.

VDDSHV5 and VDDSHV6 support power-up, power-down, or dynamic supply voltage change without any dependency on other supply rails. VDDSHV5 and VDDSHV6 supplies must always default to 3.3 V and allow changing to 1.8 V when software is ready to change the supply voltage of the interface signals.

The MMC1_SDCD and MMC1_SDWP pins are powered from the VDDSHV0 Dual-voltage I/O supply and does not allow dynamic supply voltage switching. The MMC2_SDCD and MMC2_SDWP pins are powered from the VDDSHV6 Dual-voltage I/O supply.

It is recommended to use separate LDO or supply rail for I/O group supplies configured for SD Card interface.

The I/O supply voltage for the SD Card interface can be either 1.8 V or 3.3 V. Connect a fixed 3.3 V supply rail to the SD card supply. The supply of SD Card must remain at 3.3 V even for the UHS-I modes of operation. Only the signaling levels change in these modes.

All external termination (pullup) connected to the SD Card signals must be connected to the same power source that powers I/O supply rails (Ex: VDDSHV5 for MMC1).

If MMC1 (SD Card boot) is configured as a boot device ensure that the external power switch sourcing the SD Card defaults to ON (powered state) to ensure the SD Card is powered during boot.

7.2.2.3.2 Reset

It is recommended to have a software controlled 3.3 V power switch that sources the SD Card power supply. The power switch allows power to be cycled to the SD Card since this is the only way to reset the SD Card and place it back into its default state.

The SD Card enable logic can be implemented using a three input AND gate connected to Main Domain POR status output (PORz_OUT), Main Domain warm reset status output (RESETSTATz) and processor GPIO. Terminate the AND gate input connected to the processor GPIO using a termination (pullup) connected to the specific I/O domain supply voltage. Provide provision to isolate the GPIO input to the AND gate.

The I/O supply rails used for SD Card interface are required to be configured to default 3.3 V along with the SD Card reset. The output of the AND gate (Power switch enable) can be used to reset the I/O group supply.

for the implementation details, see the device-specific EVM.

7.2.2.3.3 Signals Termination

Provide the following terminations:

- Provide provision for external terminations (pullup) for the data lines (DAT0:3) CD and CMD signals connected to the peripheral specific dual I/O supply rail close to the SD card socket.
- Provide a series termination (0 Ω) for MMC1_CLK and MMC2_CLK (close to processor pins) and an external termination (pulldown) for MMC1_CLK and MMC2_CLK signals (close to device or SD card).

7.2.2.3.4 Protection

An external ESD protection is recommended for data, clock, and control signals (Internal ESD protection devices were not designed to handle the system level ESD requirements).

7.2.2.3.5 Capacitors for the Power Supply Rails

Check if required bulk and decoupling capacitors are provided for the processor I/O supply rail (VDDSHV5/ VDDSHV6) and the device.

Follow the device-specific EVM implementation whenever recommendations are not available.

Note

Follow the device-specific recommendations for data and control interface termination. It is recommended to place the series termination for the clock output close to processor pin.

7.2.2.4 Additional Information

For the implementation details, see the notes in the *Signal Descriptions, MMC, MAIN Domain* section of the device-specific processor data sheet.

7.2.3 Octal Serial Peripheral Interface (OSPI) and Quad Serial Peripheral Interface (QSPI)

For more information, see the *OSPI/QSPI/SPI Board Design and Layout Guidelines* section of the device-specific processor data sheet. For implementation examples and termination values, see the device-specific EVM.

Review the below implementations.

7.2.3.1 I/O Power Supply

The OSPI / QSPI interface of the processor is powered by the VDDSHV1 Dual-voltage I/O supply.

Same supply rail required to be connected to VDDSHV1 of processor and I/O supply rail of the device.

7.2.3.2 Reset

It is recommended to Implement the reset logic using Dual input AND gate. One of the AND gate input is controlled by processor general purpose input/output (GPIO) pin. Terminate the AND gate input using pullup connected to the specific GPIO I/O domain supply voltage. The other input of the AND gate can be the Main Domain warm reset status output (RESETSTATz) Signal.

In case an ANDing logic is not used and the processor reset status output is used directly to reset the attach devices, ensure the I/O levels of the attach device match the processor I/O level or use a level translator to match the levels.

7.2.3.3 Signals Termination

Provide the following terminations:

- Provide provision for external terminations (pullup) for the data lines (DAT0:7) connected to the peripheral specific dual I/O supply rail close to the processor. Depending on the terminations available internal to the attach device, populate the terminations. To start with DNI the terminations on the Data lines (D0:7).
- Provide a series termination (22 Ω) (close to processor pin) and an external termination (parallel) for OSPI0_CLK (pulldown), CS pin (pullup) and INT# pin (pullup) close to the device.

7.2.3.4 Loopback Clock

Check the loopback clock configuration. Different configuration of clock loopback can be made using OSPI0_LBCLKO (OSPI Loopback Clock Output) and OSPI0_DQS (OSPI Data Strobe or Loopback Clock Input). For the following configurations, see the device-specific data sheet:

- *No Loopback, Internal PHY Loopback, and Internal Pad Loopback*

External Board Loopback

Processor OSPI Data Strobe (DQS) or Loopback Clock is used along with the DS data strobe of OSPI Octal SPI

If DS (Read Data Strobe) pin is available in the device, connect the DS pin of the device to the OSPI0_DQS pin of the processor. OSPI0_LBCLKO pad can not be connected to any PCB traces.

If DS is available or not used, to configure the external loopback, connect the OSPI0_LBCLKO output pin of the processor to the OSPI0_DQS input pin of the processor

If External Loopback is not used, the OSPI0_LBCLKO and OSPI0_DQS pads can not be connected to any PCB traces.

Note

D0 and D1 of the processor OSPI peripheral must be connected to D0 and D1 of the QSPI / OSPI memory to support legacy x1 commands. Data bit swapping is not allowed.

7.2.3.5 Interface to Multiple Devices

It is recommended to connect the OSPI (processor) to a single device memory. In case the OSPI is interfaced to multiple devices, the interface would create a split data bus which could severely degrade signal integrity at high speeds. For accessing OSPI at high speeds, a point to point data bus is required.

7.2.3.6 Capacitors for the Power Supply Rails

Check if required bulk and decoupling capacitors are provided for the processor I/O supply rail (VDDSHV1) and the device.

Follow the device-specific EVM implementation whenever recommendations are not available.

7.2.4 General-Purpose Memory Controller (GPMC)

Review the below implementations. Follow the device-specific EVM for implementation examples and termination values.

7.2.4.1 I/O Power Supply

The GPMC interface of the processor is powered by the VDDSHV3 Dual-voltage I/O supply.

Same supply rail required to be connected to VDDSHV3 of processor and I/O supply rail of the device.

7.2.4.2 GPMC Interface

Check the number of devices connected to the GPMC interface.

It is recommended to connect the processor GPMC interface to a single device in synchronous mode. Using multiple devices (i.e., using multiple CSn) would require splitting the GPMC clock (and other interface signals) on board, which would cause signal integrity issues.

A detailed analysis is required when interfacing multiple devices (not recommended) in asynchronous mode. When interfacing multiple devices in asynchronous mode, the control signals would have to be routed to multiple devices. The split routing and loading issues will have an affect on the performance.

7.2.4.3 Reset

It is not necessary to use the reset signal. When using NAND/NOR boot with GPMC, many of the memories interfaced over GPMC may not have the reset signal.

In case reset pin is available, review the reset requirements and connect the reset pin to the relevant reset source.

7.2.4.4 Signals Termination

The active high ready / active low busy (R/B#) output from the NAND is open drain and is connected to the GPMC0_WAIT0 and GPMC0_WAIT1 signals (depending on the configuration). A termination (pullup, 4.7 kΩ) must be connected to the peripheral specific dual I/O supply rail close to the device.

It is recommended to provision for an external termination (pullup) on GPMC0_CS0..3 (depending on the configuration) to hold the signal high when processor is held in reset, or after reset, before software has configured the padconfig registers to enable the Tx buffer.

Provide a series termination (22 Ω) (close to processor pin) for GPMC0_CLK.

7.2.4.5 Capacitors for the Power Supply Rails

Check if required bulk and decoupling capacitors are provided for the processor I/O supply rail (VDDSHV3) and the device.

Follow the device-specific EVM implementation whenever recommendations are not available.

7.3 External Communication Interface (Ethernet, USB, PRUSS, UART and CAN)

7.3.1 Ethernet Interface Using Common Platform Ethernet Switch 3-Port Gigabit (CPSW3G)

Review the below implementations. Follow the device-specific EVM for implementation examples and termination values.

7.3.1.1 I/O Power Supply

The Gigabit Ethernet Media Access Controller (GEMAC) of the processor (used for Ethernet interface) is powered by the VDDSHV2 Dual-voltage I/O supply.

Same supply rail required to be connected to VDDSHV2 of processor and I/O supply rail of the device.

7.3.1.2 Reset

It is recommended to Implement the reset logic using Dual input AND gate. One of the AND gate input is controlled by processor general purpose input/output (GPIO) pin. Terminate the AND gate input using pullup connected to the specific GPIO I/O domain supply voltage. The other input of the AND gate can be the Main Domain POR status output (PORz_OUT) or Main Domain warm reset status output (RESETSTATz) Signal.

In case an ANDing logic is not used and the processor reset status output is used directly to reset the attach devices, ensure the I/O levels of the attach device match the processor I/O level or use a level translator to match the levels.

7.3.1.3 PHY Pin Strapping

Most PHYs configure their outputs as inputs during reset, and captures configuration information on theses I/Os when the device is released from reset. Therefore, it may be necessary to apply appropriate pullup/pulldown resistors on these I/Os which also connect to processor I/Os. The TI PHYs used on the GP EVM use a combination of pullup and pulldown resistors to generate a mid-level voltage, allowing multiple configuration bits to be encoded on each pin. By default, the processor input buffers and internal pullup/pulldown resistors are disabled, which eliminates any concern with a mid-supply potential being applied to the processor input buffer when required by the PHY. Remove the PHYs from reset before enabling any of the associated processor input buffers to ensure the PHY is driving a valid logic state.

7.3.1.4 Ethernet PHY (and MAC) Operation and MII Interface Clock

Check the clock input type used for Ethernet PHY and MAC based on the interface.

7.3.1.4.1 Crystal

If a crystal is used as the clock source for the Ethernet PHY, the crystal specification is required to be similar for the processor to ensure optimized performance.

7.3.1.4.2 Oscillator

When an external clock (LVCMOS) oscillator is used as the clock source for the PHY, a single oscillator is recommended for the processor and the PHY. It is recommended to use two-output phase aligned buffer for processor and the PHY. Be sure to terminate XO of the processor and the Ethernet PHY as per the device-specific processor data sheet recommendations.

7.3.1.4.3 Processor Clock Output (CLKOUT0)

Alternative approach for clocking the Ethernet PHY is to use the processor clock (CLKOUT0) outputs. Clock out is buffered internally and is intended for a point-point clock topology.

Most RGMII PHYs require a 25 MHz clock input that is not synchronous to any other signals. So this signal will not have any timing requirements, but it is important the PHY does not receive any non-monotonic transitions on its clock input.

RMII PHY clocking option changes with the device controller (master) and device (slave) configuration.

When configured as controller, most RMII PHYs require a 25 MHz input clock that is not synchronous to any other signals, the 25 MHz clock signal will not have any timing requirements, but it is important to make sure the PHY does not receive any non-monotonic transitions on its clock input.

In some cases the RMII PHY may provide an option to source the 50 MHz to the MAC. For this use case, the 50 MHz data transfer clock is delayed to the MAC relative to the PHY. This shifts clock to data timing relationship which will erode the timing margin. This could be problematic for some designs if this delay is too large.

When configured as device, the MAC and the PHY uses a 50 MHz clock that is synchronous to both transmit and receive data. The 50 MHz clock is defined in the RMII specification as a common data transfer clock signal that is used by both the MAC and the PHY, where transitions are expected to arrive simultaneously at the MAC and PHY device pins. This provides the best timing margin for both transmit and receive data transfers. It is also important that the MAC and PHY do not receive any non-monotonic transitions on their clock inputs. To ensure this doesn't happen, it is highly recommended this clock signal is routed through a two-output phase aligned buffer. Recommend using equal length signal traces that are ½ the length of the data signals for connecting the clock buffer outputs, where one clock output connects to the MAC and the other connects to the PHY.

For RMII interface, the recommended configuration is the *RMII Interface Typical Application (External Clock Source)* explained in the device-specific TRM. If *RMII Interface Typical Application (Internal Clock Source)* configuration explained in the device-specific TRM is used the performance has to be validated on a system level. Provision for an external clock for initial performance testing and comparison is recommended. The Ethernet performance (RGMII) has been validated on the processor and the Ethernet PHY with 25 MHz clock.

The CLKOUT0 signal function can be used to source a 25 MHz or a 50 MHz clock to the PHY. However, it must be configured by software. This configuration cannot be used if the product needs to support Ethernet boot. This clock is likely to glitch anytime the configuration is changed.

Processor automatically begins sourcing the device reference clock (MCU_OSC0, enabled by default) to the WKUP_CLKOUT0 pin as soon as the device is released from reset (MCU_PORz 0 -> 1). This clock does not glitch after it begins to toggle. However, the first high or low pulse could be short since reset is released asynchronous to the HFOSC0 clock.

The board designer needs to make sure the PHYs are held in reset for a specified minimum reset hold time after the respective clocks are valid.

TI does not define performance of the processor clock outputs because clock performance is influenced by many variables unique to each system implementation. The board designer will have to validate timing of all peripherals by using their actual PCB delays, min/max output delay characteristics, and min setup/hold requirements of each device to confirm there is enough timing margin.

7.3.1.5 Reduced Gigabit Media Independent Interface (RGMII) /Reduced Media Independent Interface (RMII) Signals Termination

Series terminations (22 Ω) are recommended for the Ethernet MAC interface signals. These resistors must be as small as possible (0402 or smaller) and placed as close to the transmitter as possible. To start with place a series termination (22 Ω) for the TX signals. For the RX signals the PHYs internal terminations can be used. Series terminations (0 Ω) are still recommended on the RX signals.

Check the placement of the terminations as below:

- Tx signal lines (TD0..3, TXC, TX_CLK) (close to processor pin) are required to have a series termination (22 Ω).
- Check placement of terminations for Rx signal lines (RD0..3, RXC, RX_CLK) close to Ethernet PHY.

The interrupt output of the Ethernet PHY can be connected to the EXTINTn pin. A termination (parallel) is recommended for the EXTINTn input close to the processor.

EXTINTn is an input (interrupt) pin and it is recommended to be terminated when connected to a PCB trace or an external input. This is a failsafe input.

7.3.1.6 MAC (Media Access Controller) to MAC Interface

For applications requiring PHY-less (MAC-to-MAC) connection over the CPSW3G, using the RGMII interface is recommended (check with TI if this is officially supported) since the clocks are source synchronous.

7.3.1.7 Management Data Input/Output (MDIO) Interface

The MDIO interface of the processor is powered by the VDDSHV2 Dual-voltage I/O supply.

MDIO0_MDIO pin is required to have an external parallel termination (pullup) to the device I/O supply.

Before configuring the MDIO interface, see the advisory *i2329 MDIO: MDIO interface corruption (CPSW and PRU-ICSS)*.

7.3.1.8 Ethernet Medium Dependent Interface (MDI) Interface Including Magnetics

In case the PHY and MDI interface including the magnetics is implemented on the processor board, follow the EVM for MDI interface, magnetics recommendation, ESD protection and connection of magnetic shield.

7.3.1.9 Capacitors for the Power Supply Rails

Check if required bulk and decoupling capacitors are provided for the processor I/O supply rail (VDDSHV2) and the device.

Follow the device-specific EVM implementation whenever recommendations are not available.

7.3.2 Universal Serial Bus (USB)

The processor provides 2 X USB interfaces that can be configured as host or device.

USBn_VBUS is required to be connected in accordance with the *USB Design Guidelines* section of the device-specific processor data sheet. The voltage divider/clamp circuit must be implemented for proper operation. The Zener diode can only be removed if one is absolutely sure that the product will never experience a VBUS signal potential greater than 6 V. The supply voltage range for the VBUS pin are defined in the *Absolute Maximum Ratings* table.

USBn_ID functionality is supported via any of the GPIO.

7.3.2.1 USB Used

Place separate calibration resistor (pulldown) for USB0..1_RCALIB pins with recommended value in the device-specific processor data sheet, when USB rails (VDDA_CORE_USB, VDDA_1P8_USB, and VDDA_3P3_USB) are connected to power sources.

7.3.2.1.1 USB Host Interface

Check if USB power switch to control the USB device power (VBUS) connected to the USB type A connector and recommended capacitors (>120-µF connected to the VBUS close to the connector) are provided. The switch additionally provides over load protection. If the power distribution switch has an over current OC indication, terminate the OC near to the power switch and connect to the processor input.

The USBn_DRVVBUS signal configured as GPIO is used to enable the USBn_VBUS (5 V) power switch when the USB interface is configured as host. An external parallel termination (pulldown) is recommended for USBn_DRVVBUS signal close to the power switch.

USB0..1_VBUS pin can be left unconnected.

7.3.2.1.2 USB Device Interface

The VBUS power is sourced by an external host. USB device operation requires capacitance < 10 µF connected to the VBUS close to the connector.

The VBUS is required to be scaled down using an external resistor divider, which limits the voltage applied to the USBn_VBUS before connecting to the processor. Choose a zener diode with leakage current of < 100 nA at 5 V and resistors with 1% tolerance.

For removing the zener diode, see the note about USB Boot Mode.

7.3.2.1.3 USB Dual-Role-Device Interface

If the design uses USB micro-AB connector, the USB_ID signal from the connector can be routed to a GPIO pin. This can be connected to any available GPIO pin. The GPIO pin is specified in the board device tree file, including the pinmux setting of the GPIO pin.

If the hardware design uses USB type-C connector, the USB_ID signal is not needed. The DRD mode switching is controlled by the USB type-C companion device. The AM62 SK EVM USB0 port design can be used as a reference.

The TYPE-C Dual PD Controller is expected to take care of configuring the required USB capacitor value (> 120-µF / < 10-µF), see the device-specific EVM.

Note

Full compliant USB On-The-Go (OTG) feature is not supported in AM625 / AM623 and AM62A7 / AM62A3 devices. The ID pin is not bonded out.

7.3.2.2 USB Not Used

If USB0 or USB1 is not used, see the *Pin Connectivity Requirements* section of the device-specific processor data sheet.

If USB0 and USB1 are not used, provide provision to connect the USB supply rails VDDA_CORE_USB, VDDA_1P8_USB and VDDA_3P3_USB to VSS. USB0..1_DM, USB0..1_DP, USB0..1_RCALIB and USB0..1_VBUS signals can be left unconnected.

In case USB0 or USB1 are required for future expansion connect the signals (USB0..1_DM, USB0..1_DP, USB0..1_RCALIB and USB0..1_VBUS) with shortest possible traces and terminate to test points or connectors. Additionally, provision to connect the USB supply rails has to be provided.

7.3.2.3 Additional Information

Connect USB_DP and USB_DM signals directly (without any series termination resistors or capacitors). Route these signals with traces that does not include any stubs or test points. Connect USB traces directly between the processor and the external connector, unless EMI control is needed.

Connect USB_DP and USB_DM signals directly from the processor to the USB hub upstream port. The hub then distributes these signals to the downstream ports as needed. Grounded the connector ID to enable host mode. As each hub has different implementation requirements, it is recommended to follow the hub manufacturer recommendations.

Common-mode chokes may be needed for EMI/EMC control. These may reduce the signal amplitude and degrade performance. In addition, consider adding ESD protection based on the system requirement.

For detailed recommendations on USB signal connection and routing, see the *High-Speed Interface Layout Guidelines*. Add appropriate constraints or routing requirements to your schematic. This will vary from tool to tool.

7.3.3 Programmable Real-Time Unit Subsystem (PRUSS)

7.3.3.1 AM625 / AM623

For availability of the PRUSS features and supported functionalities, see the *Device Comparison* section of the device-specific processor data sheet.

The programmable nature of the PRU cores, along with their access to pins, events and all processor resources, provides flexibility in implementing fast real-time responses, specialized data handling operations, custom peripheral interfaces, and in offloading tasks from the other processor cores of the device.

The PRUSS has a large number of I/O signals available. Most of these I/Os are multiplexed with other functional signals at the processor level. PRUSS pins allow muxing using the PADCONFx registers.

Review the interface connection supports the required functionalities during schematic design.

To understand the PRUSS supported functionalities, see the device-specific processor data sheet and TRM.

7.3.3.2 AM62A7 / AM62A3

Not Supported

7.3.4 Universal Asynchronous Receiver/Transmitter (UART)

Check the UART interface requirements, application (external interface or debug), configuration (2-wire or 4-wire with flow control), use of external transceiver and install terminations (pullup) on the UART_RXD pins (UART receiver).

Make sure the external interface levels matches the Dual-voltage I/O supply voltage level.

This peripheral is frequently hooked up incorrectly. Make sure signals are connected as follows:

- TX ---> RX
- RX ---> TX

If additional interface signals are used, check the connection.

For the number of instances supported, see the device-specific processor data sheet.

Consider providing a series termination (22 Ω) on the interface signals near to the connector for debug.

An external ESD protection is recommended in case the interface signals are terminated to an external connector.

7.3.5 Controller Area Network (CAN)

The CAN signals are interfaced to the processor through an external transceiver. Follow the CAN interface specifications for differential termination and protection. Be sure to match the interface signals polarity and supply voltage levels between the transceiver and the processor.

For the number of instances supported, see the device-specific processor data sheet.

Consider providing a series termination (22 Ω) on the interface signals near to the connector for debug.

7.4 On-Board Synchronous Communication Interface (MCSPI, MCASP and I2C)

7.4.1 Multichannel Serial Peripheral Interface (MCSPI) and Multichannel Audio Serial Ports (MCASP)

Check if series terminations (22 Ω) are provided for clock signals SPI0..2_CLK (MCSPI 0..2) and MCU_SPI0..1_CLK (MCU_MCSPI 0..1) close to processor pins.

Check if series terminations (22 Ω) are provided for Transmit clock signals MCASP0..2_ACLKX and Transmit Frame Sync signals MCASP0..2_AFSX close to processor pins.

Check if series terminations (22 Ω) are provided for Receive clock signals MCASP0..2_ACLKR and Receive Frame Sync signals MCASP0..2_AFSR close to device pins.

Check if the external terminations (parallel) are provided for Chip Select signals SPI0..2_CS0..3 (MCSPI 0..2) & MCU_SPI0..1_CS0..3 (MCSPI 0..1) close to the device pins.

7.4.2 Inter-Integrated Circuit (I2C)

Check if the application requires a fully compliant I2C interface. The WKUP_I2C0 and MCU_I2C0 are true open-drain buffers and fully compliant to the I2C specifications. These support 100-kHz and 400-kHz operation. Recommended to connect noise filter for these open drain I2C interface to match the input slew rate when operating the I/O in 3.3 V mode. Check if terminations (pullup, 4.7 kΩ) are provided on both I2C signals (x_SDA and x_SCL). Be sure that the pullup resistors are connect to the correct I/O voltage rail. For more information, see Section 7.6.2. For more information, see the *Pin Connectivity Requirements* section of the device-specific processor data sheet in-case these I2C interfaces are not used.

Check if the application required additional I2C interfaces.

The I2C0..3 use LVCMOS to emulate an open-drain buffer and not fully compliant with the I2C specification, in particular falling edges are fast (< 2 ns). Any devices connected to these ports must be able to function properly with the faster fall time. These can support 3.4-Mbps I2C operations. Terminations (pullup) are recommended for these I2C signals and stubs have to be minimized (connect directly to the signal) while connecting to the pullup resistors.

If you are planning to use TI provided software, be sure to connect I2C0 to the PMIC, as this is the interface port used for PMIC control.

Note

MCU_I2C0 and WKUP_I2C0 are implemented with fail-safe I/Os.

All I2C ports in the main domain are not fail-safe and cannot have any potential applied to the I2C pins before the respective processor I/O supply is powered.

Note

When I2C3 interface is used, see the I2C3 note (can be multiplexed to more than one pin) in the I2C section of the device-specific processor data sheet.

7.5 User Interface (CSIRX0, DPI, OLDI), GPIO and Internal Diagnostics

7.5.1 Camera Serial Interface (CSI-Rx (CSI-2 port, CSIRX0 Instance))

7.5.1.1 CSIRX0 Used

The CSIRX0 I/O supply rails VDDA_1P8_CSIRX0, VDDA_CORE_CSIRX0 must be connected to the appropriate power supply rails.

Place calibration resistor (pulldown) for CSI0_RXRCALIB pin with recommended value in the device-specific processor data sheet.

Follow *High-speed interface layout guidelines* for this interface due to higher data rates on serial data lanes.

7.5.1.2 CSIRX0 Not Used

If CSIRX0 is not used and device boundary scan function is used, the CSIRX0 I/O supply rails VDDA_CORE_CSIRX0 and VDDA_1P8_ CSIRX0 must be connected to valid power sources (ferrite bead (when used) and bulk capacitor can be removed).

If CSIRX0 is not used and the device boundary scan function is not used, provide provision to connect the CSIRX0 I/O supply rails VDDA_CORE_CSIRX0 and VDDA_1P8_ CSIRX0 to VSS. Ferrite bead (when used), decoupling and bulk capacitor can be removed.

For terminating the CSI0_RXRCALIB, CSI0_RXP0..3, CSI0_RXN0..3, CSI0_RXCLKP and CSI0_RXCLKN pins, see the *Pin Connection Requirements* section of the device-specific processor data sheet.

7.5.2 Display Subsystem

7.5.2.1 DPI (Display Parallel) Interface

7.5.2.1.1 I/O Power Supply

The DPI interface of the processor is powered by the VDDSHV3 Dual-voltage I/O supply.

7.5.2.1.2 Reset

Check if provision for device reset is provided. Depending upon the use case, it is recommended to implement the reset logic using Dual input AND gate. One of the AND gate input is controlled by processor general purpose input/output (GPIO) pin. Terminate the AND gate input using pullup connected to the specific GPIO I/O domain supply voltage. The other input of the AND gate can be the Main Domain warm reset status output (RESETSTATz) Signal.

In case an ANDing logic is not used and the processor reset status output is used directly to reset the attach devices, ensure the I/O levels of the attach device match the processor I/O level or use a level translator to match the levels.

7.5.2.1.3 Connection

Check display (RGB) connections.

When connecting only 16-bit data to an 18-bit panel (BGR565 to BGR666), connect D0-D4 to B1-B5 on LCD, D5-D10 to G0-G5 on the LCD, and D11-D15 to R1-R5 on LCD. Then connect B0->B5, R0->R5. This allows full color spectrum with some degradation in gradients.

7.5.2.1.4 Signals Termination

Check if series termination (22 Ω) is provided for VOUT0_PCLK (Pixel Clock Output) pin close to processor pin. If space is not a constraint, consider adding series terminations (22 Ω) for all other control and data pins.

7.5.2.1.5 Capacitors for the Power Supply Rails

Check if required bulk and decoupling capacitors are provided for the processor I/O supply rail (VDDSHV3) and the device.

Follow the device-specific EVM implementation whenever recommendations are not available.

7.5.2.2 Open LVDS Display Interface (OLDI)

7.5.2.2.1 AM625 / AM623

7.5.2.2.1.1 OLDI Used

####### 7.5.2.2.1.1.1 I/O Power Supply

The OLDI I/O supply rail VDDA_1P8_OLDI0 pin must be connected to the valid 1.8 V source. Fore more information, see the *Recommended Operating Conditions* section of the device-specific processor data sheet.

####### 7.5.2.2.1.1.2 Reset

Check if provision for device reset is provided. Depending upon the use case, it is recommended to implement the reset logic using Dual input AND gate. One of the AND gate input is controlled by processor general purpose input/output (GPIO) pin. Terminate the AND gate input using pullup connected to the specific GPIO I/O domain supply voltage. The other input of the AND gate can be the Main Domain warm reset status output (RESETSTATz) Signal.

In case an ANDing logic is not used and the processor reset status output is used directly to reset the attach devices, ensure the I/O levels of the attach device match the processor I/O level or use a level translator to match the levels.

####### 7.5.2.2.1.1.3 OLDI Interface Compatibility

Check OLDI interface compatibility. For validating the I/O voltage level compatibility, see the *OLDI LVDS (OLDI) Electrical Characteristics* section of the device-specific processor data sheet.

####### 7.5.2.2.1.1.4 Capacitors for the Power Supply Rails

Check if required bulk and decoupling capacitors are provided for the processor OLDI0 1.8 V analog supply rail (VDDA_1P8_OLDI).

Follow the device-specific EVM implementation whenever recommendations are not available.

7.5.2.2.1.2 OLDI Not Used

The OLDI I/O supply rail VDDA_1P8_OLDI0 must remain powered by a valid 1.8 V source (ferrite bead (when used) and bulk capacitor can be removed). For more information, see the *Recommended Operating Conditions* section of the device-specific processor data sheet.

For terminating the OLDI0_A0..7N, OLDI0_A0..P, OLDI0_CLK0..1N and OLDI0_CLK0..1P pins, see the *Pin Connection Requirements* section of the device-specific processor data sheet.

7.5.2.2.1.3 Additional Information

The differential impedance for the OLDI signal traces must be within 100 +/- 10 Ω. Source termination resistors are not required.

The signals are recommended to be connected as a point-to-point interface going from the processor to a connector. Ensure there are no stubs in the design.

Follow *High-speed interface layout guidelines* due to higher data rates on serial data lanes.

Ensure board-level implementation complies with the physical layer definition of *IEEE1596.3* standard and *ANSI/TIA/EIA644-A standard (Electrical Characteristics of Low Voltage Differential Signaling (LVDS) interface Circuits)*.

7.5.2.2.2 AM62A7 / AM62A3

Not Supported.

7.5.3 General Purpose Input/Output (GPIO)

7.5.3.1 CLKOUT Available on GPIO

MCU_OSC0_XO is available by default on the WKUP_CLKOUT0.

7.5.3.2 Termination and Buffering

Consider adding series termination (22 Ω) to limit the current or avoid reflections and buffering the GPIO output when higher current sourcing is required.

EXTINTn is an input pin and is recommended to be terminated when connected externally or a PCB trace is connected.

7.5.3.3 Unused GPIO

The *Pin Connectivity Requirements* section in the device-specific data sheet describes the special connectivity requirements for pins, including unused pins. It should be okay to leave any unused pin that does not have a special requirement mentioned in the pin connectivity section unconnected.

If a PCB trace is connected to any of the unused processor GPIO pads/pins, an external termination (pullup/pulldown) is recommended. If the I/Os are terminated to an external interface connector, an external ESD protection is recommended.

7.5.3.4 Additional Information

Signals on unused interfaces can typically be left as no connection, unless otherwise stated. Many of the I/Os have a *Pad Configuration Register* that provides control over the input capabilities of the I/O (RXENABLE field in each conf_<module>_<pin> register). For more details, see the *Control Module* chapter of the device-specific TRM. Software can disable the I/O receive buffers (that is, RXENABLE=0) that are not connected in the design as soon as possible during initialization. Software needs to be ensure that it does not accidentally enable the receiver of an I/O (by setting the RXENABLE bit) when the associated pin is floating.

Note

For specific guidance on certain unused pins, see the *Pin Connectivity requirements* section of the device-specific processor data sheet.

Note

For specific guidance configuring I/Os, see the *Pad Configuration Registers* chapter of the device-specific TRM.

7.5.4 Internal Diagnostics

7.5.4.1 Monitoring of Voltage Using Processor

7.5.4.1.1 Voltage Monitor Pins Used

Connect the VSYS voltage to the VMON_VSYS through an external voltage divider (0.45 V ± 3 %). Consider implementing a noise filter (capacitor) on the voltage divider output as described in the device-specific processor data sheet.

For more information see the *System Power Supply Monitor Design Guidelines* section of the device-specific processor data sheet.

Connect VMON_1V8_SOC and VMON_3V3_SOC pins directly to their respective supplies.

7.5.4.1.2 Voltage Monitor Pins Not Used

Connect VMON_VSYS and VMON_3P3_SOC pins directly to VSS.

VMON_1P8_SOC must be tied to the respective supply. Grounding this signal would short internal 1V8 supplies and is not allowed.

7.5.4.2 Temperature Monitoring

7.5.4.2.1 AM625 / AM623

The Voltage and Thermal Manager (VTM) module on the AM625 / AM623 supports voltage and thermal management of the processor by providing control of on-chip temperature sensors.

The processor supports a single VTM module, VTM0, which is located in the WKUP domain. VTM0 has two associated temperature monitors, Temp_Sensor_Main_0, and Temp_Sensor_Main_1, each of which are located near hot-spots in the device die.

7.5.4.2.2 AM62A7 / AM62A3

The Voltage and Thermal Manager (VTM) module on the AM62A7 / AM62A3 supports voltage and thermal management of the processor by providing control of on-chip temperature sensors.

The processor supports a single VTM module, VTM0, which is located in the WKUP domain. VTM0 has three associated temperature monitors, Temp_Sensor_Main_0, Temp_Sensor_Main_1 and Temp_Sensor_Main_2, each of which are located near hotspots in the device die.

7.5.4.2.3 Additional Information

TI does not spec or guarantee any accuracy for the VTM module with regard to temperature measurements. A ± 7°C accuracy is provided to give an indication and we have performed internal characterization to confirm the measurements are within specified range.

7.5.4.3 Termination of Error Signal Output MCU_ERRORn

Recommend terminating MCU_ERRORn signal as per the *Pin Connectivity Requirements* section of the device-specific processor data sheet.

7.5.4.4 Oscillator Clock Loss Detection

The processor supports HFOSC0 clock loss detection circuitry to detect when HFOSC0_CLK stops toggling. Dedicated hardware logic monitors HFOSC0 clock using CLK_12M_RC clock. When HFOSC0_CLK stops toggling for 9 CLK_12M_RC clock periods, a HFOSC0 clock stop loss condition is detected. If CTRLMMR_MCU_PLL_CLKSEL[8] CLKLOSS_SWTCH_EN is set , the reference clock is switched from HFOSC0_CLKOUT to CLK_12M_RC to allow the device to operate with a slower clock.

During clock-loss condition, the processor reports the error to the external device through MCU_ERRORn pin - the pin is driven Low. The recovery mechanism is up to the external system (such as a PMIC to take action).

For example, doing a full system power cycle to see if the system recovers. If the system does not recover then, it has to take some other action such as to check system clocks, external crystal or supply rails.

7.6 Verifying Board Level Design Issues

7.6.1 Pinmux

All peripheral and I/O configuration must be verified using the TI *SysConfig-PinMux* Tool to ensure valid I/O Sets have been used.

For more information, see the PinmuxConfigSummary.csv provided by the SysConfig-PinMux tool.

7.6.2 Terminations (Pullups)

Terminating a signal to the wrong I/O supply rail can cause leakage between the I/O rails of the processor. Each signal has an associated I/O supply rail (Ex: VDDSHVx [x=0-6]). For more information, see the *Pin Attributes* table in the device-specific processor data sheet.

For example, if you want to pullup SPI0_CLK signal in any mux mode (EHRPWM1_A, GPIO1_17, and so forth), pull up the signal to VDDSHV0.

7.6.3 General Debug

7.6.3.1 Clock Output for Board Bring-Up, Test or Debug

The below clock outputs are available on the processor pins for test and debug purposes only.

- OBSCLK0, MCU_OBSCLK0 (recommended): Observation clock outputs
- SYSCLKOUT0 (optional) : MAIN_PLL0_HSDIV0_CLKOUT (SYSCLKOUT0) divided by 4 and then sent out of the device
- MCU_SYSCLKOUT0 (optional) : MCU_PLL0_HSDIV0_CLKOUT (MCU_SYSCLKOUT0) divided by 4 and sent out of the device

If the processor pins designated OBSCLK0 (available on two pins in AM625 / AM623 devices), OBSCLK0..1 (in AM62A7 / AM62A3 devices), MCU_OBSCLK0, SYSCLKOUT0, MCU_SYSCLKOUT0 are not used, provide a test point for test/debug. Consider adding a termination (parallel).

In case these pins are used, a test point can be inserted on the trace and provision to isolated these signals from the connected devices can be provided for test/debug.

OBSCLK pins can be used to select one of the several different clocks as output.

System clock pins (MCU_SYSCLKOUT0 and SYSCLKOUT0) are hardwired to dedicated clock resources.

7.6.3.2 Additional Information

Provide test points for MCU_RESETSTATz, RESETSTATz and PORz_OUT for debug.

For attached devices that have an alert output, over current indication or PG (power good) output that is not used, provide a termination (parallel) and test point for debug or future enhancements.

8 Notes For Layout (To be Added on the Schematic)

Add design notes as required for the processor peripherals (example, USB, Ethernet, CSI, OLDI (AM625 / AM623), eMMC, SD, and so forth) and attach device including Board Boot mode configurations, placement of terminations, placement of decoupling and bulk capacitors.

Mark all differential signals, critical signals and specify the target impedance. See examples below:

- DDR target impedance is 40 Ω (single-ended) and 80 Ω (differential) for the DDR signals.
- The differential impedance for the USB data lines must be within the specified tolerance for a nominal value of 90 Ω.
- The differential impedance for the Ethernet MDI signals, CSI and OLDI (AM625 / AM623) signals must be within the specified tolerance for a nominal value of 100 Ω.

9 Design Simulation

Signal Integrity SI simulations are performed on the EVMs. The baseline drive impedance and ODT settings are derived from the simulations.

It is recommended to perform simulation for the design as the values may be different based on board design.

The drive strength is adjustable using the DDR Register Configuration Tool on SysConfig.

For more information, see the [FAQ] AM62A7 or AM62A3 Custom board hardware design – Processor DDR Subsystem and Device Register configuration.

10 Additional References

The reference document includes schematic checklist for some of the attach devices that can be used during design and review.

TPS65219 Schematic, Layout Checklist

Design files for Powering the AM62x with the TPS65219 PMIC

11 Summary

This schematic checklist is provided as a guide for use during schematic development. The recommendations provided within this document may help reduce debug time and limit or eliminate future re-spins of the system.

12 References

12.1 AM625/AM623

- Texas Instruments: *AM625 / AM623 Sitara™ Processors Data Sheet*
- Texas Instruments: *AM625 / AM623 Sitara Processors Technical Reference Manual*
- Texas Instruments: *AM625 / AM623 Silicon Errata*
- Texas Instruments: *Starter Kit SK-AM62 EVM*
- Texas Instruments: *Starter Kit SK-AM62-P1 EVM using PMIC*
- Texas Instruments: *Hardware Design Guide for AM625 / AM623 Devices*
- Texas Instruments: *AM625 / AM623 Power Consumption Summary*
- Texas Instruments: *Powering the AM625 / AM623 With the TPS65219 PMIC*
- Texas Instruments: *Discrete Power Solution for AM625 / AM623*
- Texas Instruments: *AM625 / AM623 Escape Routing PCB Design Application note*
- Texas Instruments: *AM62x (AMC) Escape Routing for PCB Design Application note*
- Texas Instruments: *AM625 / AM623 DDR Board Design and Layout Guidelines*

12.2 AM62A7/AM62A3

- Texas Instruments: *AM62A7 / AM62A3 Sitara™ Processors Data Sheet*
- Texas Instruments: *AM62A7 / AM62A3 Sitara Processors Technical Reference Manual*
- Texas Instruments: *AM62A7 / AM62A3 Silicon Errata*
- Texas Instruments: *Starter Kit SK-AM62A-LP EVM*
- Texas Instruments: *AM62A7 / AM62A3 Power Estimation Tool*
- Texas Instruments: *AM62A7 / AM62A3 Escape Routing PCB Design Application note*
- Texas Instruments: *AM62A7 / AM62A3 DDR Board Design and Layout Guidelines*
- Texas Instruments: *Hardware Design Guide for AM62A7 / AM62A3 Devices*

12.3 Common

- Texas Instruments: *Thermal Design Guide for DSP and Arm Application Processors*
- Texas Instruments: *Sitara Processor Power Distribution Networks: Implementation and Analysis*
- Texas Instruments: *Emulation and Trace Headers Technical Reference Manual*
- Texas Instruments: *High-Speed Interface Layout Guidelines*
- *XDS Target Connection Guide*
- *IEEE1596.3*
- *ANSI/TIA/EIA644-A standard (Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits*
- Texas Instruments: *General Hardware Design/BGA PCB Design/BGA Decoupling*
- Texas Instruments: *Clocking Design Guide for KeyStone Devices*
- Texas Instruments: *Jacinto™ 7 DDRSS Register Configuration Tool*

13 Terminology

BOM – Bill of Materials

CAN – Controller Area Network

CKE – Clock Enable

CPSW3G – Common Platform Ethernet Switch 3-port Gigabit

CSIRX – Camera Streaming Interface Receiver

DFU – Device Firmware Upgrade

DNI – Do Not Install

DPI – Display Parallel Interface

E2E – Engineer to Engineer

ECC – Error-Correcting Code

EMC – Electromagnetic Compatibility

EMI – Electromagnetic Interference

eMMC – embedded Multi-Media Card

EMU – Emulation Control

ePWM – enhanced Pulse-Width Modulator

eQEP – enhanced Quadrature Encoder Pulse

ESD – Electrostatic discharge

ESL – Effective Series Inductance

ESR – Effective Series Resistance

FET – Field-Effect Transistor

GEMAC – Gigabit Ethernet Media Access Controller

GPIO – General Purpose Input/Output

GPMC – General-Purpose Memory Controller

HS-RTDX – High Speed Real Time Data eXchange

I2C – Inter-Integrated Circuit Interface

IBIS – Input/Output Buffer Information Specification

IEP – Industrial Ethernet Peripheral

JTAG – Joint Test Action Group

LDO – Low Dropout

LVCMOS – Low voltage complementary metal oxide semiconductor

LVDS – Low Voltage Differential Signaling

MAC – Media Access Controller

MCASP – Multichannel Audio Serial Ports

MCSPI – Multichannel Serial Peripheral Interface

MDI – Medium Dependent Interface

MDIO – Management Data Input/Output

MMC – Multi-Media Card

MMCSD – Multi-Media Card/Secure Digital

ODT – On-die Termination

OLDI – Open LVDS Display Interface

OSPI – Octal Serial Peripheral Interface

OTP – One-Time-Programmable

PCB – Printed Circuit Board

PDN – Power Distribution Network

PET – Power Estimation Tool

PMIC – Power management integrated circuit

POR – Power-on Reset

PRUSS – Programmable Real-Time Unit Subsystem

QSPI – Quad Serial Peripheral Interface

RGMII – Reduced Gigabit Media Independent Interface

RMII – Reduced Media Independent Interface

ROC – Recommended Operating Condition

SD – Secure Digital

SDIO – Secure Digital Input Output

SPI – Serial Peripheral Interface

TCK – JTAG Test Clock Input

TDI – JTAG Test Data Input

TDO – JTAG Test Data Output

TEN – Test Enable

TMS – JTAG Test Mode Select Input

TRM – Technical Reference Manual

TRSTn – JTAG Reset

UART – Universal Asynchronous Receiver/Transmitter

USB – Universal Serial Bus

14 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2023) to Revision B (April 2023) Page

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