AM263x Crystal Selection

Summary

This document is a quick note on the selection of crystals for the AM263x family of MCU.

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1 Crystal Selection

To enable oscillation at the specified crystal frequency, a specific load capacitance CL, must be seen by the crystal when it is inserted into the application circuit. This CL capacitance is specified in the crystal datasheet and is primarily created by the addition of the CL1 and CL2 capacitors into the crystal circuit as shown in the schematic excerpt below.

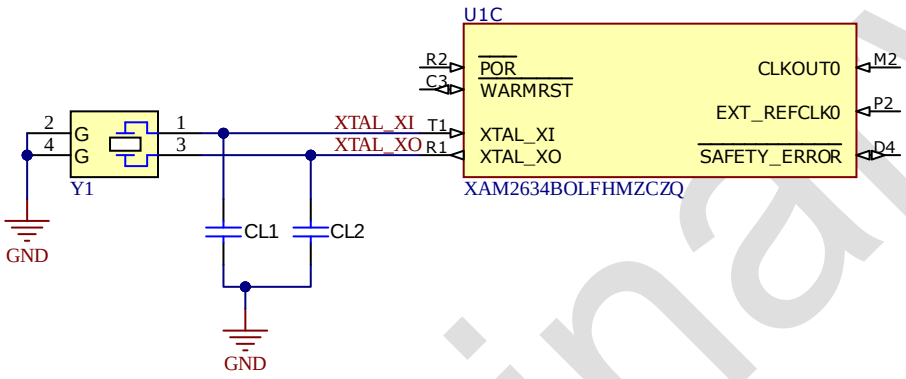

Figure 1 – AM263x Crystal Circuit

The values of CL1 and CL2 must take into account the additional, parasitic loading of the PCB traces, the MCU package, and die capacitance, such that the total capacitance is as close as possible to specified crystal CL value. The load capacitors, CL1, and CL2 should be chosen such that the below equation is satisfied.

- CL – total capacitance seen by the crystal when inserted in-circuit.
- CL1, CL2 – additional load capacitor on XI and XO pins
- CPCBXI, CPCBXO– capacitance of the traces from the MCU to the crystal – can be minimized by keeping routing short and using smallest trace width.
- CXI, CXO – parasitic capacitance from the MCU package and die pads

$$CL = [(CL1 + CPCBXI + CXI) \times (CL2 + CPCBXO + CXO)] / [(CL1 + CPCBXI + CXI) + (CL2 + CPCBXO + CXO)]$$

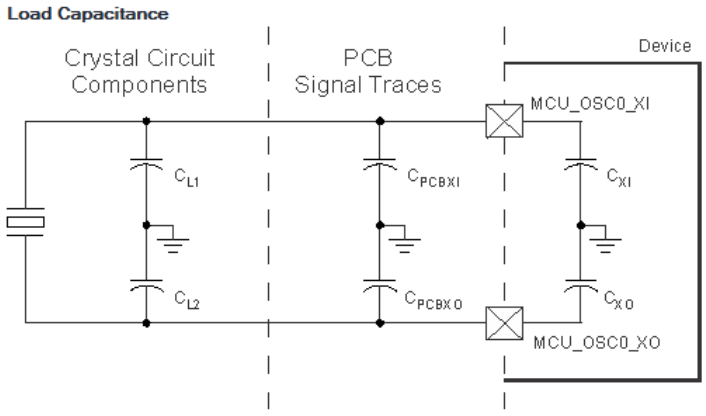

Figure 2 - Crystal Load Capacitance and Parasitics

Assuming, CL1, and CL2 (and their associated parasitics) on the XI branch and XO branch of the oscillator circuit are equal, then CL1, and CL2 can be solved as shown below. This assumes the XI branch and the XO branch each contribute half of the total CL loading.

```
CL1 = [(2CL) - (CPCBXI + CXI)]
CL2 = [(2CL) - (CPCBXO + CXO)]
```

As an example, if CL = 8pF, CPCBXI = 1pF, CPCBXO = 1pF, CXI = 0.01pF, and CXO = 0.01pF, CL1 and CL2 can be calculated as:

```
CL1 = [(2CL) - (CPCBXI + CXI)] = [(2 × 8 pF) - 1.0 pF - 0.01 pF)] = 14.99 pF
CL2 = [(2CL) - (CPCBXO + CXO)] = [(2 × 8 pF) - 1.0 pF - 0.01 pF)] = 14.99 pF
```

In this example case, CL1 and CL2 should be selected to the nearest available capacitor value of 15pF.

CL1 and CL2 must be between the minimum and maximum allowed by the MCU datasheet crystal parameter tables. Additionally, the ESR, and PPM offset and all other requirements must by respected for valid operation. See the AM263x datasheet for the final device values. They are excerpted here for convenience.

Table 1 - AM263x Crystal Oscillator Parameters – Datasheet Excerpt

7.11.4.1.1 Crystal Oscillator (XTAL) Parameters

PARAMETER		MIN	TYP	MAX	UNIT
F_{xtal}	Crystal Parallel Resonance Frequency (Fundamental mode oscillation only)	–50ppm	25	50ppm	MHz
CC1	Capacitance of C_{L1} + C_{PCBXI}	12		24	pF
CC2	Capacitance of C_{L2} + C_{PCBXO}	12		24	pF
C_{shunt}	Crystal Circuit Shunt Capacitance			5	pF
ESR_{xtal}	Crystal Effective Series Resistance			46	Ω

7.11.4.1.2 External Clock Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
C_{Pkg}	Shunt Capacitance of pkg		0.01		pF
P_{xtal}	Power dissipation		$0.5 \times ESR \times (2 \times \pi \times F_{xtal} \times C_L \times 1.8)^2$		W
t_s	Start up time		1.5		ms

2 Revision History

Rev 1 – 2022/10/13, R. Rosales (rosales.r@ti.com)

- Initial revision