Embedded Coder Support Package for Texas Instruments AM26X Processors

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Examples

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Control

ADC BURST MODE EPWM

Description:

The ADC Burst Mode EPWM example sets up ePWM0 to periodically trigger a burst mode conversion of burst size 3 on ADC1 for conversion of inputs on Channel 0, Channel 1, Channel 2 and Channel 3. The interrupt ISR is used to read the results of inputs on the various channels

Example path:

examples\block_examples\adc\adc_burst_mode_epwm

Model:

Target Hardware Resource Configurations:

Pinmux: UART0_RXD and UART0_TXD
UART0: Enabled
Interrupt X-BAR 0 configured for ADC1_INT1, ADC1_INT2 and ADC1_INT3

ADC BURST MODE EPWM EXAMPLE

HWI block - key parameters

Device type: ADC
Interrupt number: 146
Instance number: 1

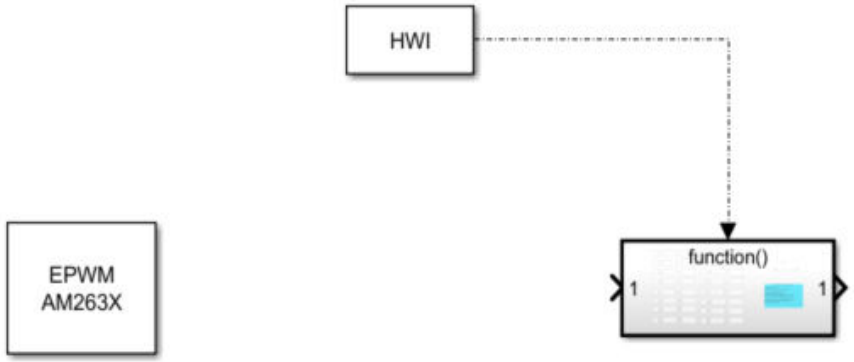
EPWM block - key parameters

Time base:
EPWM Module: EPWM0
Timer period: 1999
TBCLK: Divide clock by 4
HSCLK: Divide clock by 1
Counter mode: Up-count

Counter compare:
CMPA Value: 1000
CMPB Value: 0
CMPC Value: 0
CMPD Value: 0

Action qualifier:
CNTR CMPAU: Set high
CNTR CMPAD: Set low

Event Trigger:
Enable EPWM Interrupt: True
Enable ADC SOCA: True



Output:

```
; 4095 4095 4059 4021 4095 3957 3927 4095 4095 3839 3808 4095 4095 4095 4095 4095 4095 4095 3600 35
4095 3529 3511 4095 4095 3451 3424 4095 4095 4095 4095 4095 4095 4095 3273 3264 4094 3224 3211 4088
35 3167 3146 4076 4076 4073 4071 4069 4067 4065 3035 3028 4058 2997 2991 4052 4050 2957 2940 4040 4
 4038 4034 4032 4030 4028 2857 2854 4022 2829 2826 4015 4013 2801 2787 4003 4002 4000 3997 3995 399
990 2725 2723 3984 2702 2701 3978 3976 2683 2671 3965 3964 3963 3961 3959 3956 3954 2623 2622 3947
7 2606 3941 3938 2592 2583 3928 3928 3926 3923 3921 3919 3917 2546 2547 3910 2534 2534 3903 3901 25
2517 3892 3890 3890 3887 3884 3882 3879 2488 2489 3874 2479 2479 3866 3864 2471 2465 3855 3854 3851
50 3847 3845 3843 2443 2444 3838 2436 2436 3830 3829 2430 2427 3819 3818 3816 3814 3812 3810 3807 2
 2411 3802 2404 2404 3794 3793 2398 2396 3784 3784 3781 3778 3777 3774 3773 2383 2383 3767 2378 237
760 3757 2375 2373 3748 3747 3746 3744 3742 3739 3738 2362 2362 3730 2359 2359 3724 3723 2356 2355
3 3711 3710 3707 3705 3704 3701 2346 2346 3695 2344 2343 3688 3687 2341 2342 3678 3673 3675 3672 36
3667 3665 2334 2334 3659 2332 2332 3653 3651 2330 2331 3642 3641 3639 3637 3633 3633 3631 2324 2324
25 2324 2323 3618 3616 2321 2322 3608 3607 3605 3603 3600 3598 3595 2318 2317 3590 2317 2315 3585 3
 2314 2315 3575 3574 3571 3569 3567 3565 3564 2314 2311 3557 2311 2310 3552 3549 2309 2310 3540 353
538 3535 3533 3532 3530 2308 2305 3524 2307 2306 3518 3516 2305 2307 3508 3508 3505 3503 3501 3498
7 2304 2303 3491 2303 2302 3486 3484 2301 2304 3475 3475 3473 3471 3469 3467 3465 2302 2299 3460 23
2299 3456 3453 2299 2301 3444 3443 3443 3440 3438 3436 3433 2299 2297 3429 2299 2297 3423 3422 2297
99 3414 3412 3411 3409 3407 3406 3404 2297 2296 3398 2297 2296 3392 3391 2295 2297 3384 3382 3381 3
 3377 3375 3374 2296 2295 3368 2296 2295 3363 3360 2295 2296 3354 3352 3351 3349 3347 3346 3343 229
293 3339 2295 2293 3333 3331 2293 2296 3326 3325 3322 3320 3318 3316 3314 2295 2292 3309 2294 2292
5 3302 2293 2294 3295 3295 3293 3291 3290 3288 3286 2294 2291 3281 2293 2291 3276 3274 2292 2294 32
```

ADC BURST MODE OVERSAMPLING

Description:

This example sets up ePWM0 to periodically trigger conversions on ADC1 for inputs on channel 0, channel 1 and channel 3. The burst mode conversions are configured for SOC's that will be converting the analog values from channel 3. The ISR is configured to read the conversions results from all three channels

Example path:

examples\block_examples\adc\adc_burst_mode_oversampling

Target Hardware Resource Configurations:

Pinmux: UART0_RXD and UART0_TXD
UART0: Enabled
Interrupt X-BAR 0 configured for ADC1_INT1

ADC BURST MODE OVERSAMPLING EXAMPLE

HWI block - key parameters

Device type: ADC
Interrupt number: 146
Instance number: 1

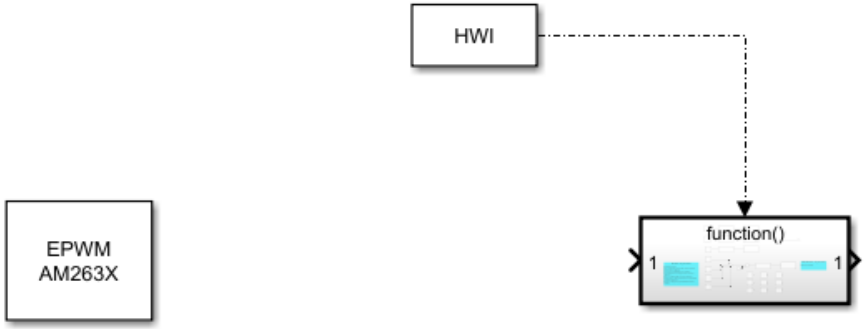
EPWM block - key parameters

Time base:
EPWM Module: EPWM0
Timer period: 1999
TBCLK: Divide clock by 4
HSCLK: Divide clock by 1
Counter mode: Up-count

Counter compare:
CMPA Value: 1000
CMPB Value: 0
CMPC Value: 0
CMPD Value: 0

Action qualifier:
CNTR CMPAU: Set high
CNTR CMPAD: Set low

Event Trigger:
Enable EPWM Interrupt: True
Event for EPWM interrupt generation: TBCTR equals CMPA when increasing
Enable ADC SOCA: True
SOCA event selection: TBCTR equals CMPA when increasing



Output

```
3207 3207 3205 3207 3207 3205 3207 3207 3205 3207 3207 3205 3207 3207 3205 3207 3207 3205 3207 3207 3205 3207 3207 3205
3207 3207 3205 3207 3207 3205 3207 3207 3205 3207 3207 3205 3207 3207 3205 3207 3207 3205 3207 3207 3205 3207 3207 3205
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3207 3207 3205 3207 3207 3205 3207 3207 3205
```

ADC DIFFERENTIAL MODE

Description:

This example sets up ePWM0 to periodically trigger SOC0 and SOC1 on ADC1 for conversion of inputs on ADC_AIN0 and ADC_AIN1 in differential modes(ADC_AIN0-ADC_AIN1) on SOC0 and (ADC-AIN1-ADC_AIN0) on SOC1

Example path:

examples\block_examples\adc\adc_differential_mode

Model:

Target Hardware Resource Configurations:

Pinmux: UART0_RXD and UART0_TXD
UART0: Enabled
Interrupt X-BAR 0 configured for ADC1_INT1

ADC DIFFERENTIAL MODE EXAMPLE

HWI block - key parameters

Device type: ADC
Interrupt number: 146
Instance number: 1

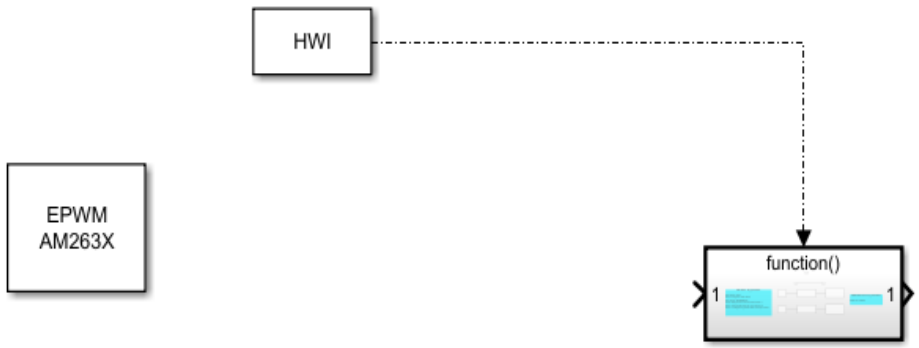
EPWM block - key parameters

Time base:
EPWM Module: EPWM0
Timer period: 1999
TBCLK: Divide clock by 4
HSCLK: Divide clock by 1
Counter mode: Up-count

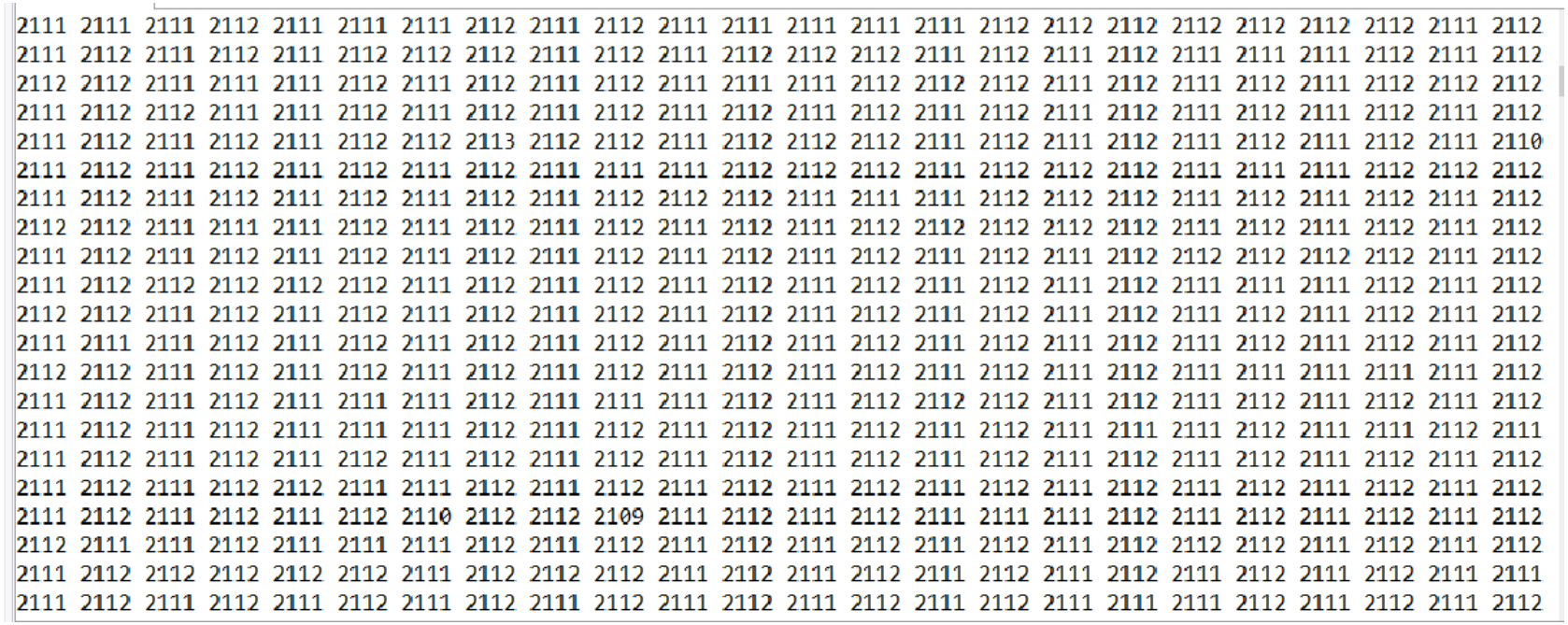
Counter compare:
CMPA Value: 1000
CMPB Value: 0
CMPC Value: 0
CMPD Value: 0

Action qualifier:
CNTR CMPAU: Set high
CNTR CMPAD: Set low

Event Trigger:
Enable EPWM Interrupt: True
Event for EPWM interrupt generation: TBCTR equals CMPA when increasing
Enable ADC SOCA: True
SOCA event selection: TBCTR equals CMPA when increasing



Output:



ADC MULTIPLE SOC EPWM

Description:

This example sets up ePWM0 to periodically trigger conversions SOC0, SOC1, SOC2 on both ADC1 and ADC2. This example demonstrates multiple ADCs working together to process a batch of conversions

Example path:

examples\block_examples\adc\adc_multiple_soc_epwm

Model:

Target Hardware Resource Configurations:

Pinmux: UART0_RXD and UART0_TXD
UART0: Enabled
Interrupt X-BAR 0 configured for ADC2_INT1

ADC MULTIPLE SOC EPWM EXAMPLE

HWI block - key parameters

Device type: ADC
Interrupt number: 146
Instance number: 2

EPWM block - key parameters

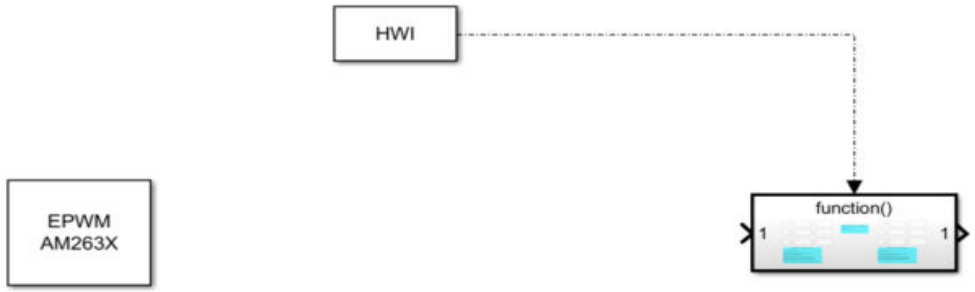
Time base:
EPWM Module: EPWM0
Timer period: 2000
TBCLK: Divide clock by 4
HSCLK: Divide clock by 1
Counter mode: Up-count

Counter compare:
CMPA Value: 1000
CMPB Value: 0
CMPC Value: 0
CMPD Value: 0

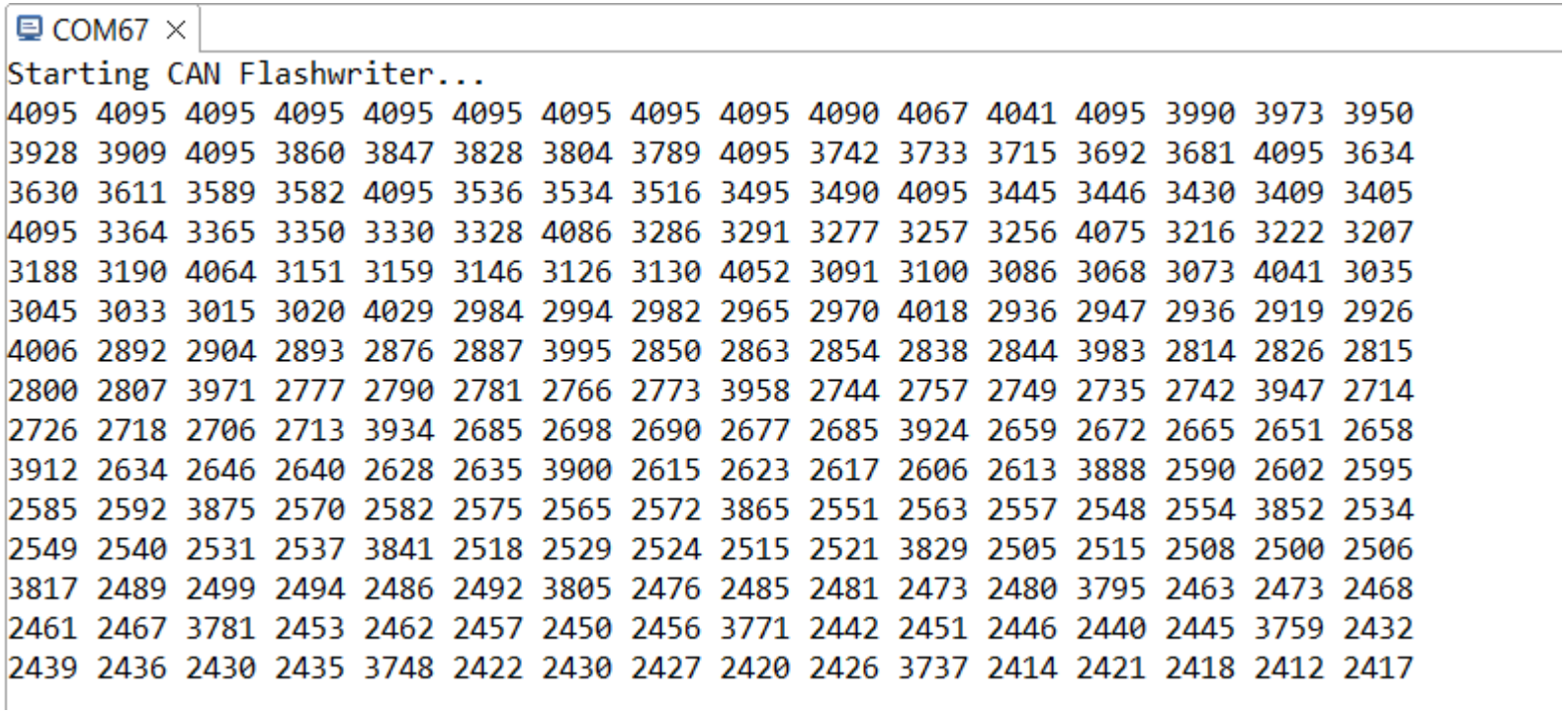
Action qualifier:
CNTR CMPAU: Set high
CNTR CMPAD: Set low

Event Trigger:

Enable ADC SOCA: True
SOCA event selection: TBCTR equals CMPA when increasing



Output:



ADC SOC EPWM

Description:

The ADC SOC EPWM example demonstarated periodic triggering of conversion on ADC1 by EPWM0. For ADC1, SOC 0 is what gets triggered by EPWM0. The SOC0 sample on channel 0 of ADC1. Additionally, ADCINT1 is configured to generate an interrupt with SOC0 being the source of this interrupt. The ISR that gets called on receiving the interrupt reads SOC0 results, after which it clear ADC1INT1 flag

Example path:

examples\block_examples\adc\adc_soc_epwm

Model:

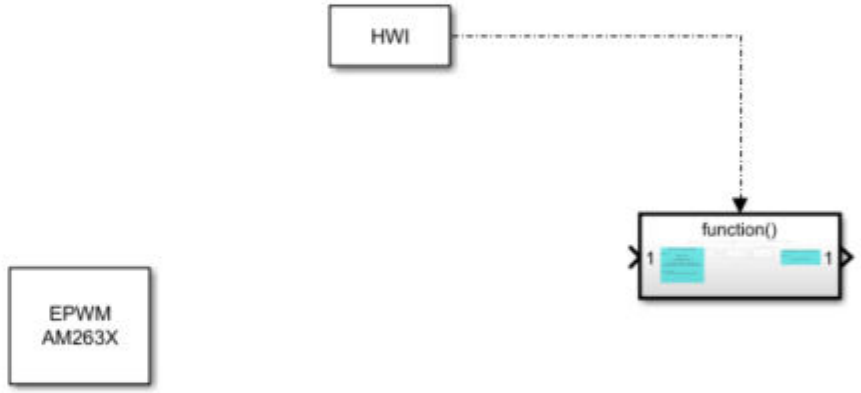
Target Hardware Resource Configurations:

Pinmux: UART0_RXD and UART0_TXD
UART0: Enabled
Interrupt X-BAR 0 configured for ADC0_INT1

ADC SOC EPWM EXAMPLE

R5 HWI Interrupt block - key parameters

Device Type: ADC
Interrupt Number: 146
Instance Number: 1



EPWM block - key parameters

Time Base

Module: EPWM0
Timer Period: 2000
Counter Mode: Up count

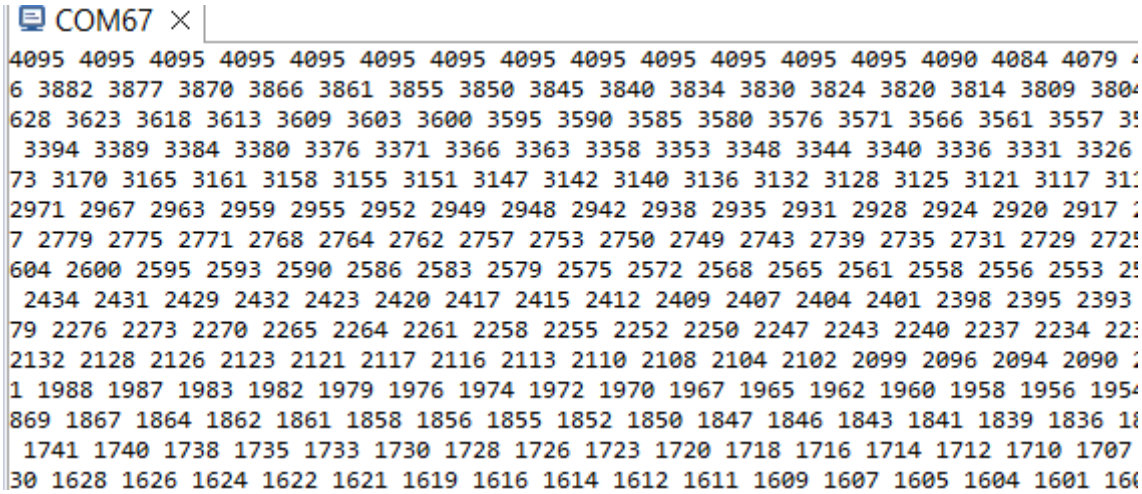
Counter Compare

CMPA value: 1000
CMPB value: 0
CMPC value: 0
CMPD value: 0

Event Trigger

Enable ADC SOC for module A == True
SOC for module A event selection == Tbctr equal to zero
Number of event for SOC to generate == 1 event

Output:



ADC PPB DELAY

Description:

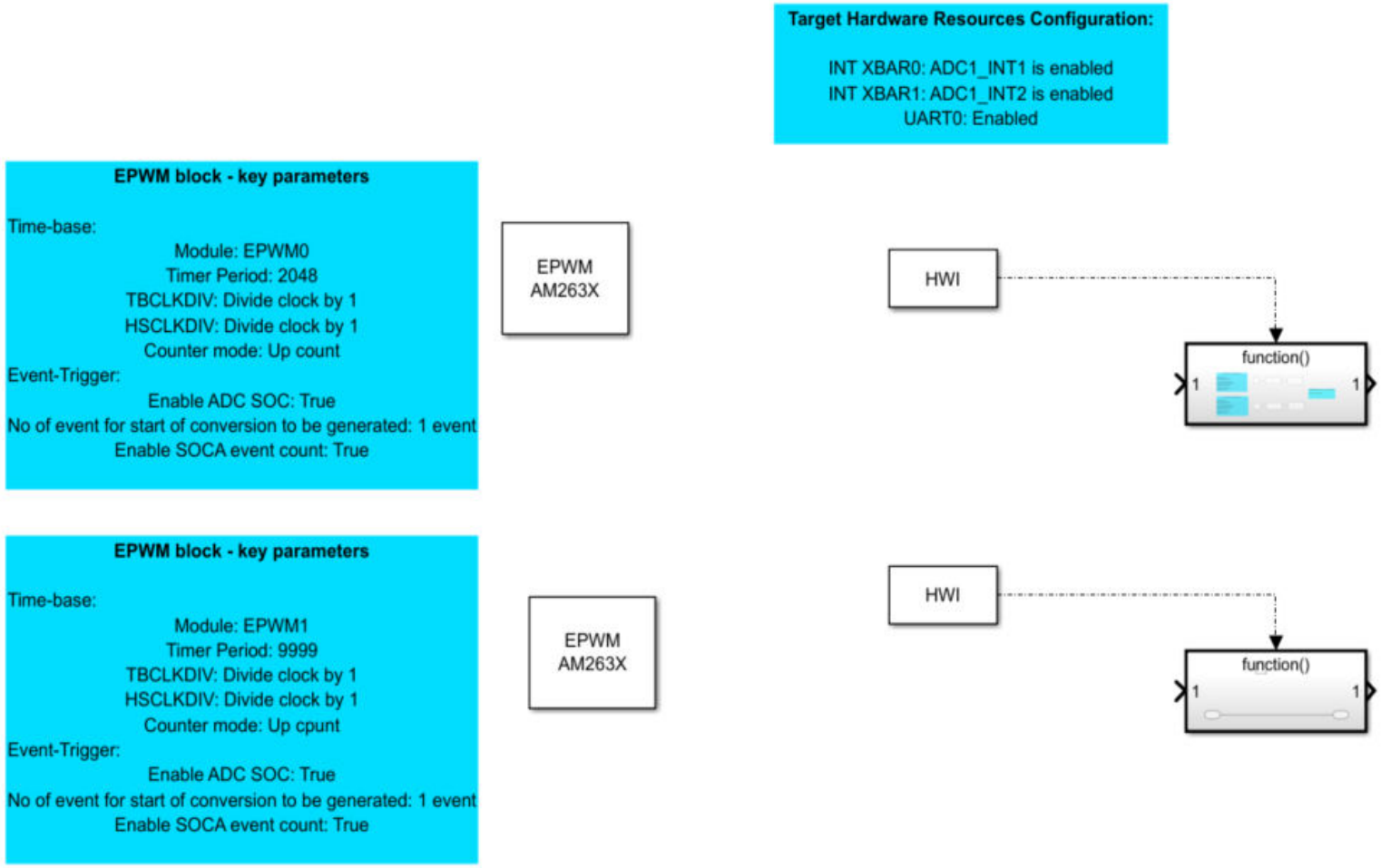
This example demonstrates the PPB delay time stamp feature of ADC, The PPBs in ADC offer timestamping the delay between SOC conversion and trigger for SOC

Example path:

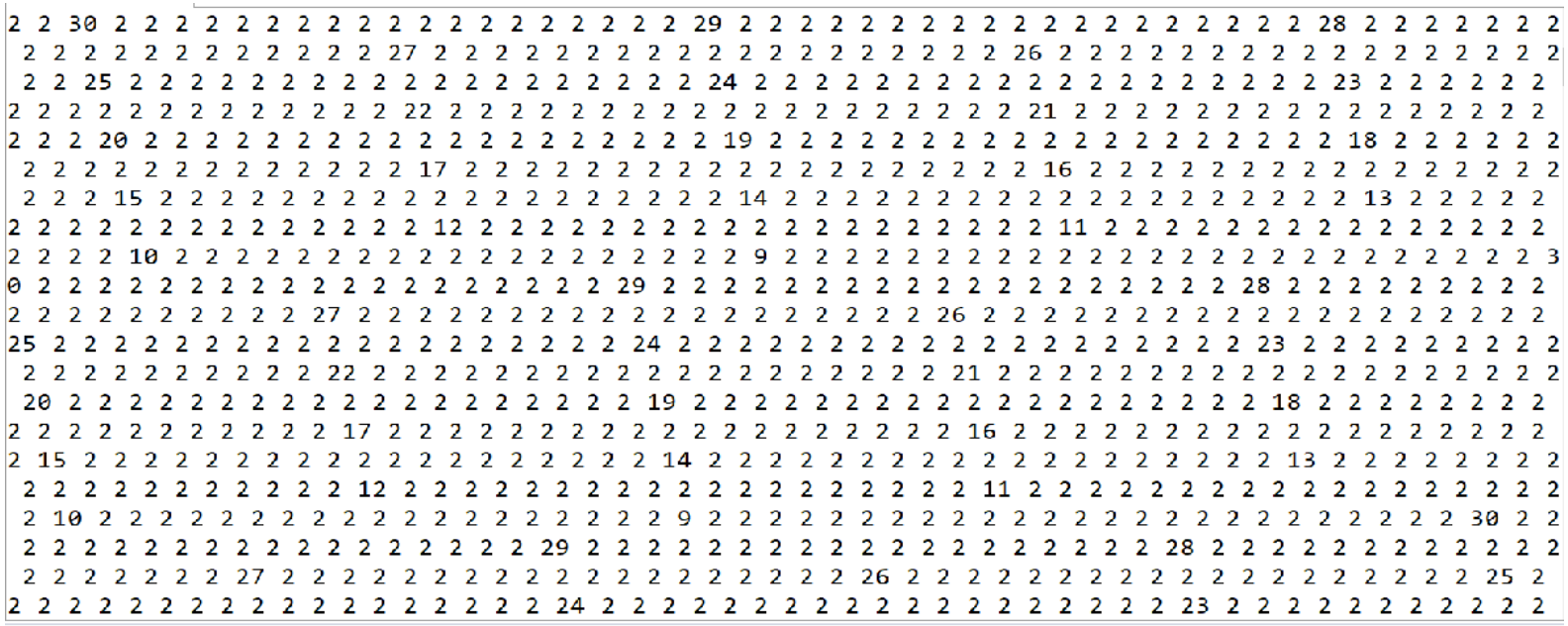
examples\block_examples\adc\adc_ppb_delay

Model:

ADC PPB DELAY EXAMPLE



Output:



ADC PPB OFFSET

Description:

This example demonstrates the PPB offset feature of the Post Processing Block of ADC. The PPB offset feature is as follows:

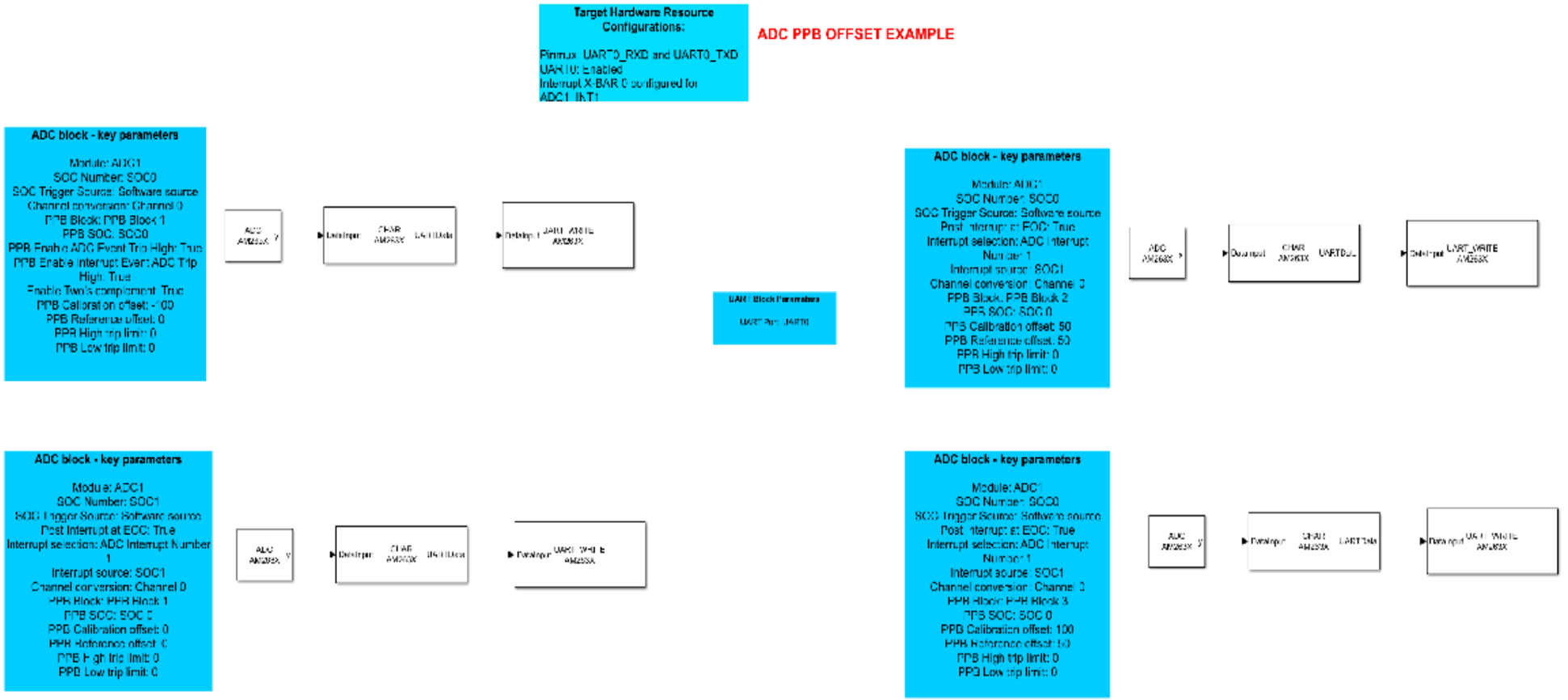
1) PPB Calibration Offset: This is used for setting calibration offset of SOC result, ADC SOC result = ADC result - PPB Calibration value

2) PPB Reference Offset: This is used to calculate an offset from a given reference, PPB result corresponding to given SOC = ADC result - PPB reference

Example path:

examples\block_examples\adc\adc_ppb_offset

Model:


Target Hardware Resource Configurations:
Pinmux: UART0_RXD and UART0_TXD
UART0: Enabled
Interrupt X-BAR 0 configured for
ADC1_INT1
ADC PPB OFFSET EXAMPLE
ADC block - key parameters
Module: ADC1
SOC Number: SOC0
SOC Trigger Source: Software source
Channel conversion: Channel 0
PPB Block: PPB Block 1
PPB SOC: SOC0
PPB Enable ADC Event Trip High: True
PPB Enable Interrupt Event: ADC Trip High: True
Enable Two's complement: True
PPB Calibration offset: -100
PPB Reference offset: 0
PPB High trip limit: 0
PPB Low trip limit: 0
UART Block Parameters
UART Port: UART0
ADC block - key parameters
Module: ADC1
SOC Number: SOC0
SOC Trigger Source: Software source
Post Interrupt at EOC: True
Interrupt selection: ADC Interrupt Number 1
Interrupt source: SOC1
Channel conversion: Channel 0
PPB Block: PPB Block 2
PPB SOC: SOC 0
PPB Calibration offset: 50
PPB Reference offset: 50
PPB High trip limit: 0
PPB Low trip limit: 0
ADC block - key parameters
Module: ADC1
SOC Number: SOC1
SOC Trigger Source: Software source
Post Interrupt at EOC: True
Interrupt selection: ADC Interrupt Number 1
Interrupt source: SOC1
Channel conversion: Channel 0
PPB Block: PPB Block 1
PPB SOC: SOC 0
PPB Calibration offset: 0
PPB Reference offset: 0
PPB High trip limit: 0
PPB Low trip limit: 0
ADC block - key parameters
Module: ADC1
SOC Number: SOC0
SOC Trigger Source: Software source
Post Interrupt at EOC: True
Interrupt selection: ADC Interrupt Number 1
Interrupt source: SOC1
Channel conversion: Channel 3
PPB Block: PPB Block 3
PPB SOC: SOC 0
PPB Calibration offset: 100
PPB Reference offset: 50
PPB High trip limit: 0
PPB Low trip limit: 0

Output:

```
0 16 16 16 0 16 16 16 0 16 16 16 0 16 16 16 0 16 16 16 0 16 16 16 0 16 16 16 0 16 16 16 0 1
6 16 16 0 16 16 16 0 16 16 16 0 16 16 16 0 16 16 16 0 16 16 16 0 16 16 16 0 16 16 16 0 16 1
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 0 16 16 16 0 16 16 16 0 16 16 16 0 16 16 16 0 16 16 16 0 16 16 16 0 16 16 16 0 16 16 16 0
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16 16 0 16 16 16 0 16 16 16 0 16 16 16 0 16 16 16 0 16 16 16 0 16 16 16 0 16 16 16 0 16 16
16 0 16 16 16 0 16 16 16 0 16 16 16 0 16 16 16 0 16 16 16 0 16 16 16 0 16 16 16 0 16 16 16
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16 16 0 16 16 16 0 16 16 16 0 16 16 16 0 16 16 16 0 16 16 16 0 16 16 16 0 16 16 16 0 16 16
```

ADC SOC CONTINUOUS

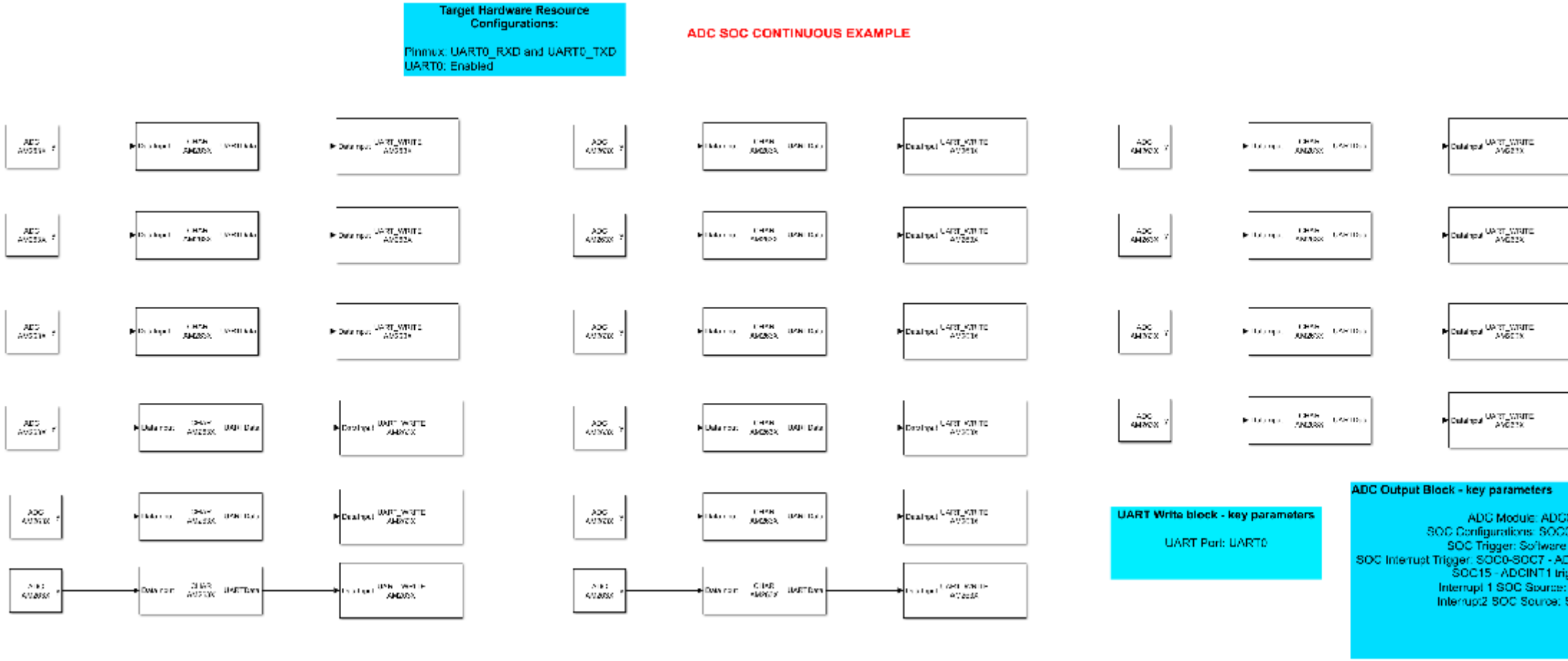
Description:

This example converts ADC1 Channel 0 on all its SOC configurations, acheiving full sampling rate on input signal on given channel

Example path:

examples\block_examples\adc\adc_soc_continuous

Model:


Target Hardware Resource Configurations:
Pinmux: UART0_RXD and UART0_TXD
UART0: Enabled
ADC SOC CONTINUOUS EXAMPLE
UART Write block - key parameters
UART Port: UART0
ADC Output Block - key parameters
ADC Module: ADC
SOC Configurations: SOC
SOC Trigger: Software
SOC Interrupt Trigger: SOC0-SOC7 - AD
SOC15 - ADCINT1 trig
Interrupt 1 SOC Source:
Interrupt2 SOC Source:

Output:

```
4095 4095 4095 4095 4095 4095 4095 0 0 0 3642 3440 0 0 0 3025 1082 1082 1083 1083 1083 1082 1082 1082
1082 1083 1082 1082 1083 1082 1082 1082 1083 1083 1083 1083 1082 1083 1083 1082 1082 1082 1082 1082 10
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3 1082 1082 1082 1083 1083 1082 1082 1082 1082 1082 1083 1082 1082 1083 1082 1082 1082 1083 1081 1083
```

ADC SOC Software

Description:

This example uses the ADC to perform an ADC SOC conversion triggered by software. The configured ADC module is ADC0, and SOC0 is to be triggered by software. Additionally, ADCINT1 is enabled and is configured to be generated at end of conversion of SOC0. This examples demonstartes forcing SOC0 through software and then capturing ADC results

Example path:

examples\block_examples\adc\adc_soc_software

Model:

Target Hardware Resource Configurations:

Pinmux: UART0_RXD and UART0_TXD
UART0: Enabled

ADC SOC SOFTWARE EXAMPLE

ADC block - key parameters

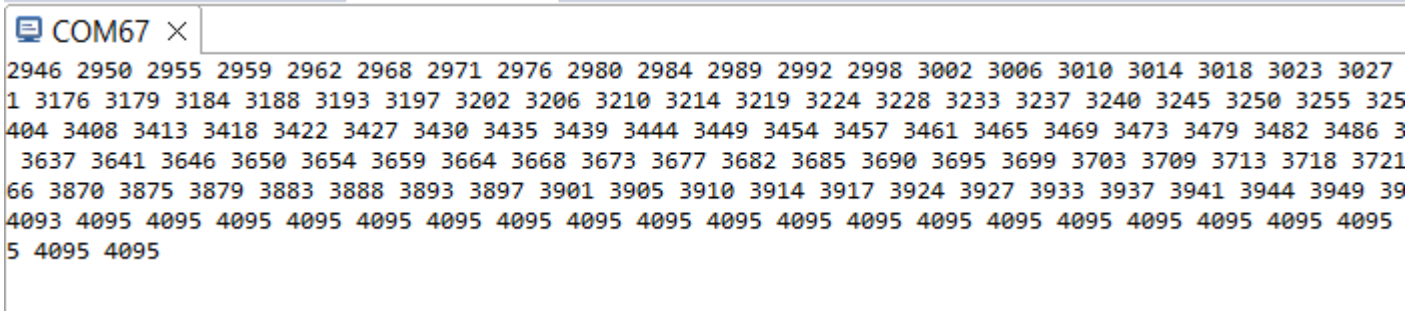
General
Module: ADC0
Prescaler: 4.0
SOC Trigger No: SOC0
SOC Trigger Source: Software Source
Post Interrupt: True
Interrupt Number: ADC Interrupt 1

Input Channels
Channel: Channel 2

UART Write block - key parameters

General
UART Port: UART0

Output:



ADC SOC OVERSAMPLING

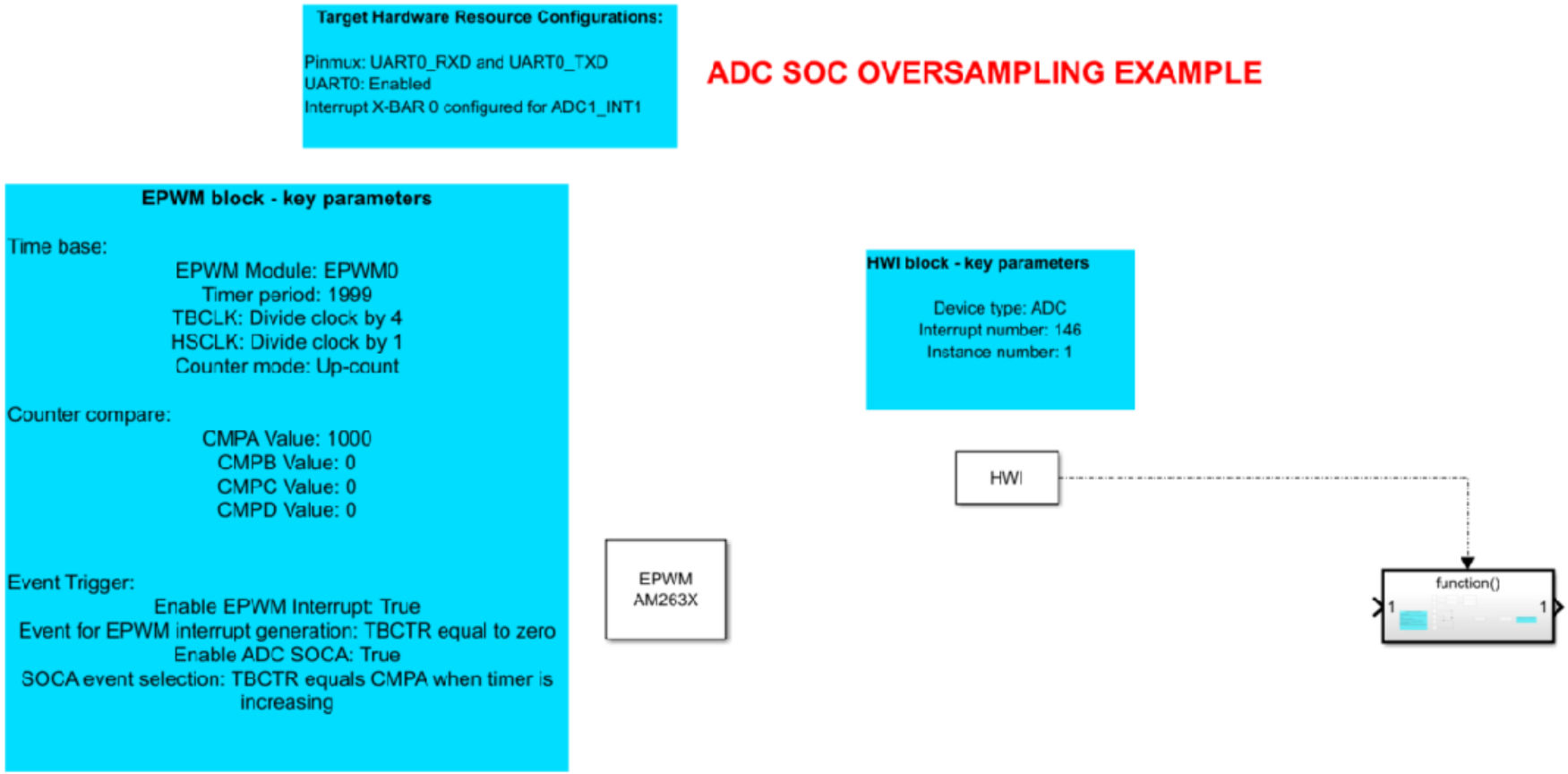
Description:

This example shows oversamping on a given ADC channel, periodically triggered by EPWM. ADC1 Channel 2 is sampled by SOC (2-5) and are triggered by EPWMSOCA along with SOC 0 (sampling channel 0) and SOC 1 (sampling Channel 1).

Example path:

examples\block_examples\adc\adc_soc_oversampling

Model:



Output:

```
Starting CAN Flashwriter...
4095 4095 16380 4095 4064 15734 4095 3790 14535 4095 3563 13559 4095 3376 12755 4072 321
7 12081 4045 3083 11524 4019 2970 11049 3992 2875 10652 3966 2792 10315 3939 2723 10028
3912 2662 9788 3886 2613 9598 3862 2572 9428 3836 2534 9272 3809 2503 9142 3784 2475 902
9 3759 2450 8931 3733 2429 8849 3708 2412 8780 3684 2395 8720 3659 2381 8668
```

ADC SOC SOFTWARE SYNC

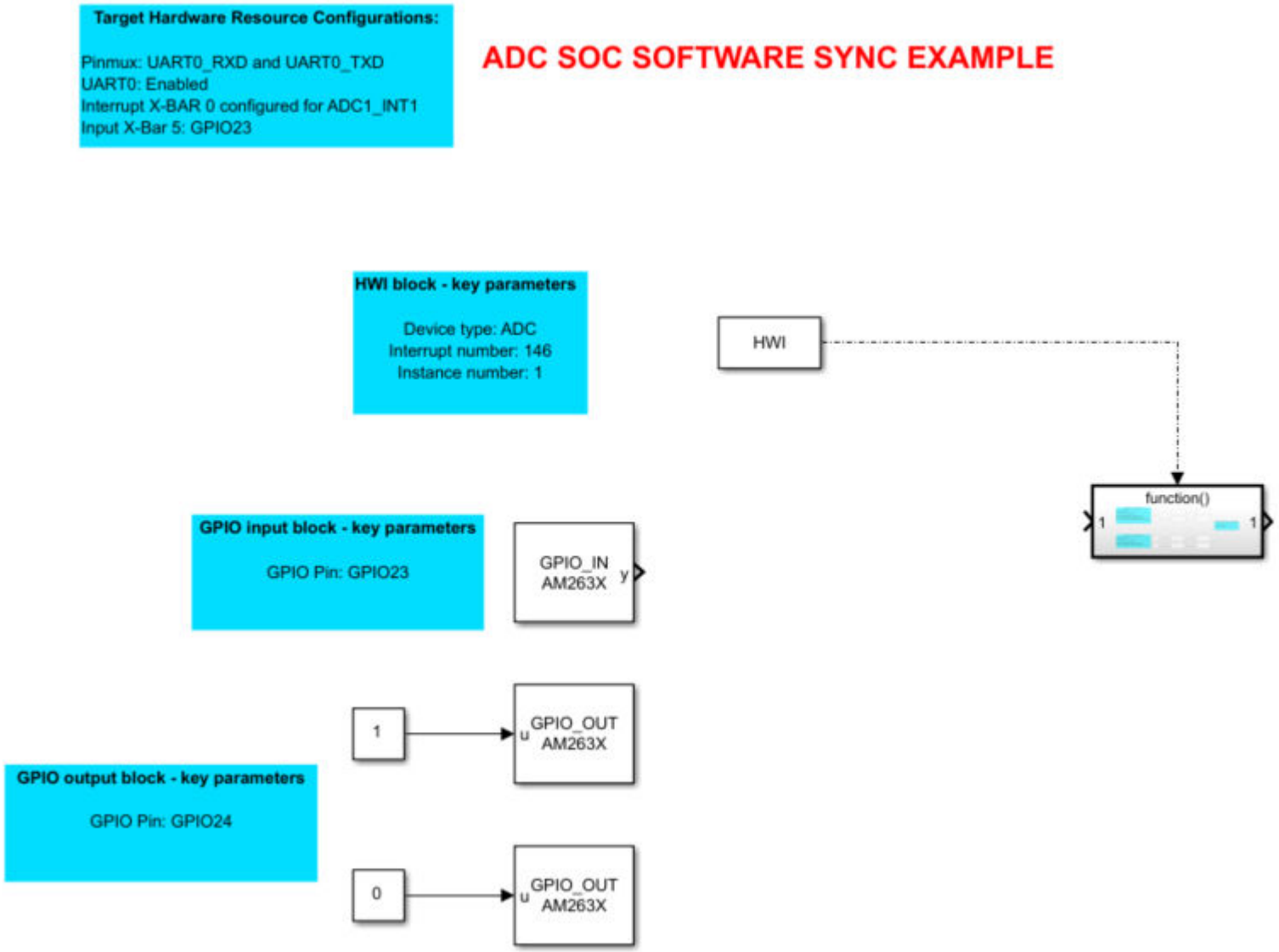
Description:

This example shows synchronous operation on ADC1 and ADC2 trigger by a software forced by toggling a GPIO. The example uses a GPIO loopb into the INPUTBAR[5] as trigger for the SOC in the given ADC and uses software to toggle to the loopback GPIO trigger the conversions.

Example path:

examples\block_examples\adc\adc_soc_software_sync

Model:


Target Hardware Resource Configurations:
Pinmux: UART0_RXD and UART0_TXD
UART0: Enabled
Interrupt X-BAR 0 configured for ADC1_INT1
Input X-Bar 5: GPIO23
ADC SOC SOFTWARE SYNC EXAMPLE
HWI block - key parameters
Device type: ADC
Interrupt number: 146
Instance number: 1
HWI
function()
1
1
GPIO input block - key parameters
GPIO Pin: GPIO23
GPIO_IN
AM263X
y
1
u
GPIO_OUT
AM263X
GPIO output block - key parameters
GPIO Pin: GPIO24
0
u
GPIO_OUT
AM263X

Output:

```
Starting CAN Flashwriter...
1508 4095 1513 4095 1519 4095 1522 4095 1529 4095 1533 4095 1539 4095 1542 4095 1548 4095 1550 4095 1558 4095 1561 4095 1
568 4095 1571 4095 1578 4095 1582 4095 1588 4095 1591 4095 1597 4095 1601 4095 1608 4095 1610 4095 1618 4095 1621 4095 16
28 4095 1631 4095 1638 4095 1640 4095 1647 4095 1650 4095 1656 4095 1659 4095 1667 4095 1670 4095 1677 4095 1680 4095 168
6 4095 1689 4095 1695 4095 1699 4095 1705 4095 1709 4095 1715 4095 1719 4095 1725 4095 1728 4095 1735 4095 1738 4095 1745
 4095 1747 4095 1754 4095 1757 4095 1764 4095 1766 4095 1774 4095 1777 4095 1783 4095 1786 4095 1793 4095 1796 4095 1803
4095 1805 4095 1812 4095 1815 4095 1822 4095 1825 4095 1831 4095 1834 4095 1841 4095 1846 4095 1851 4095 1854 4095 1860 4
095 1862 4095 1870 4095 1873 4095 1880 4095 1882 4095 1889 4095 1892 4095 1898 4095 1901 4095 1908 4095 1911 4095 1917 40
95 1921 4095 1927 4095 1931 4095 1937 4095 1940 4095 1946 4095 1949 4095 1956 4095 1959 4095 1966 4095 1969 4095 1976 409
5 1979 4095 1986 4095 1989 4095 1995 4095 1999 4095 2004 4095 2007 4095 2014 4095 2017 4095 2023 4095 2026 4095 2033 4095
 2035 4095 2042 4095 2046 4095 2053 4095 2055 4095 2060 4095 2065 4095 2070 4095 2074 4095 2081 4095 2084 4095 2090 4095
2092 4095 2099 4095 2102 4095 2108 4095 2111 4095 2118 4095 2120 4095 2128 4095 2130 4095 2137 4095 2139 4095 2147 4095 2
149 4095 2156 4095 2160 4095 2165 4095 2168 4095 2175 4095 2177 4095 2183 4095 2186 4095 2193 4095 2196 4095 2202 4095 22
07 4095 2214 4095 2214 4095 2221 4095 2224 4095 2230 4095 2232 4095 2239 4095 2242 4095 2249 4095 2252 4095 2258 4095 226
0 4095 2267 4095 2270 4095 2276 4095 2279 4095 2286 4095 2289 4095 2295 4095 2298 4095 2304 4095 2306 4095 2313 4095 2316
 4095 2323 4095 2325 4095 2331 4095 2335 4095 2341 4095 2345 4095 2351 4095 2354 4095 2360 4095 2362 4095 2369 4095 2372
4095 2378 4095 2380 4095 2387 4095 2390 4095 2396 4095 2399 4095 2406 4095 2409 4095 2415 4095 2417 4095 2423 4095 2426 4
095 2433 4095 2435 4095 2442 4095 2445 4095 2451 4095 2454 4095 2459 4095 2462 4095 2468 4095 2471 4095 2478 4095 2481 40
95 2487 4095 2489 4095 2496 4095 2497 4095 2505 4095 2507 4095 2513 4095 2515 4095 2522 4095 2528 4095 2531 4095 2533 409
5 2540 4095 2542 4095 2549 4095 2552 4095 2557 4095 2560 4095 2566 4095 2569 4095 2575 4095 2578 4095 2585 4095 2587 4095
 2596 4095 2602 4095 2605 4095 2611 4095 2613 4095 2619 4095 2622 4095 2628 4095 2631 4095 2638 4095 2640 4095 2645 4095 2
2655 4095 2658 4095
```

EPWM Chopper:

Description:

This example allows a carrier signal to modulate PWM waveform generated by action-qualifier and dead-band submodule, by configuring Chopping(carrier) frequency, programmable puse width of first pulse and duty cycle

Example path:

examples\block_examples\epwm\epwm_c hopper

Model:

Target hardware resource configurations

Pinmux: EPWM0_A, EPWM1_A, EPWM2_A, EPWM3_A, EPWM3_B

EPWM CHOPPER EXAMPLE

EPWM block - key parameters

Time Base:
Module: EPWM0
Counter Mode: Up count
Timer period: 19999

Counter Compare:
CMPA value: 100
CMPB value: 10999
CMPC value: 0
CMPD value: 0

Action qualifier:
CNTR is equal to CMPAU: Set output pins to high
CNTR is equal to CMPBU: Set output pins to low

EPWM AM263X

EPWM AM263X

EPWM block - key parameters

Time Base:
Module: EPWM1
Counter Mode: Up count
Timer period: 19999

Counter Compare:
CMPA value: 100
CMPB value: 10999
CMPC value: 0
CMPD value: 0

Action qualifier:
CNTR is equal to CMPAU: Set output pins to high
CNTR is equal to CMPBU: Set output pins to low

Chopper:
Duty cycle: 1/8 Duty
Chopper Frequency: SYSCLOCKOUT/5
Chopper first pulse width: 16

EPWM block - key parameters

Time Base:
Module: EPWM2
Counter Mode: Up count
Timer period: 19999

Counter Compare:
CMPA value: 100
CMPB value: 10999
CMPC value: 0
CMPD value: 0

Action qualifier:
CNTR is equal to CMPAU: Set output pins to high
CNTR is equal to CMPBU: Set output pins to low

Chopper:
Duty cycle: 6/8 Duty
Chopper Frequency: SYSCLOCKOUT/5
Chopper first pulse width: 16

EPWM AM263X

EPWM AM263X

EPWM block - key parameters

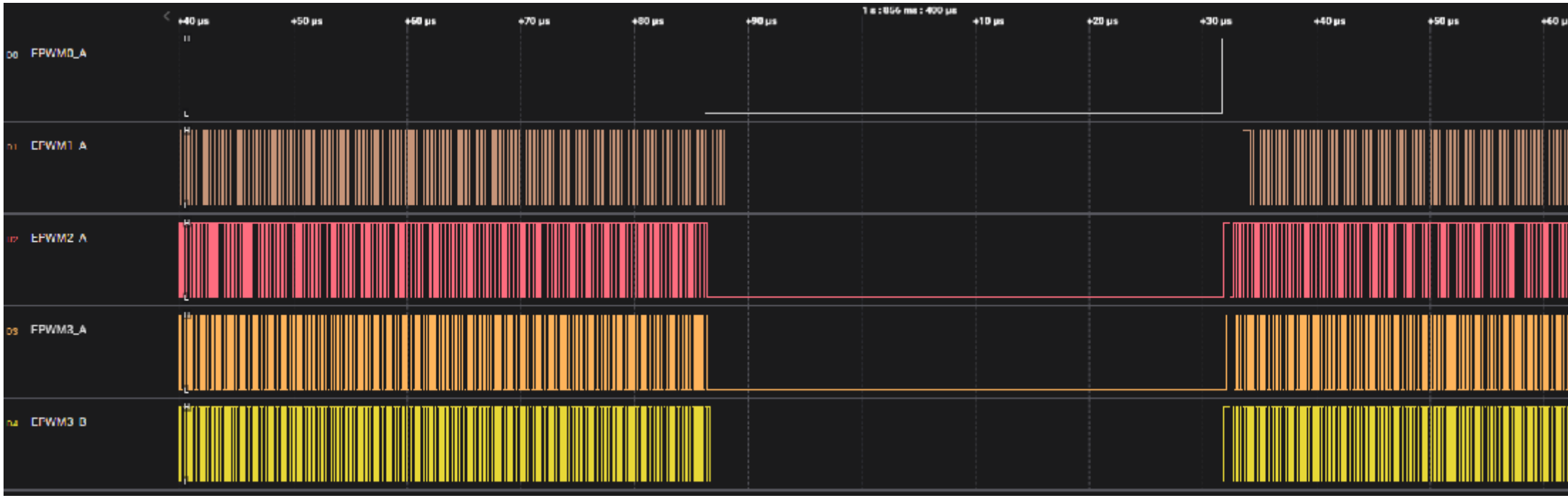
Time Base:
Module: EPWM3
Counter Mode: Up count
Timer period: 19999

Counter Compare:
CMPA value: 100
CMPB value: 10999
CMPC value: 0
CMPD value: 0

Action qualifier:
CNTR is equal to CMPAU: Set output pins to high
CNTR is equal to CMPBU: Set output pins to low

Chopper:
Duty cycle: 4/8 Duty
Chopper Frequency: SYSCLOCKOUT/7
Chopper first pulse width: 16

Output:



EPWM deadband

Description:

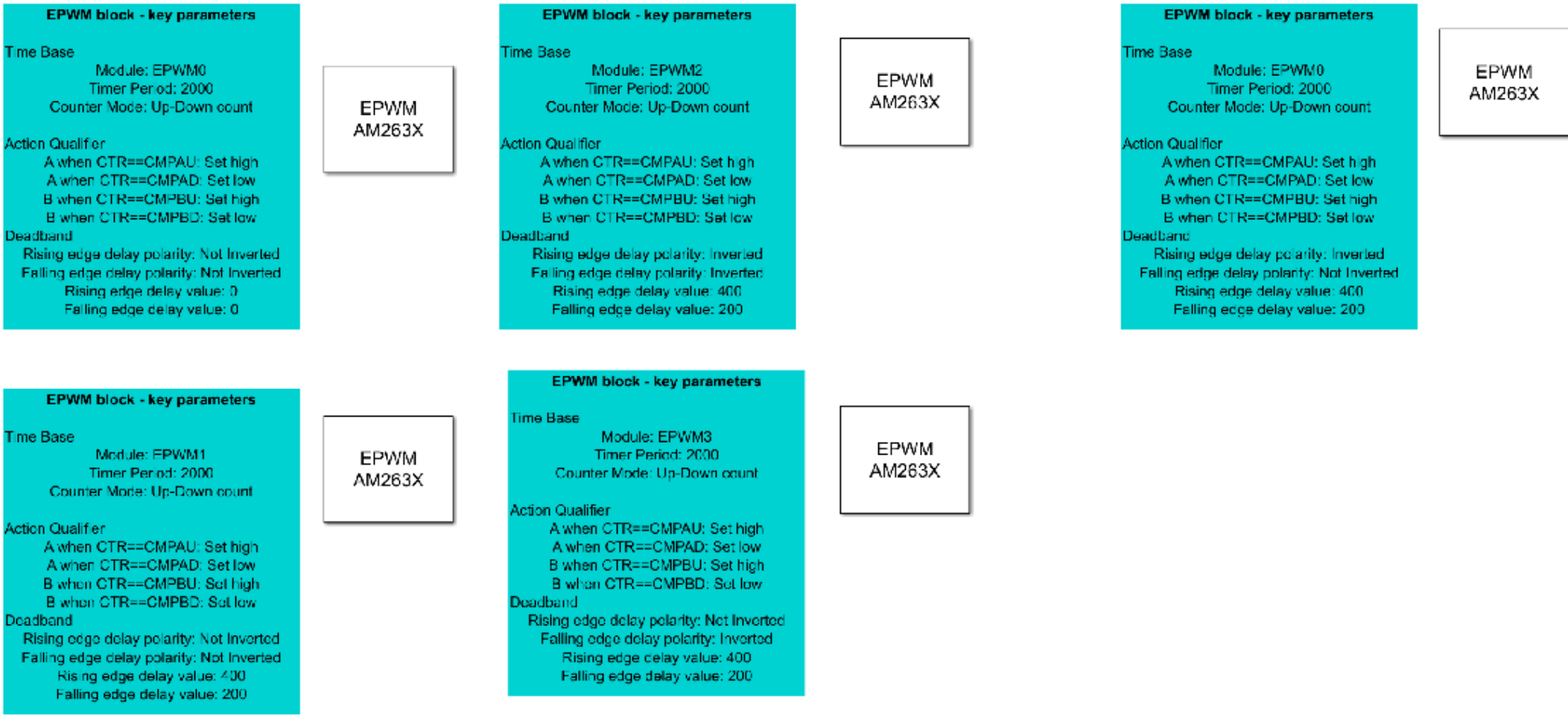
The EPWM Deadband example is used to showcase the features of deadband submodule. 6 EPWM modules are configured with varying deadband features and EPWM0 is taken as the reference whose Deadband is disabled

Example path:

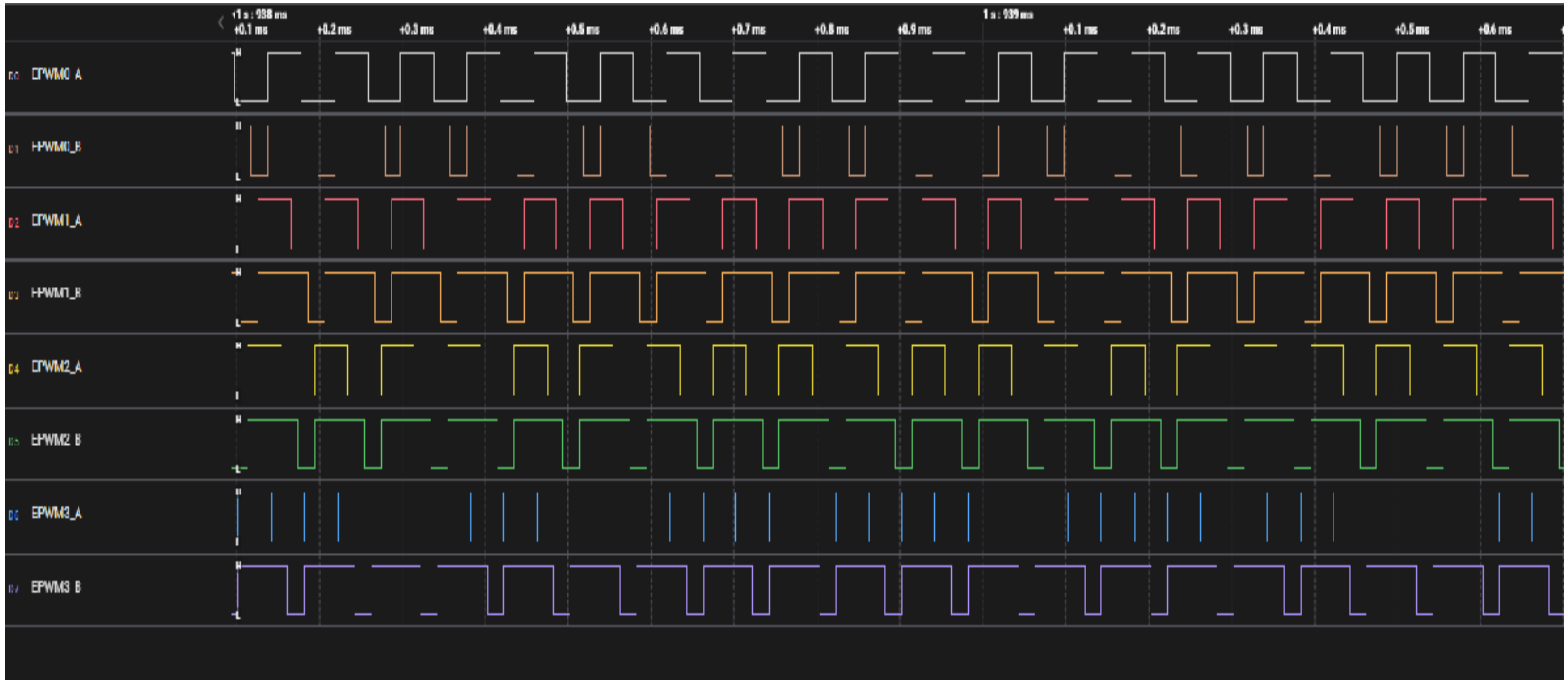
examples\block_examples\epwm\epwm_deadband

Model:

EPWM Deadband Example



Output:



EPWM Synchronization

Description:

The EPWM Synchronization example is used to showcase the synchronization feature of EPWM. 5 EPWM modules are configured with EPWM 0 taken as reference and other EPWM modules are phase shifted with respect to the first EPWM module. The sync in source for EPWM 1-EPWM 4 is EPWM 0 sync-out signal. On receiving this sync-in source, these EPWM module counter value will start counting from the phase shift value up until the configured period value.

Example path:

examples\block_examples\epwm\epwm_deadband

Model:

Target Hardware Resource Configuration

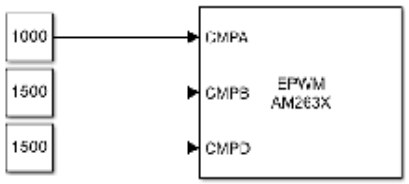
Pinmux Enable: EPWM0A, EPWM0B, EPWM1A, EPWM1B, EPWM2A, EPWM2B, EPWM3A, EPWM3B

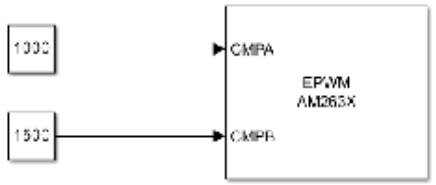
EPWM SYNCHRONIZATION EXAMPLE

EPWM block - key parameters

Time Base
Module: EPWM0
Timer Period: 2000
Counter Mode: Up count

Action Qualifier
A when CTR==Zero: Set high
A when CTR==CMPAU: Set low





EPWM block - key parameters

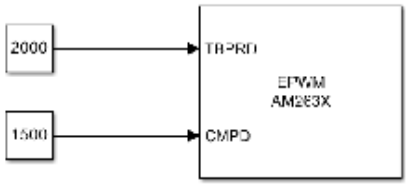
Time Base
Module: EPWM2
Timer Period: 2000
Counter Mode: Up count
Sync in source: EPWM sync-out
Phase Shift Value: 600

Action Qualifier
A when CTR==Zero: Set high
A when CTR==CMPAU: Set low

EPWM block - key parameters

Time Base
Module: EPWM1
Timer Period: 2000
Counter Mode: Up count
Sync in source: EPWM sync-out
Phase Shift Value: 300

Action Qualifier
A when CTR==Zero: Set high
A when CTR==CMPAU: Set low

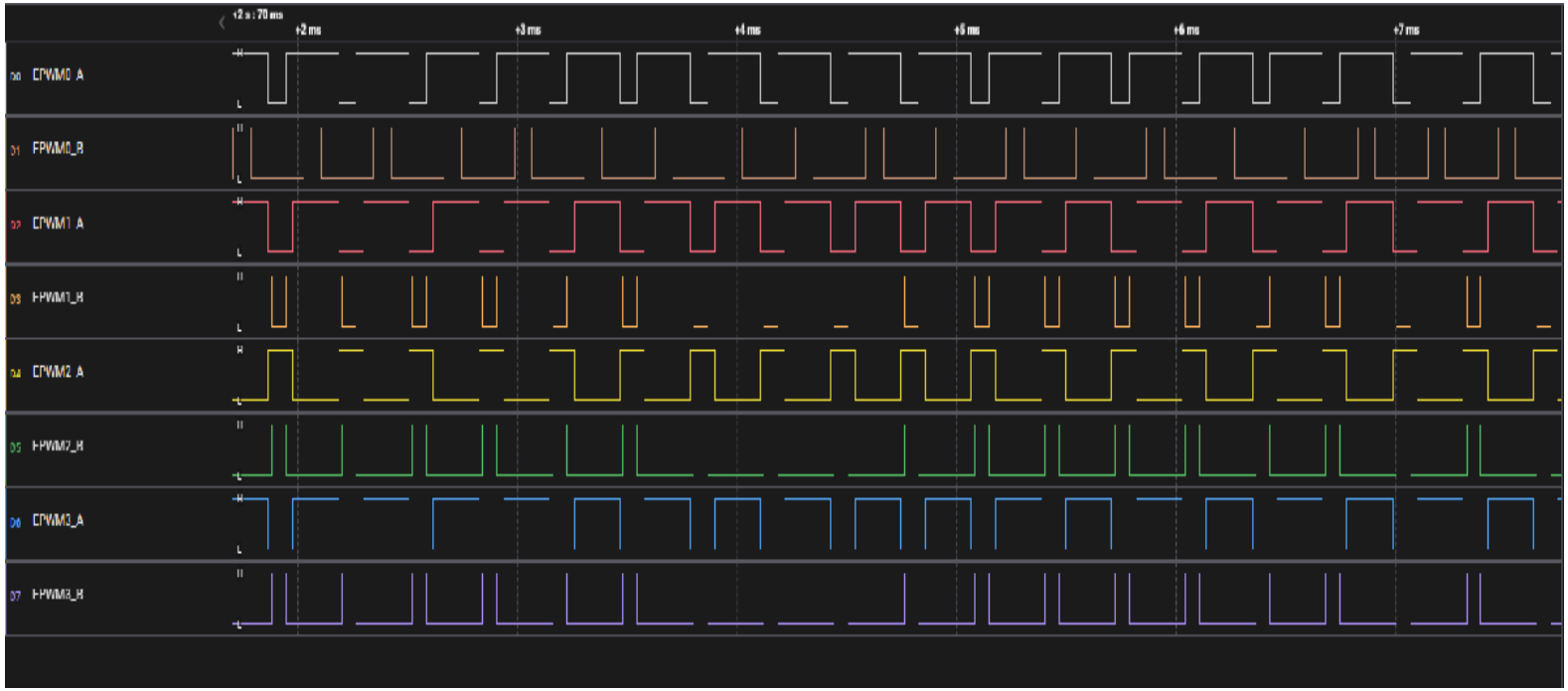


EPWM block - key parameters

Time Base
Module: EPWM3
Timer Period: 2000
Counter Mode: Up count
Sync in source: EPWM sync-out
Phase Shift Value: 900

Action Qualifier
A when CTR==Zero: Set high
A when CTR==CMPAU: Set low

Output:



EPWM TRIP ZONE

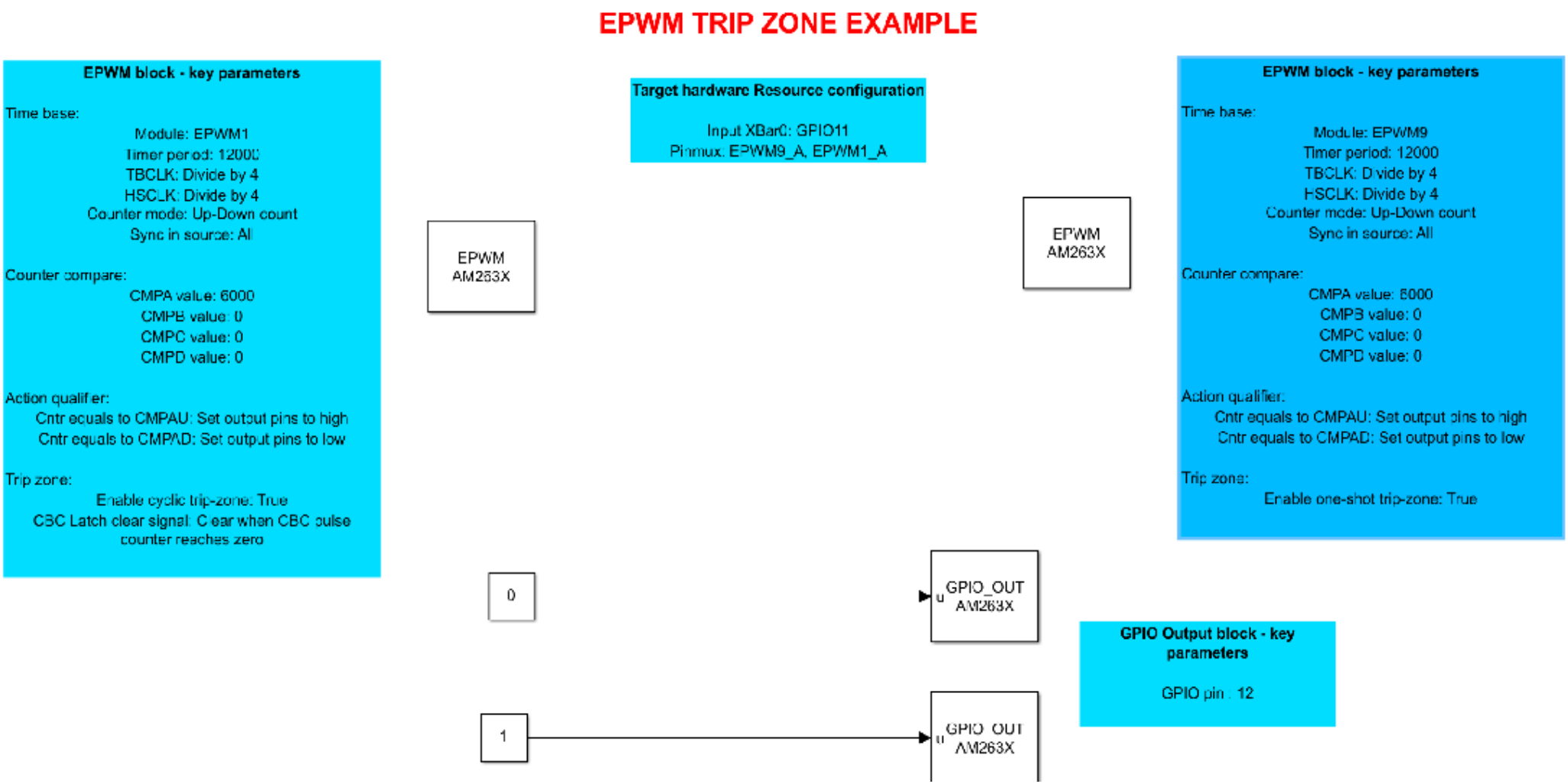
Description:

This example configures EPWM9 and EPWM1 using trip zone sudmodule. EPWM9 has TZ1 as one shot trip source and EPWM1 has TZ1 as cycle-by-cycle trip source. On receiving the trip trigger, EPWM9 output configured for one-shot trip will change to trip state forever. EPWM1 output configured for cycle-by-cycle will trip on receiving the epwm trigger and will recover when the event configured for clearing CBC latch occurs.

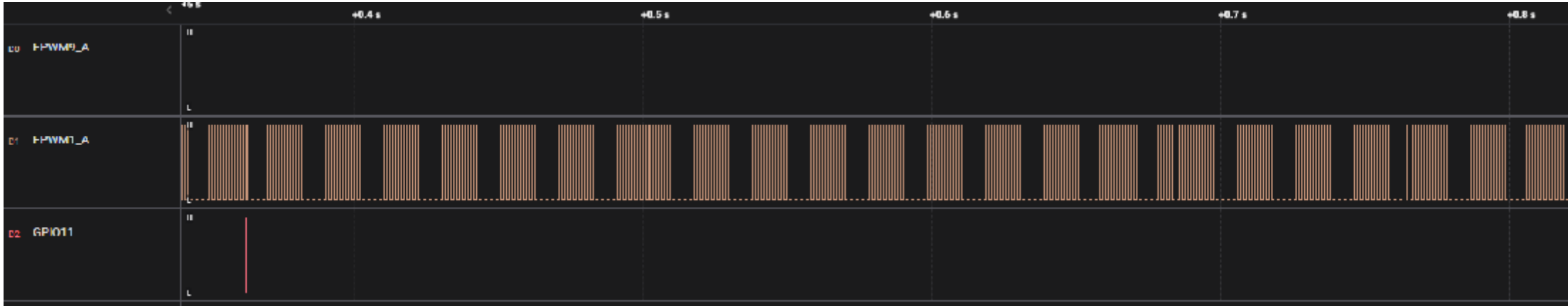
Example path:

examples\block_examples\epwm\epwm_trip_zone

Model:


EPWM TRIP ZONE EXAMPLE
EPWM block - key parameters
Time base:
Module: EPWM1
Timer period: 12000
TBCLK: Divide by 4
HSCLK: Divide by 4
Counter mode: Up-Down count
Sync in source: All
Counter compare:
CMPA value: 6000
CMPB value: 0
CMPC value: 0
CMPD value: 0
Action qualifier:
Cntr equals to CMPAU: Set output pins to high
Cntr equals to CMPAD: Set output pins to low
Trip zone:
Enable cyclic trip-zone: True
CBC Latch clear signal: Clear when CBC pulse counter reaches zero
Target hardware Resource configuration
Input XBar0: GPIO11
Pinmux: EPWM9_A, EPWM1_A
EPWM AM263X
EPWM AM263X
EPWM block - key parameters
Time base:
Module: EPWM9
Timer period: 12000
TBCLK: Divide by 4
HSCLK: Divide by 4
Counter mode: Up-Down count
Sync in source: All
Counter compare:
CMPA value: 6000
CMPB value: 0
CMPC value: 0
CMPD value: 0
Action qualifier:
Cntr equals to CMPAU: Set output pins to high
Cntr equals to CMPAD: Set output pins to low
Trip zone:
Enable one-shot trip-zone: True
0
1
u GPIO_OUT AM263X
u GPIO_OUT AM263X
GPIO Output block - key parameters
GPIO pin : 12

Output:



EPWM HR DEADBAND SFO

Description:

This example modifies MEP control registers to show edge displacement for high-resolution deadband with ePWM in up-count mode due to HRPWM control extension of respective module

Example path:

examples\block_examples\epwm\hrpwm_deadband_sfo

Model:

Target Hardware Parameter Configurations

Pinmux: Enable EPWM0_A, EPWM0_B

HRPWM Deadband SFO Example

EPWM block - key parameters

Time Base

Module: EPWM0
Timer Period: 99
Counter Mode: Up count

Action Qualifier

A when CTR==Zero: Set high
A when CTR==CMPAU: Set low
B when CTR==Zero: Set high
B when CTR==CMPU: Set low

Deadband

Rising edge delay polarity: Not Inverted
Falling edge delay polarity: Not Inverted
Rising edge delay value: 8
Falling edge delay value: 8
Dead band counter clock rate: 2*TBCLK

HRPWM

Enable HRPWM: True
Enable Automatic HRMSTEP scaling: True
nable SFO Library: True
MEP Scale Factor: 33
Control mode on EPWMxA: CMPAHR/CMPBHR or TBPRDHR control MEP edge
Control mode on EPWMxB: CMPAHR/CMPBHR or TBPRDHR control MEP edge
Edge control mode on EPWMxA: MEP controls falling edge
CMPAHR: 12800
Edge control mode on EPWMxB: MEP controls falling edge
CMPBHR: 12800
Deadband edge mode: MEP controls rising and falling edge
Rising edge delay: 15
Falling edge delay: 15

EPWM
AM263X

EPWM HR DUTY CYCLE SFO

Description:

This example modifies MEP control registers to show edge displacement for high-resolution duty cycle with ePWM in up-count mode due to HRPWM control extension of respective module

Example path:

examples\block_examples\epwm\hrpwm_duty_cycle_sfo

Model:

Target Hardware Parameter Configurations

Pinmux: Enable EPWM0_A, EPWM0_B

HRPWM Duty Cycle SFO Example

EPWM block - key parameters

Time Base

Module: EPWM0
Timer Period: 99
Counter Mode: Up count

Action Qualifier

A when CTR==Zero: Set high
A when CTR==CMPAU: Set low
B when CTR==Zero: Set high
B when CTR==CMPU: Set low

HRPWM

Enable HRPWM: True
Enable Automatic HRMSTEP scaling: True
nable SFO Library: True
MEP Scale Factor: 33
Control mode on EPWMxA: CMPAHR/CMPBHR or TBPRDHR control MEP edge
Control mode on EPWMxB: CMPAHR/CMPBHR or TBPRDHR control MEP edge
Edge control mode on EPWMxA: MEP controls falling edge
CMPAHR: 1062
Edge control mode on EPWMxB: MEP controls falling edge
CMPBHR: 1062

EPWM HR PHASE SHIFT SFO

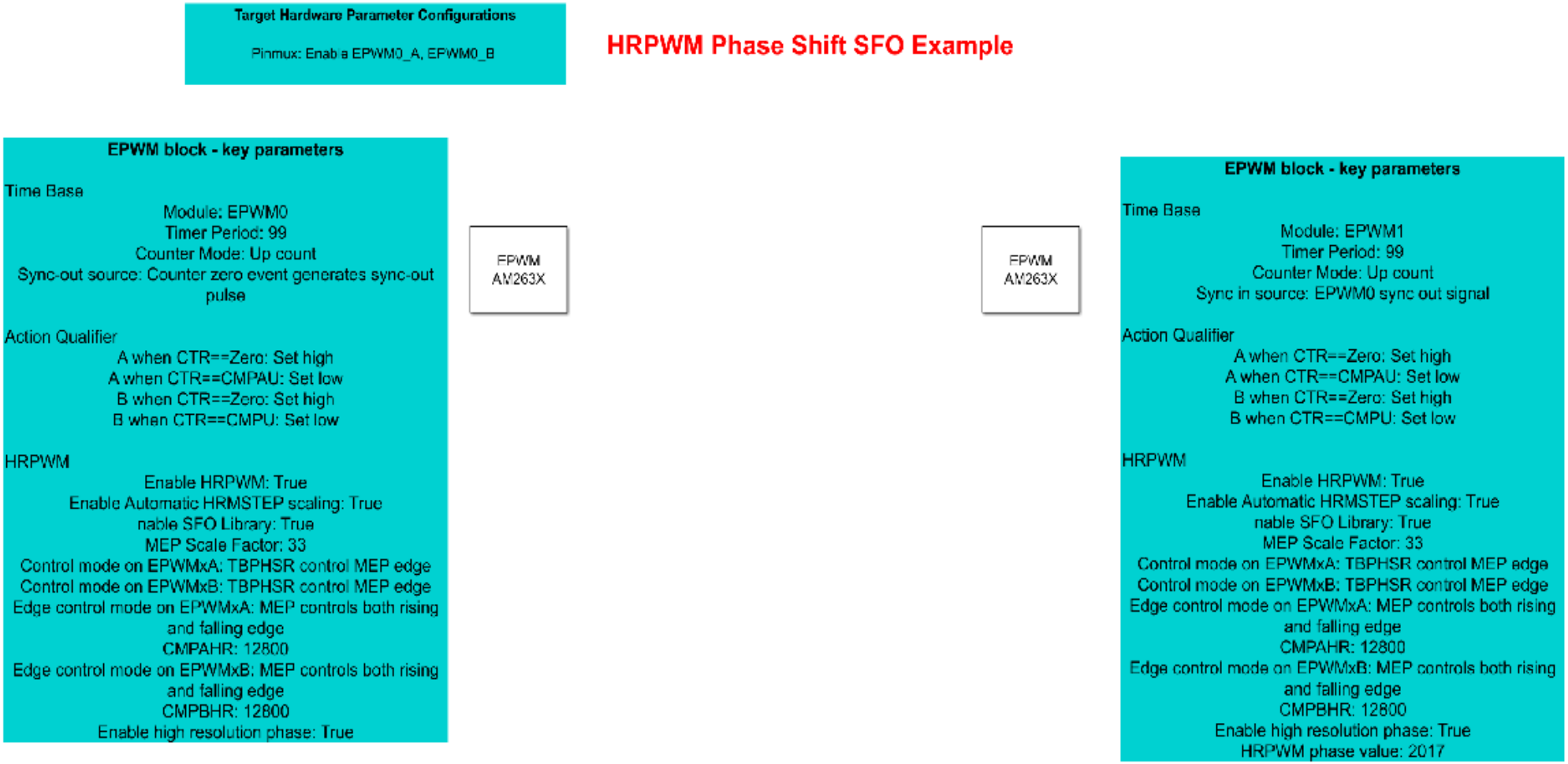
Description:

This example modifies MEP control registers to show edge displacement for high-resolution phase shift with ePWM in up-count mode due to HRPWM control extension of respective module

Example path:

examples\block_examples\epwm\hrpwm_phase_shift_sfo

Model:



GPIO INPUT INTERRUPT

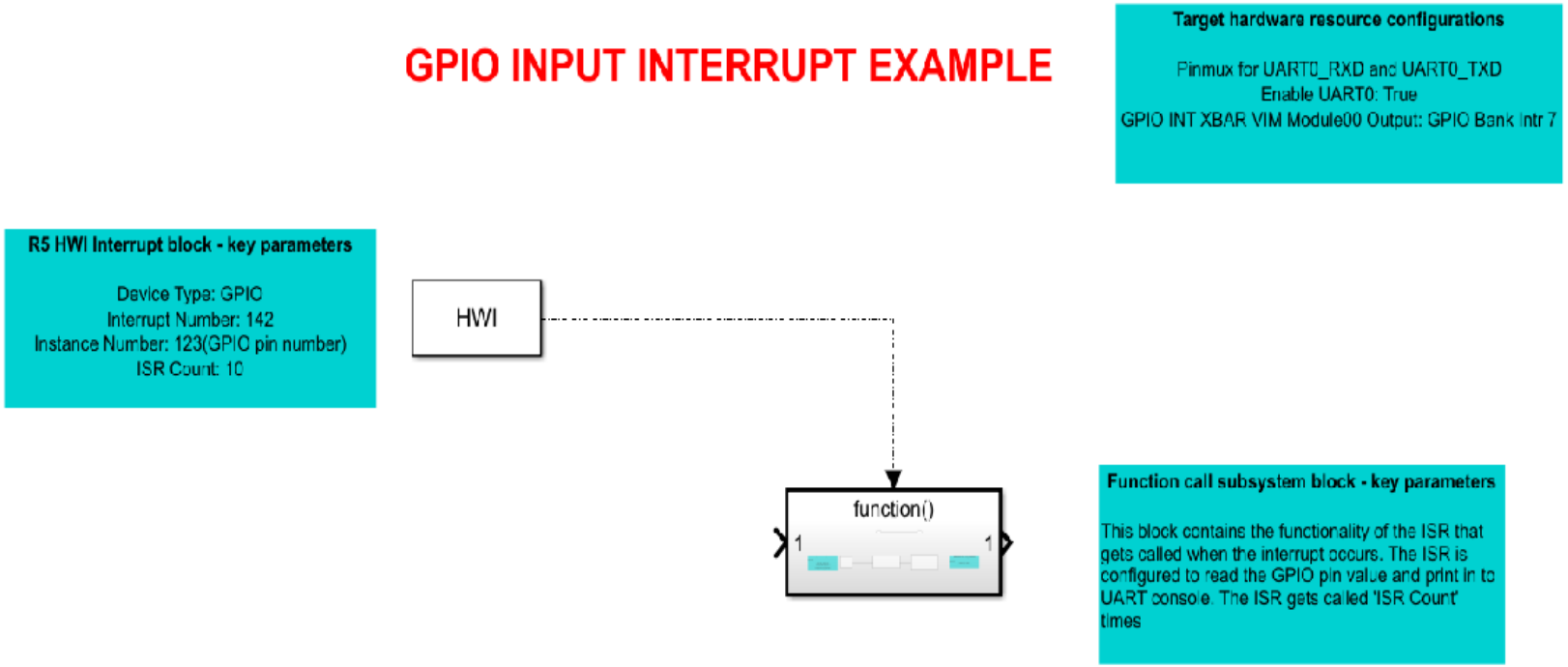
Description:

This example configures a GPIO pin in input mode and configures it to generate interrupt on rising edge. The application reads the input pin state and displays it in the UART console everytime the interrupt gets triggered(SW4 is pressed)

Example path:

examples\block_examples\gpio\gpio_input_interrupt

Model:



Output:

```
Starting CAN Flashwriter...
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
```

GPIO LED BLINK

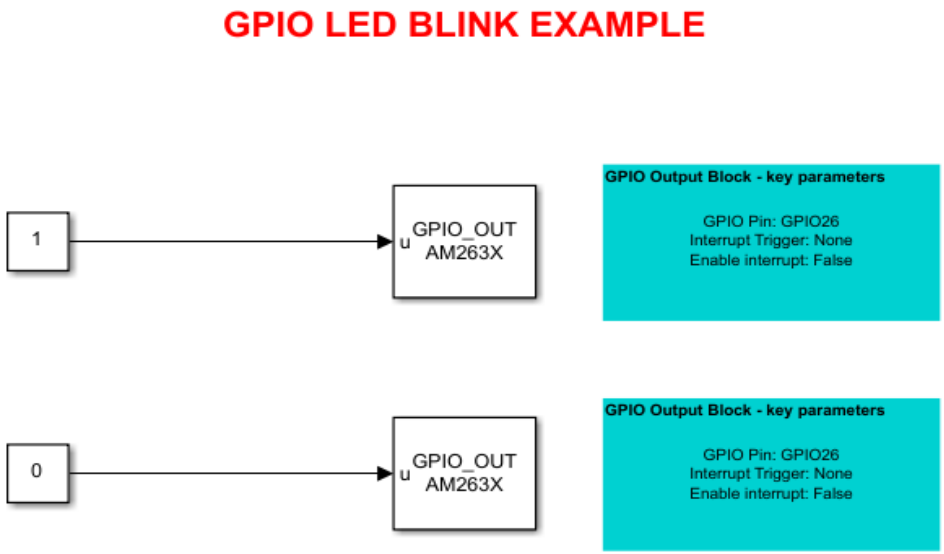
Description:

This example configures a GPIO pin connected to an LED on the EVM in output mode.The example toggles the GPIO LED on/off

Example path:

examples\block_examples\gpio\gpio_led_blink

Model:



UART echo

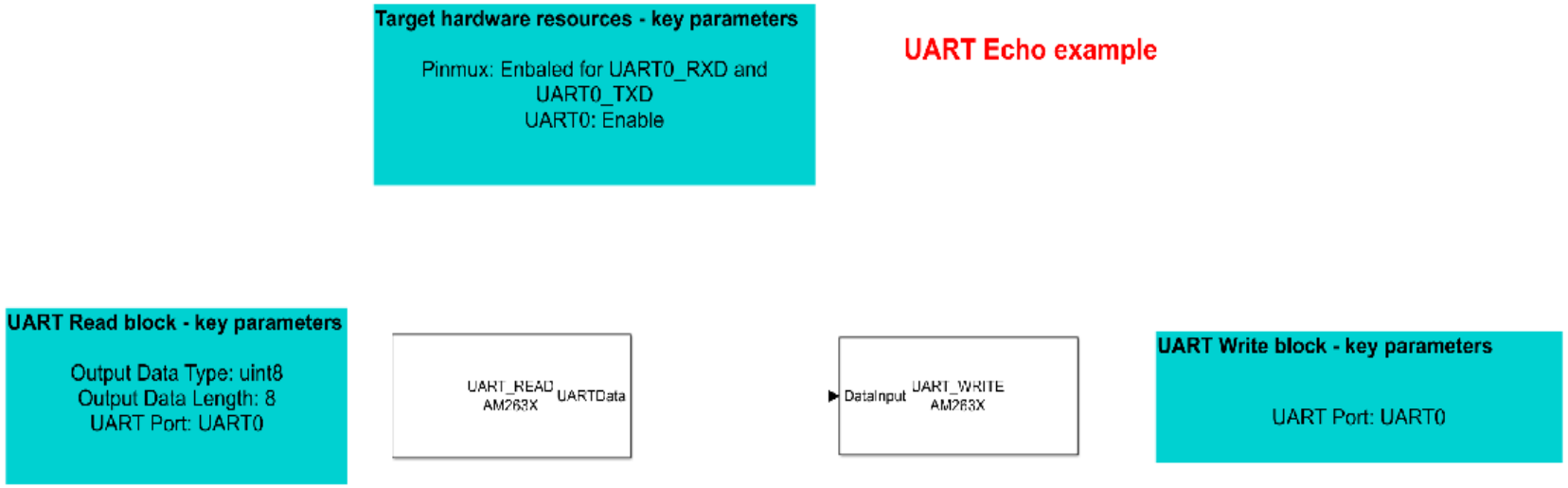
Description:

This example features the working of the UART READ and UART WRITE operation. Here the UART Read block is configured to read 8 characters and echos back the same into the UART port using the UART WRITE block.

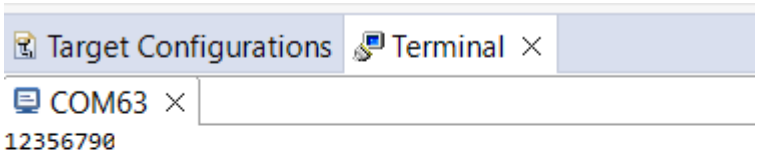
Example path:

examples\block_examples\uart\uart_echo

Model:


Target hardware resources - key parameters
Pinmux: Enbaled for UART0_RXD and
UART0_TXD
UART0: Enable
UART Echo example
UART Read block - key parameters
Output Data Type: uint8
Output Data Length: 8
UART Port: UART0
UART_READ
AM263X
UARTData
DataInput
UART_WRITE
AM263X
UART Write block - key parameters
UART Port: UART0

Output:


Target Configurations
Terminal
COM63
12356790