

AM243x LAUNCH PAD

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REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.1	10 FEB 2023	Drafted from PROC109E3B - Changed R237 and R238 to 4.7K from 2.2k ohm - Added SPDT selection circuitry U50, U51 and U52 for BP SERVO board	Mistral Design Team		
0.2	23 FEB 2023	- Changed U50, U51 and U52 to VQFN package	Mistral Design Team		
0.3	27 FEB 2023	- Updated MCAN/eQEP_MUX_SEL circuit as pwe TI comments	Mistral Design Team		
0.4	02 MAR 2023	- Updated U50, U51 and U52 to TMUX1574 from TS3A44159RSVR	Mistral Design Team		
0.5	13 SEP 2023	- Updated U18 Part No from AM2434BSFGHIALX to AM2434BSFFHIALX	Mistral Design Team		

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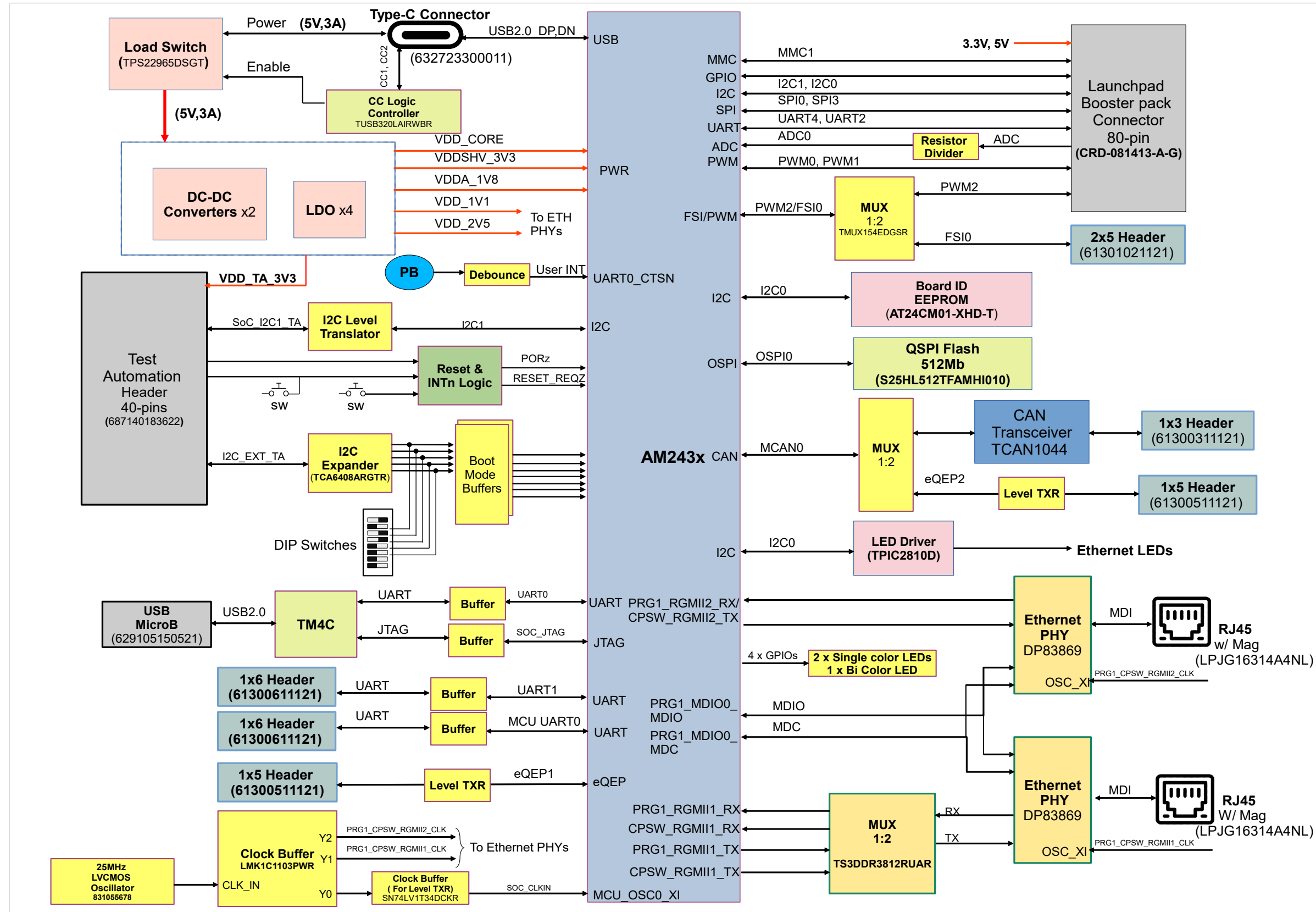
Title REVISION HISTORY

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BLOCK DIAGRAM



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Title BLOCK DIAGRAM

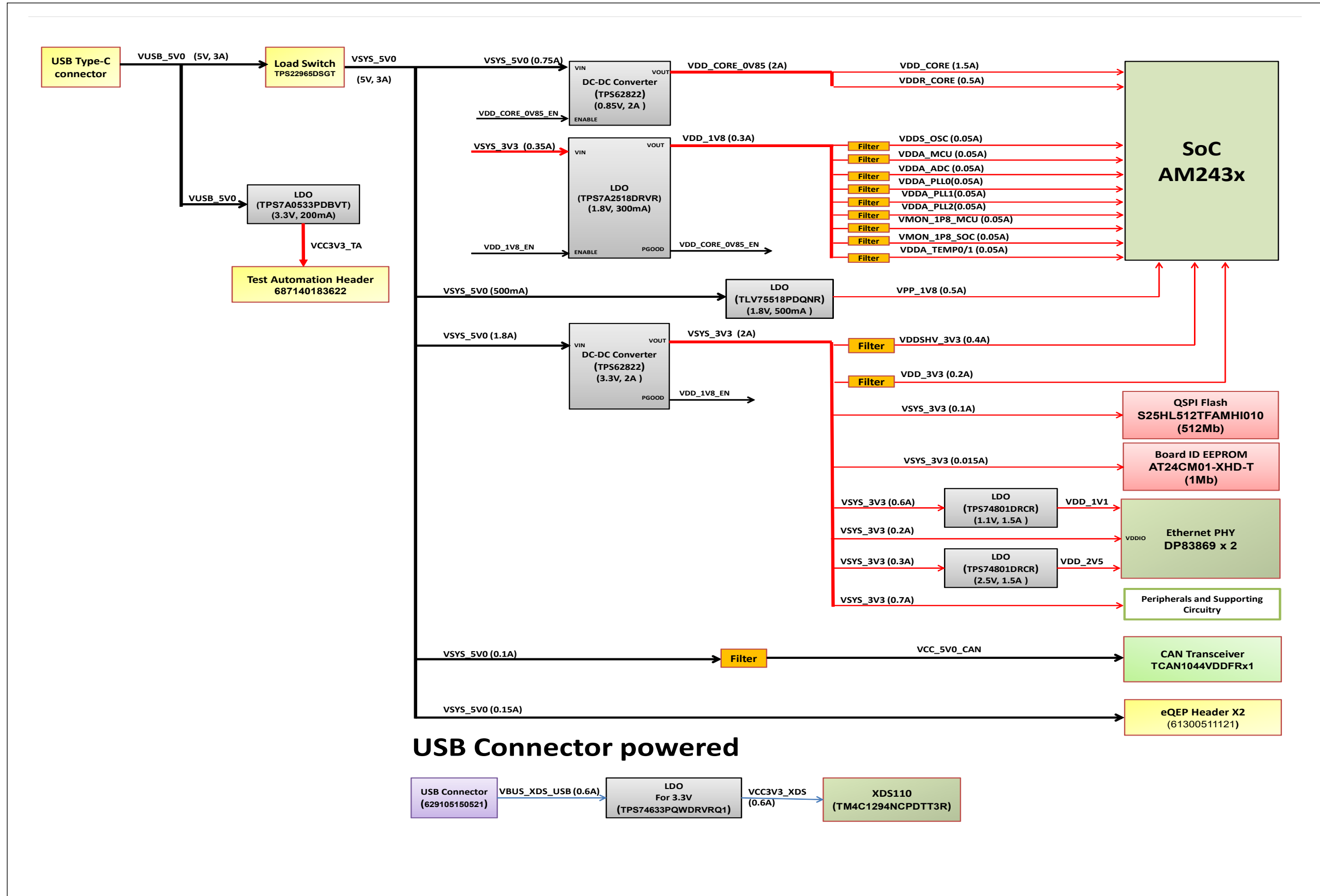
Size PROC109 LP AM243

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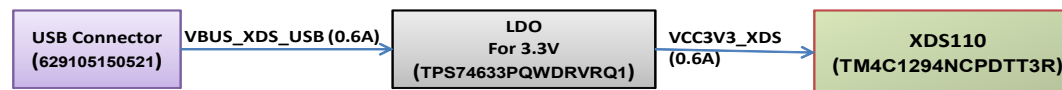
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POWER TREE



USB Connector powered



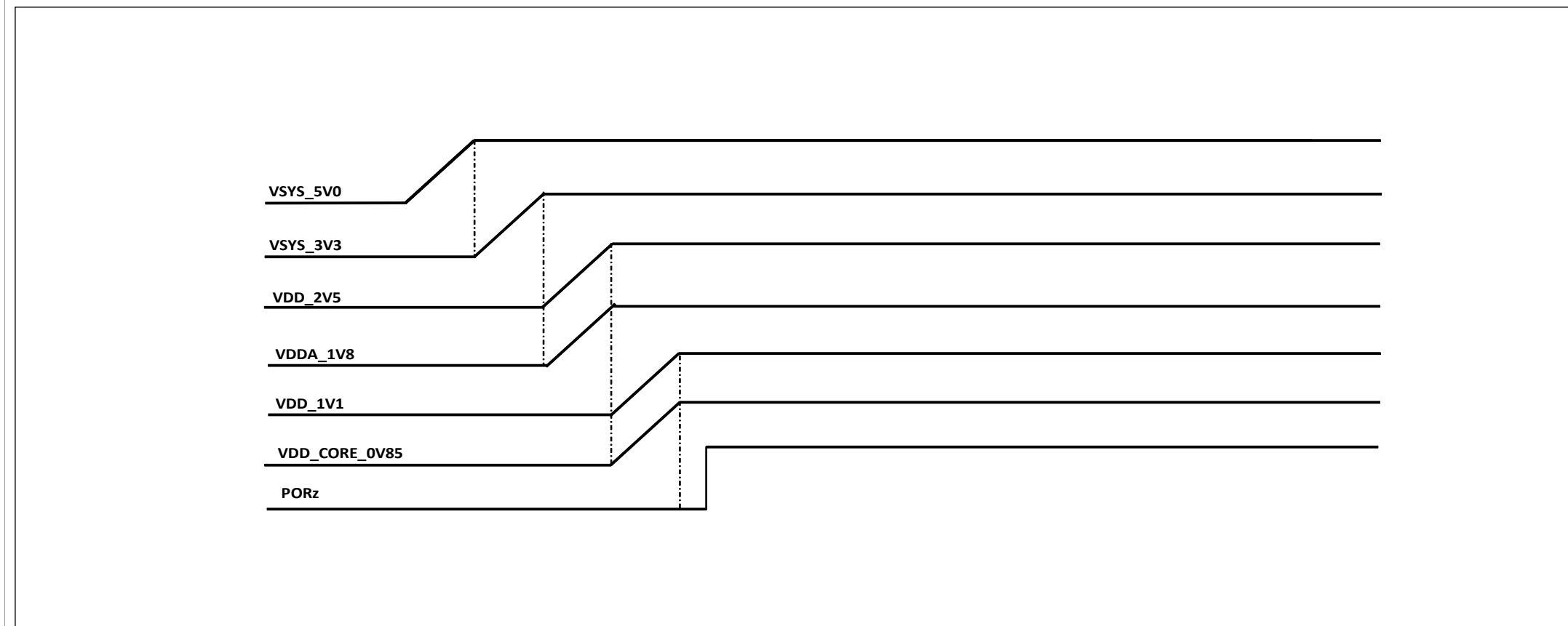
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Title POWER TREE

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POWER ON SEQUENCE



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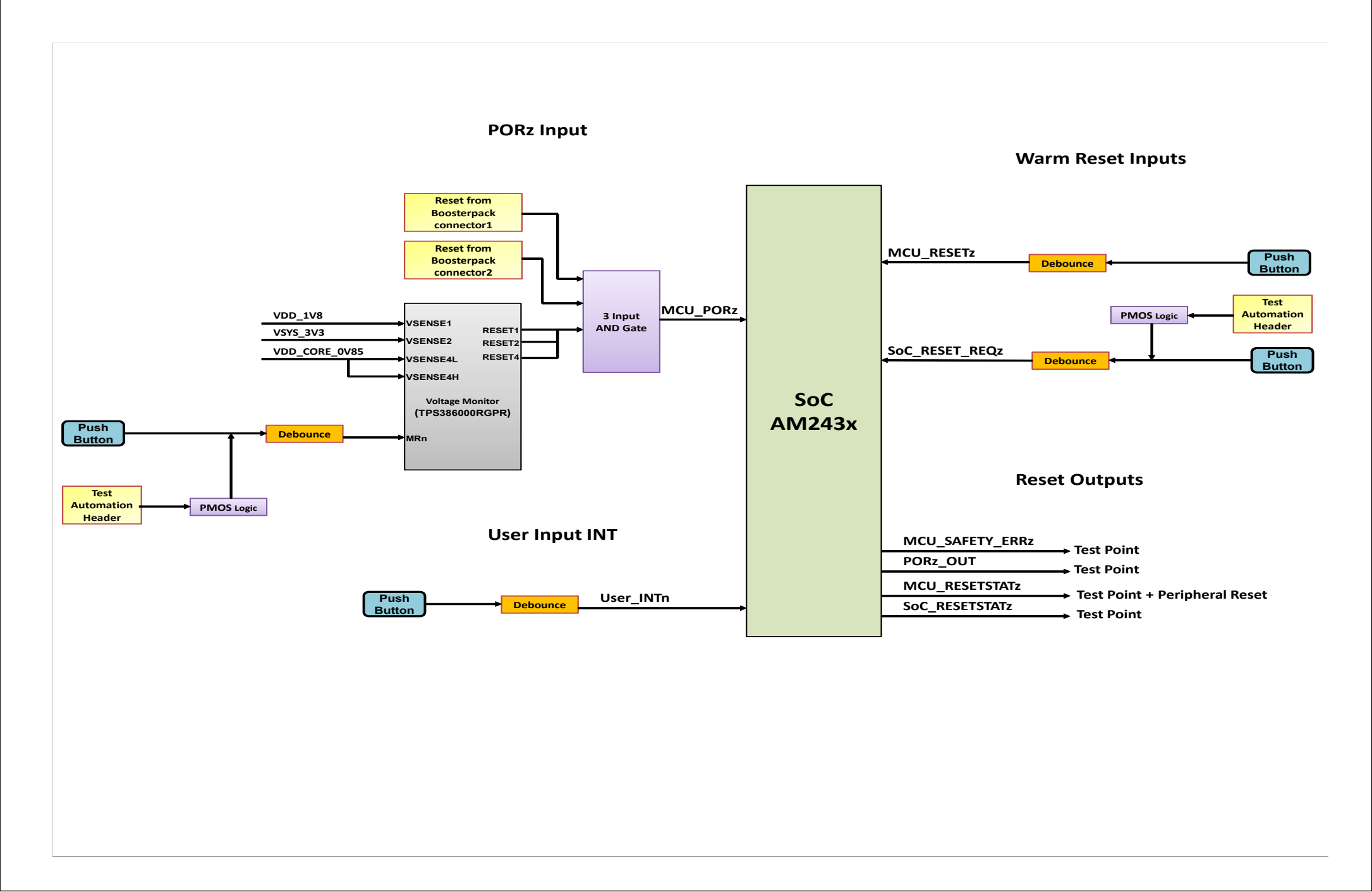
Title POWER ON SEQUENCE

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RESET ARCHITECTURE



GPIO MAPPING TABLE

AM243x LP - GPIO Mapping Table						
Net name	AM243x LP Mapping		Input/Output	Default	State	Remarks
	Package Signal Name	GPIO Number				
TEST_LED1_GREEN	GPMCO_AD7	GPIO0_22	Output	PD	Active High	To Turn ON the test LED (Green)
TEST_LED2_RED	UART0_RTSN	GPIO1_55	Output	PD	Active High	To Turn ON the test LED (Red)
TEST_LED3_RED	PRG1_PRU1_GPO18	GPIO1_39	Output	PD	Active High	To Turn ON the test LED (Red) in Bicolor LED
TEST_LED4_GREEN	PRG1_PRU1_GPO19	GPIO1_38	Output	PD	Active High	To Turn ON the test LED (Green) in Bicolor LED
GPIO_RGMII1_PHY_RSTn	GPMCO_AD13	GPIO0_26	Output	PU	Active Low	To Reset the RGMII1 Ethernet PHY
PRG_CPSW_RGMII1_MUX_SEL	GPMCO_AD12	GPIO0_27	Output	PD	NA	To select the RGMII1 path between PRG and CPSW
USER_INTn	UART0_CTSN	GPIO1_54	Input	PU	Active Low	User Interrupt input from Push Button Switch
OSPIO_RESET_N	OSPIO_CSN1	GPIO0_12	Output	PU	Active Low	To reset the QSPI FLASH on OSPIO Instance
MCAN/eQEP_MUX_SEL	PRG0_PRU1_GPO8	GPIO1_28	Output	PD	NA	To select the functionality of MCAN0_RX pin as MACNO_RX or eQEP_I
FSI/BP_MUX_SEL	GPMCO_AD11	GPIO0_28	Output	PD	NA	To select the functionality of GPMCO_AD8 and GPMCO_AD9 pins as FSI_RX or PWM
MCAN0_STB	PRG0_PRU1_GPO5	GPIO1_25	Output	PU	Active Low	To put the CAN Transceiver out of Standby
PRG1_CPSW_ETH2_LED_1000/RX_ER	PRG1_PRU1_GPO5	GPIO0_70	Input	PD	NA	Ethernet PHY2 RX ER indication to SoC
PRG1_CPSW_ETH2_LED_LINK	PRG1_PRU1_GPO8	GPIO0_73	Input	PD	NA	Ethernet PHY2 RX link indication to SoC
GPIO_RGMII2_PHY_RSTn	PRG1_PRU1_GPO18	GPIO0_20	Output	PU	Active Low	To Reset the RGMII2 Ethernet PHY
PRG1_CPSW_RGMII_INTn	PRG1_PRU1_GPO19	GPIO0_84	Input	PU	Active Low	Interrupt signal from Both RGMII1 & RGMII2 Ethernet PHYs
PRG1_CPSW_ETH1_LED_1000/RX_ER	PRG1_PRU0_GPO5	GPIO0_50	Input	PD	NA	Ethernet PHY1 RX ER indication to SoC
PRG1_CPSW_ETH1_LED_LINK	PRG1_PRU0_GPO8	GPIO0_53	Input	PD	NA	Ethernet PHY1 RX link indication to SoC
PRG1_CPSW_ETH1_LED_ACT	PRG1_PRU0_GPO9	GPIO0_54	Input	PD	NA	Ethernet PHY1 MII COL indication to SoC
PRG1_CPSW_ETH2_LED_ACT	PRG1_PRU1_GPO9	GPIO0_74	Input	PD	NA	Ethernet PHY2 MII COL indication to SoC

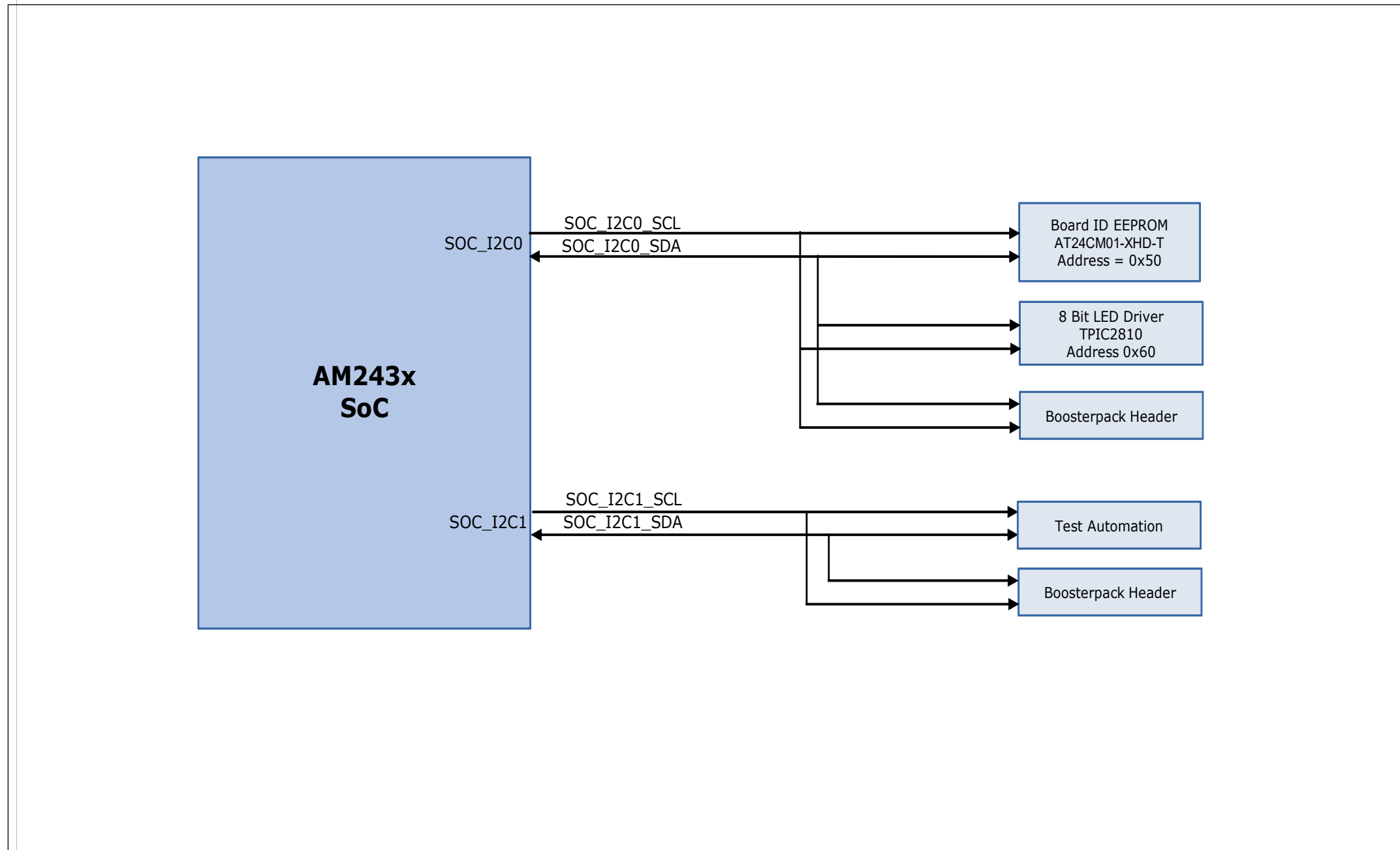
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Title: GPIO MAPPING TABLE

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I2C TREE



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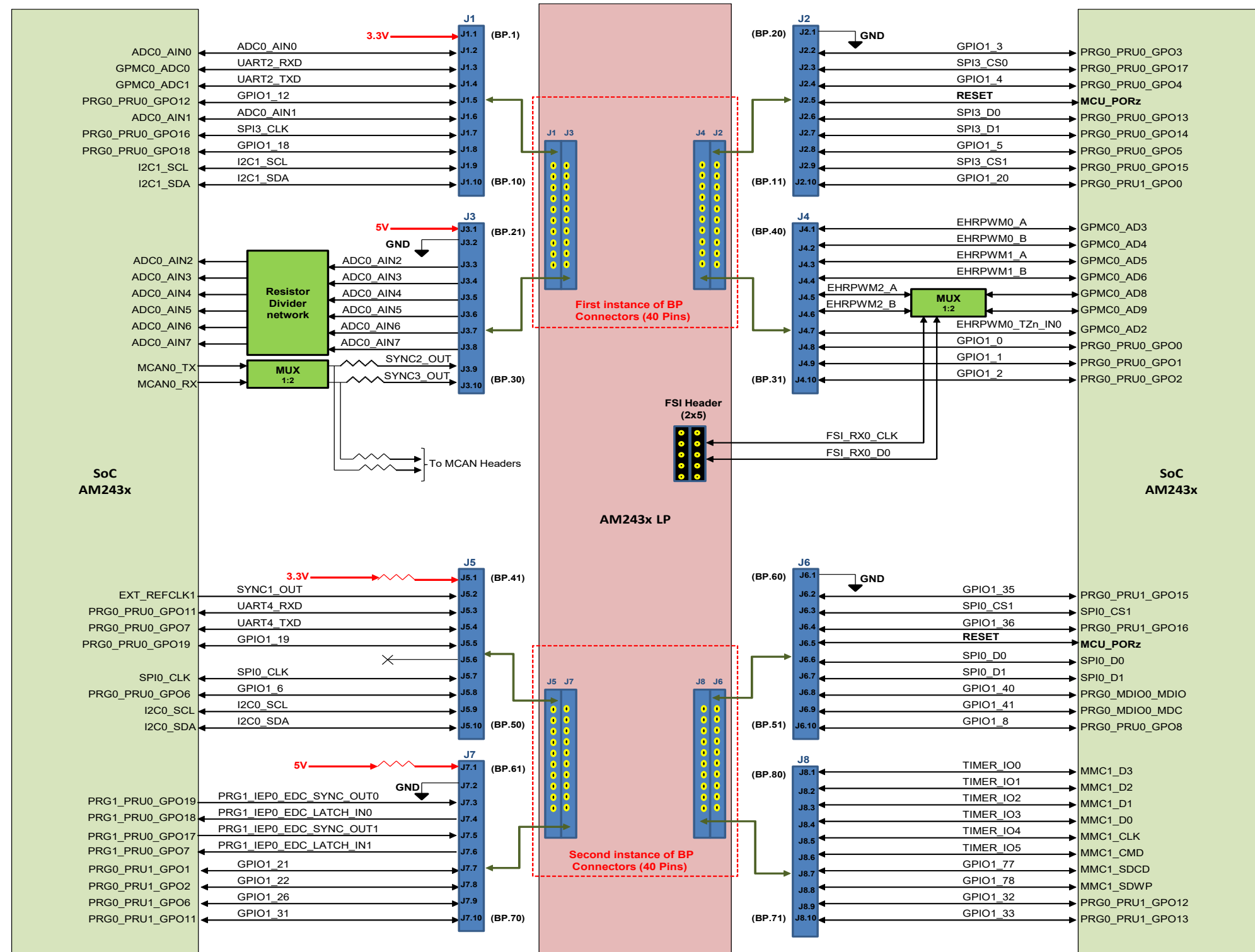
Title I2C TREE

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BOOSTERPACK CONNECTOR PINOUTS



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Title BOOSTERPACK CONNECTOR PINOUTS

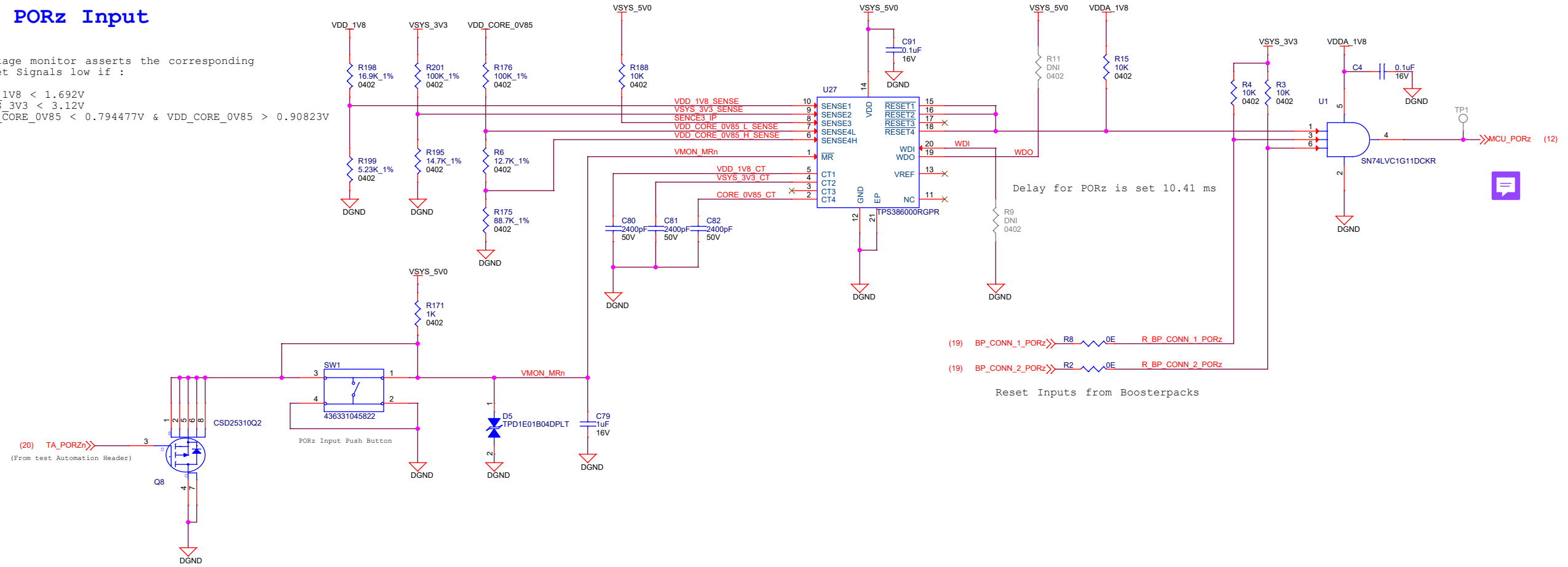
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Reset Inputs

MCU PORz Input

Voltage monitor asserts the corresponding reset Signals low if :

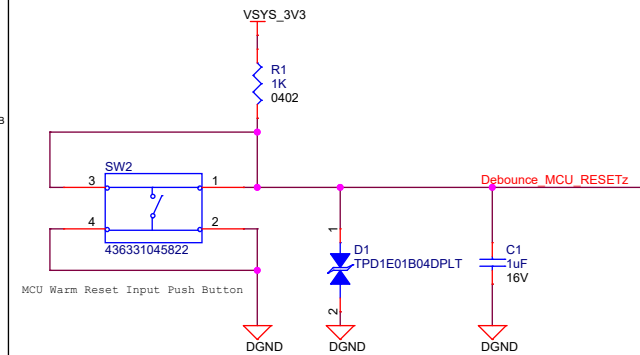
VDD_1V8 < 1.692V
 VSYS_3V3 < 3.12V
 VDD_CORE_0V85 < 0.794477V & VDD_CORE_0V85 > 0.90823V



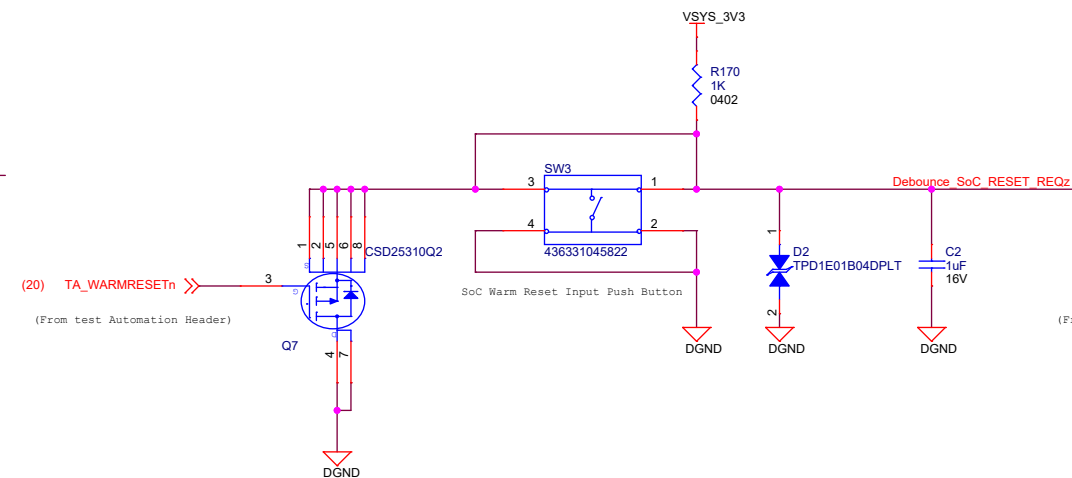
Delay for PORz is set 10.41 ms

(19) BP_CONN_1_PORz >> R8 >> R BP CONN 1 PORz
 (19) BP_CONN_2_PORz >> R2 >> R BP CONN 2 PORz
 Reset Inputs from Boosterpacks

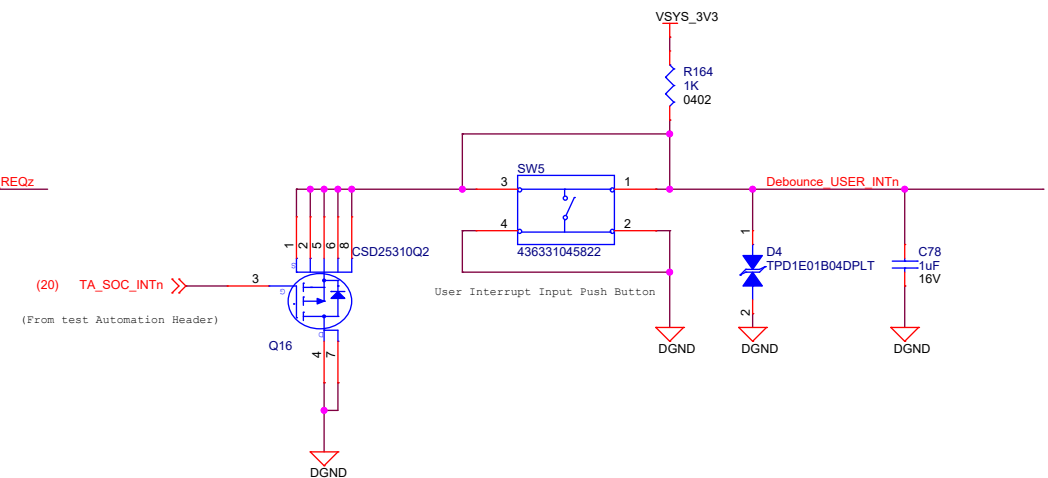
MCU Warm Reset Input



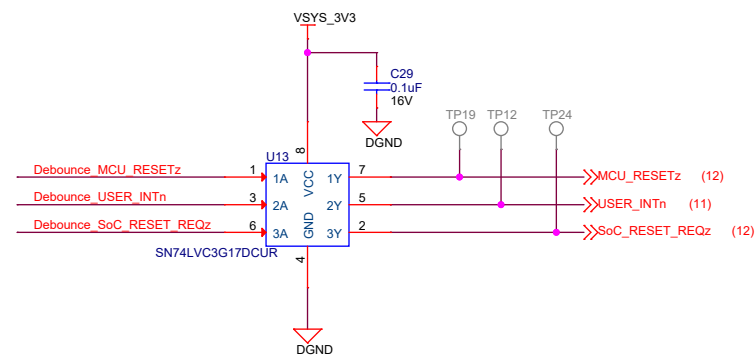
SoC Warm Reset Input



User Push Button



DEBOUNCE CIRCUIT



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Title RESET INPUTs

Size PROC109 LP AM243

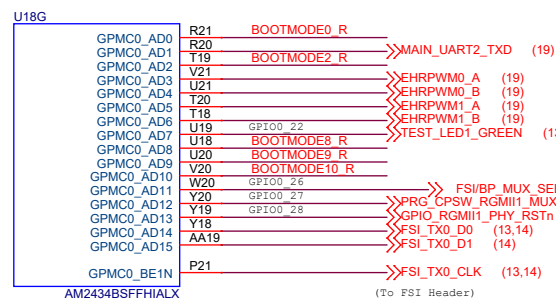
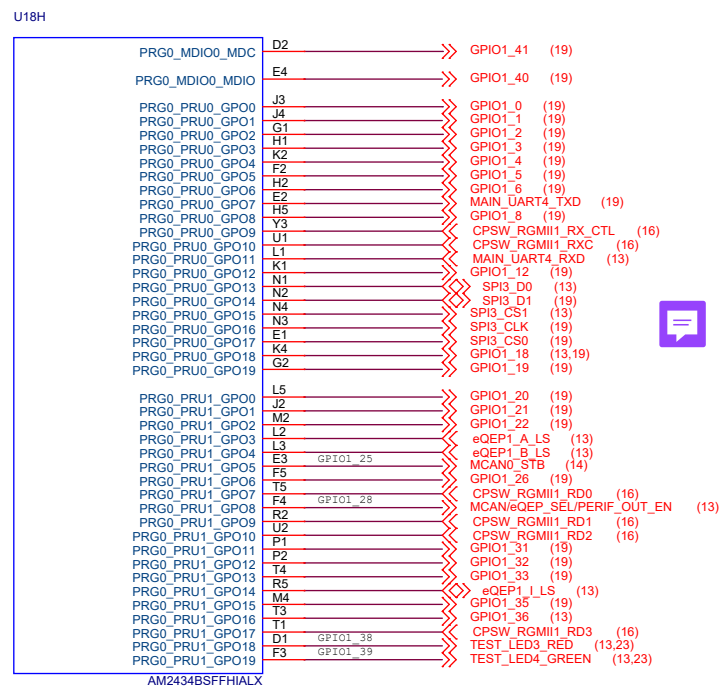
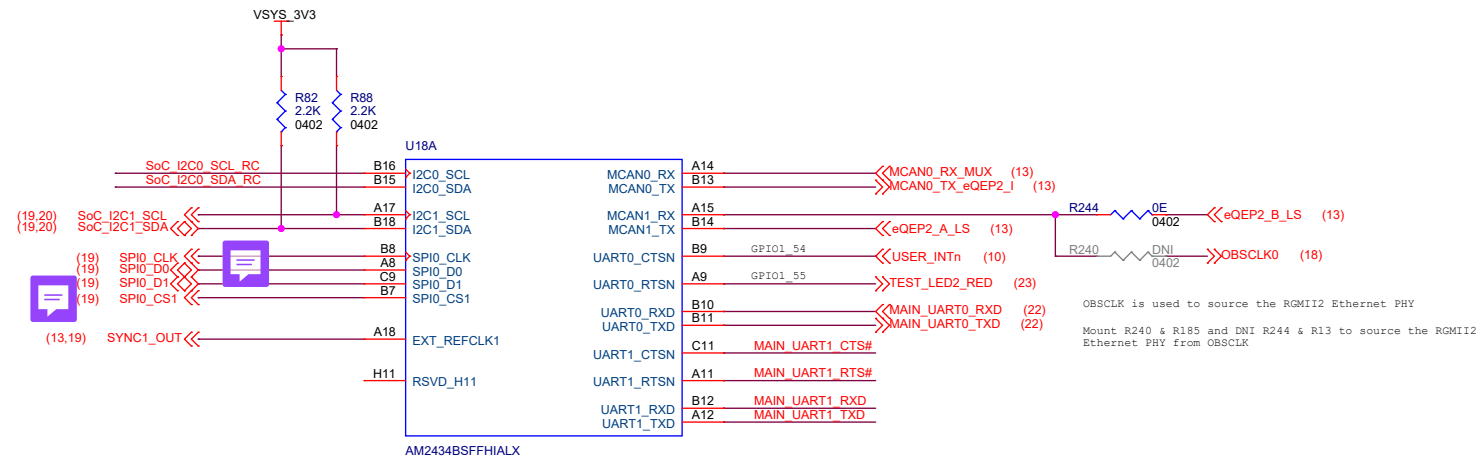
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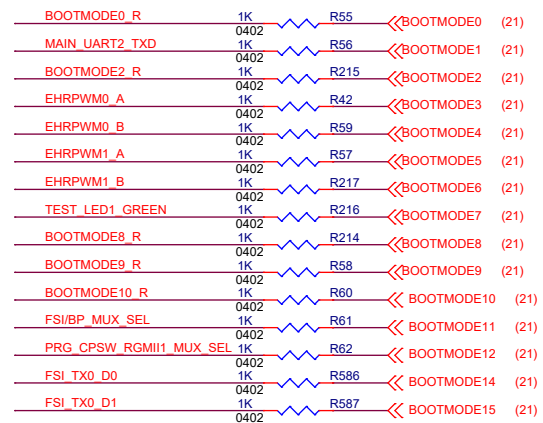
A

SoC Blocks



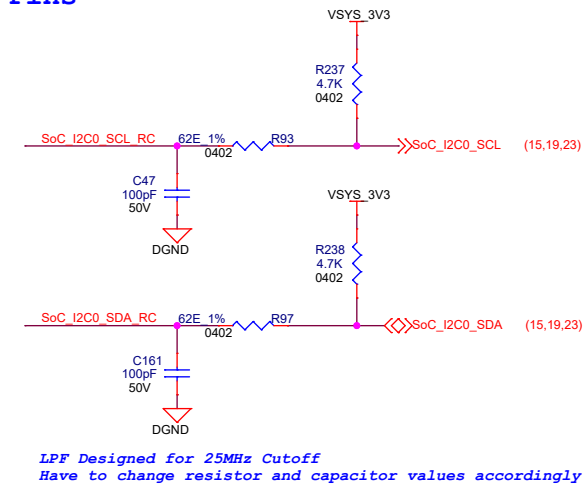
Note : No Input to SoC should be driven from others while Booting

BOOT Mode Pins

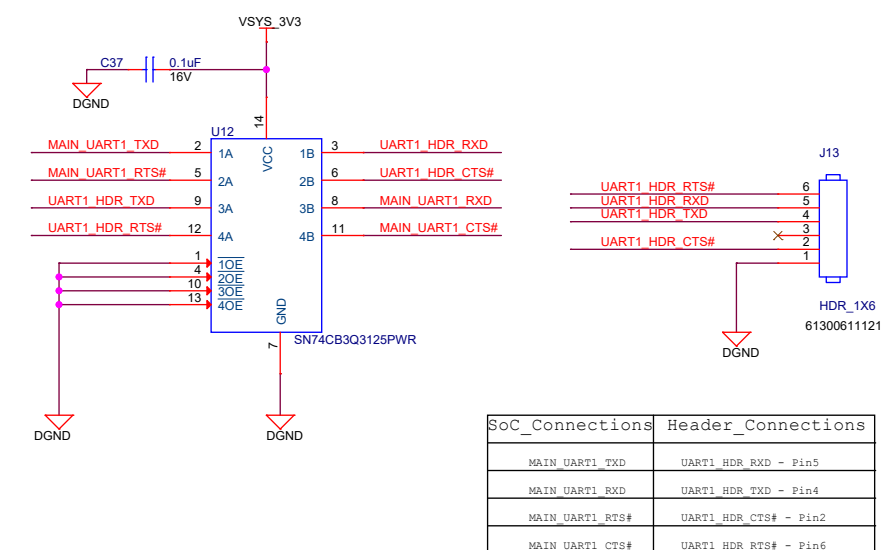


Note: 1K resistors are used to isolate the BOOTMODE control logic after the value is latched

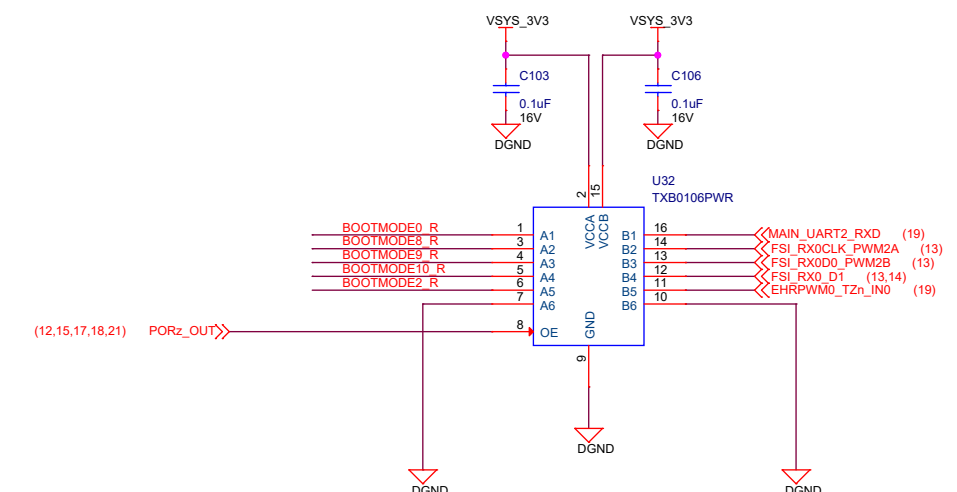
LPF For I2C Pins



UART Buffer & EXT UART HDR for UART1



Isolation Buffer for Bootmode Input pins



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Title SOC1

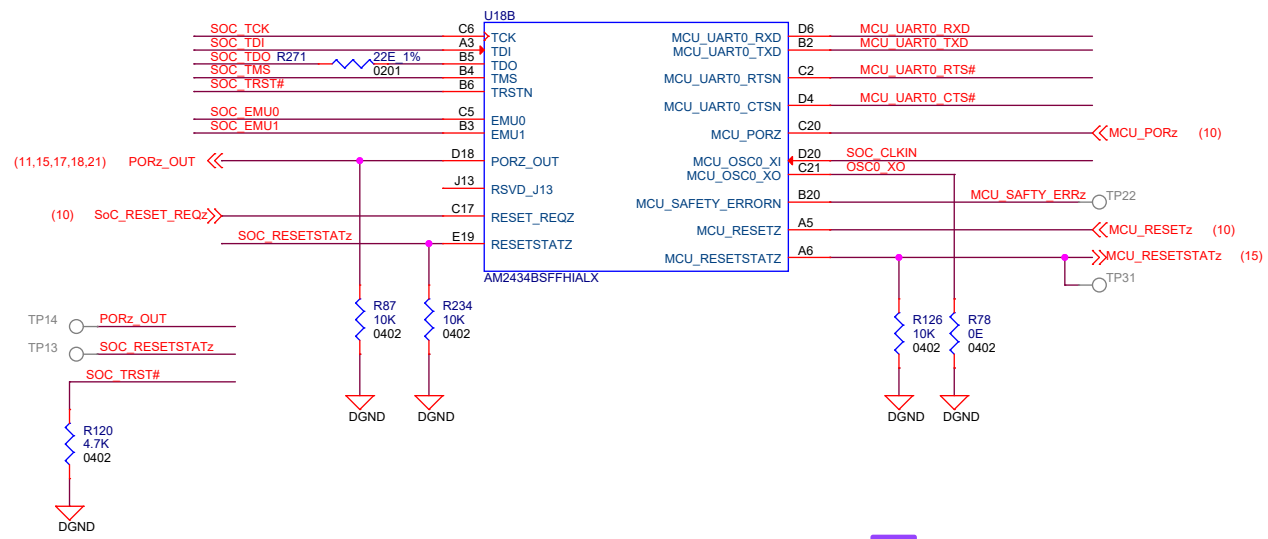
Size PROC109 LP AM243

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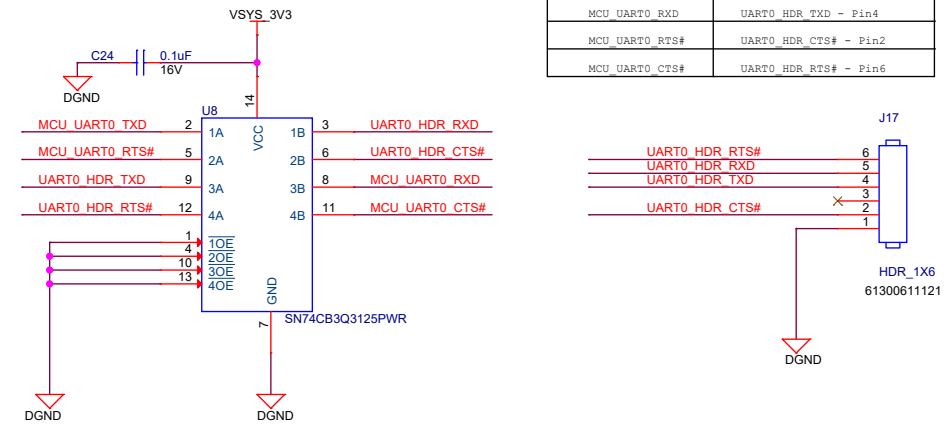
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SoC Blocks

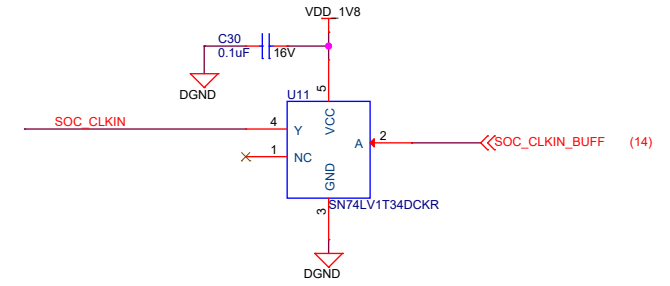


MCU UART0 Buffer & Header

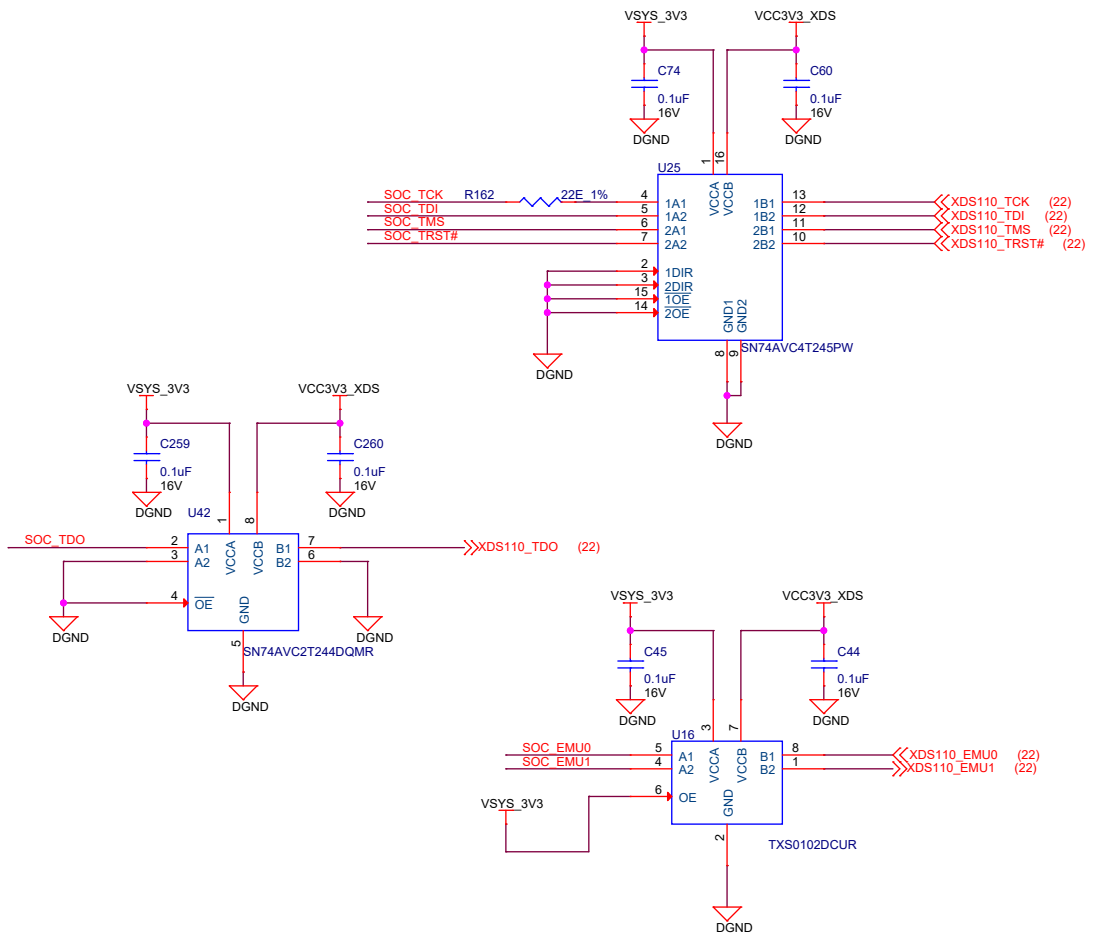


SoC_Connections	Header_Connections
MCU_UART0_TXD	UART0_HDR_RXD - Pin5
MCU_UART0_RXD	UART0_HDR_TXD - Pin4
MCU_UART0_RTS#	UART0_HDR_CTS# - Pin2
MCU_UART0_CTS#	UART0_HDR_RTS# - Pin6

SoC Clock Buffer



XDS110 JTAG Isolation Buffer

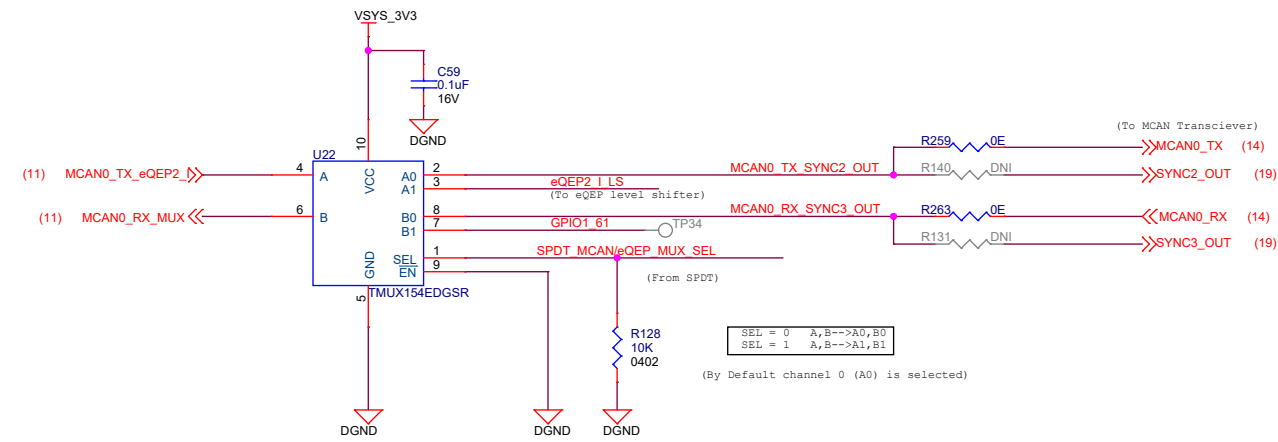


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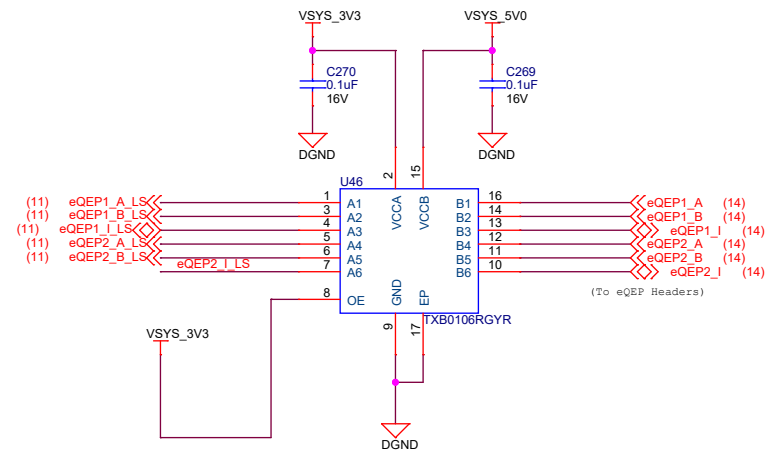


Title: SOC2		
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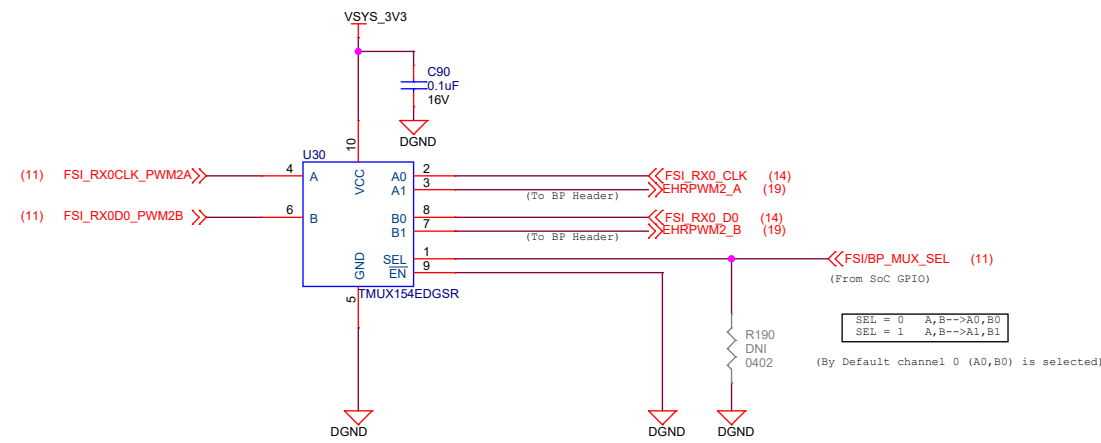
MCAN/eQEP FET Switch



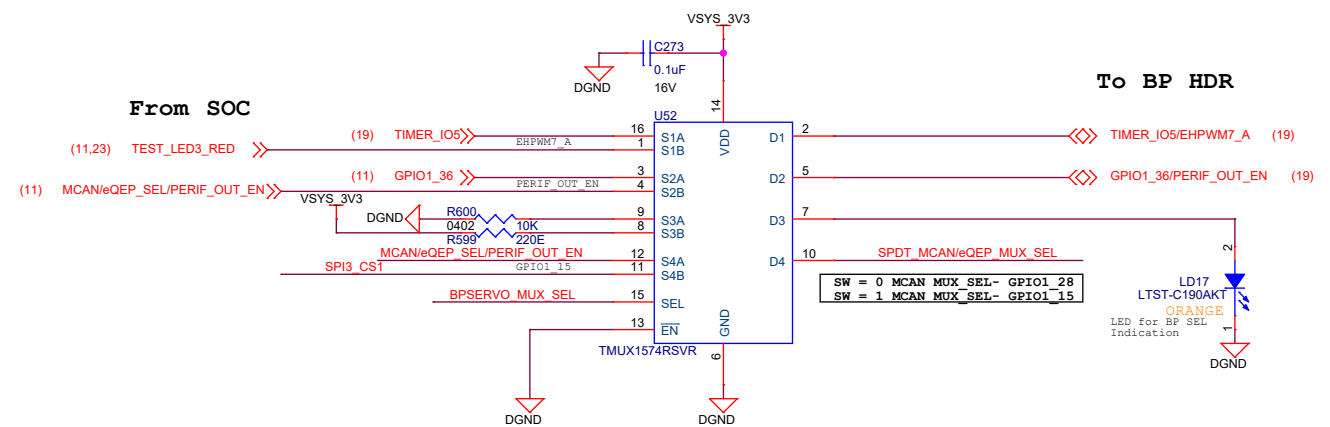
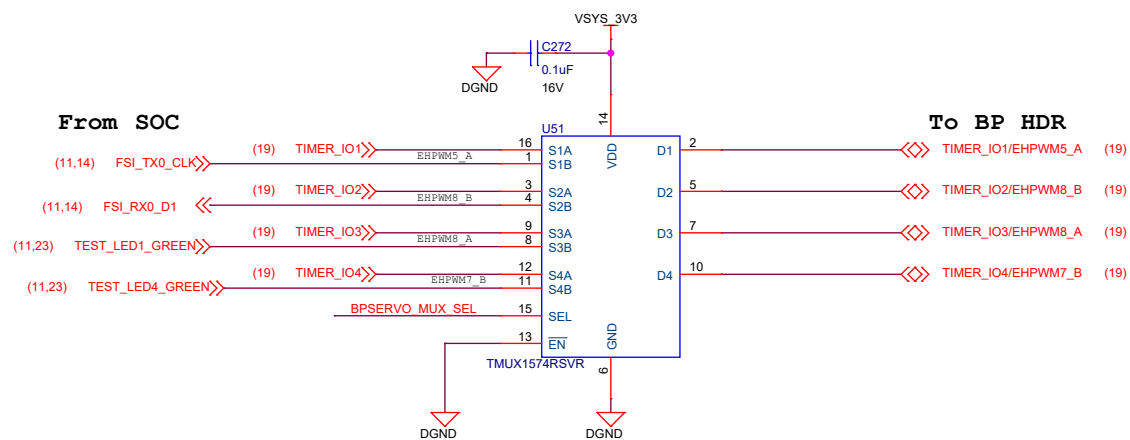
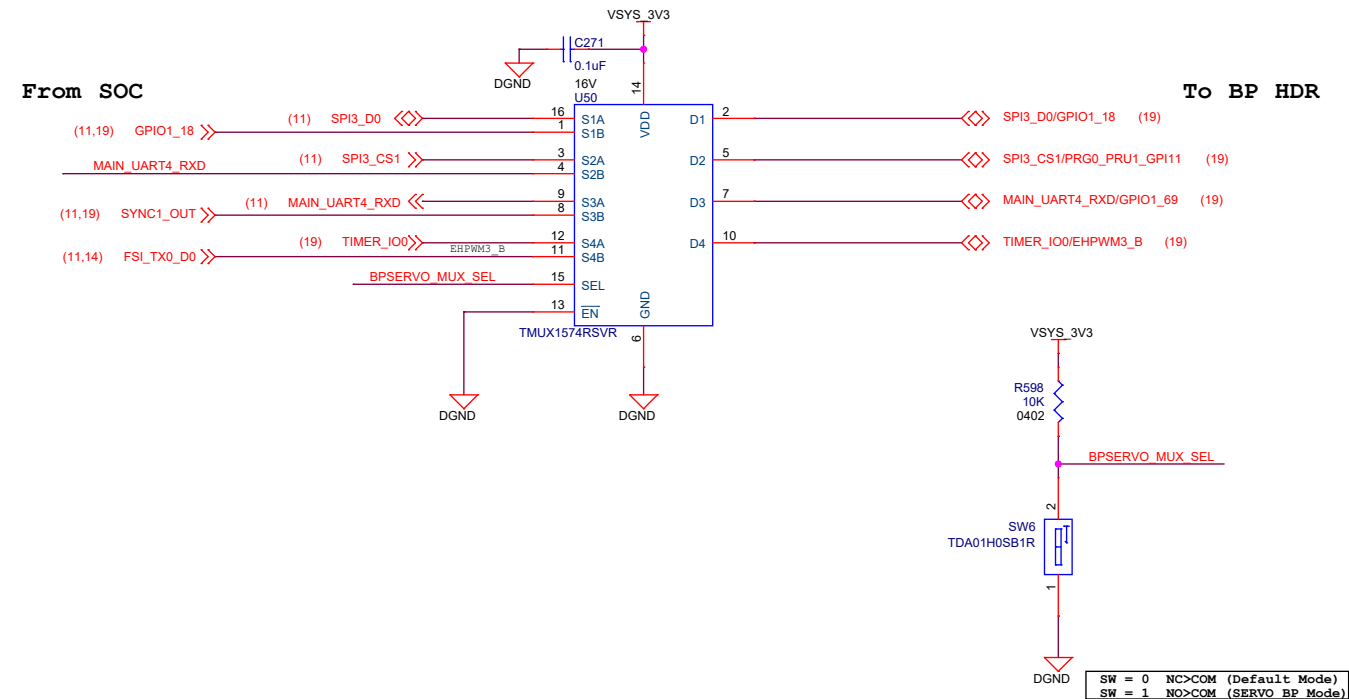
eQEP Level Shifter



FSI/BP FET Switch



SPDT for BP-SERVO SELECTION

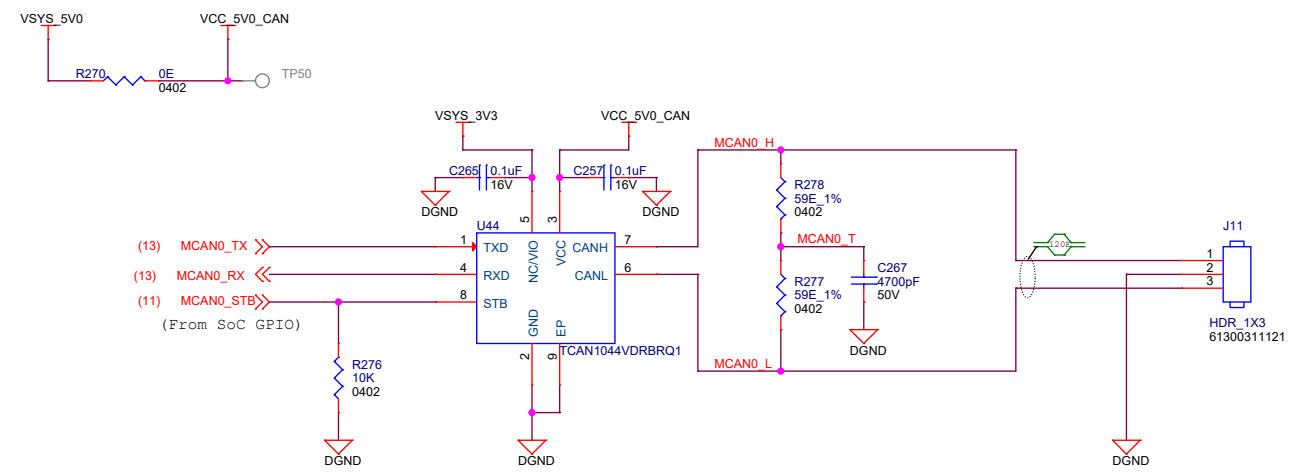


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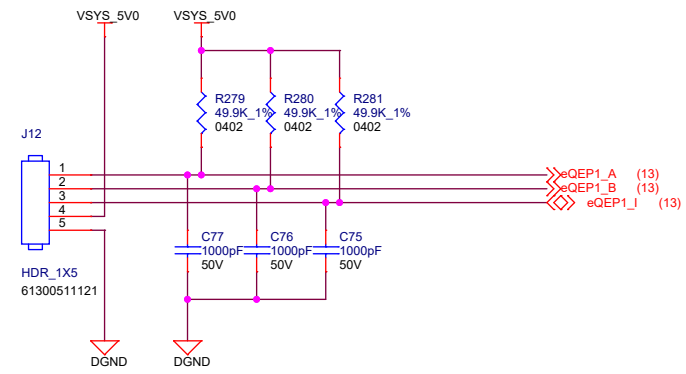


Title		MCAN_eQEP_FSI_MUX	
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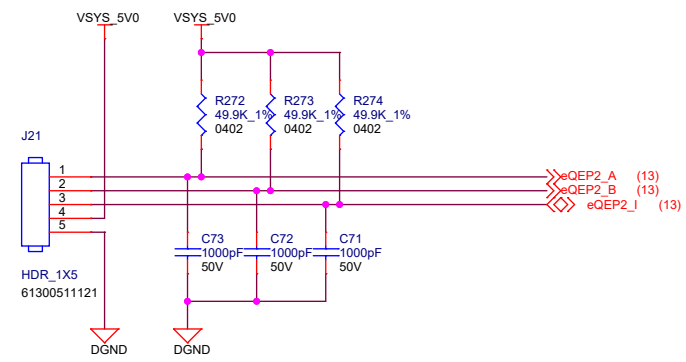
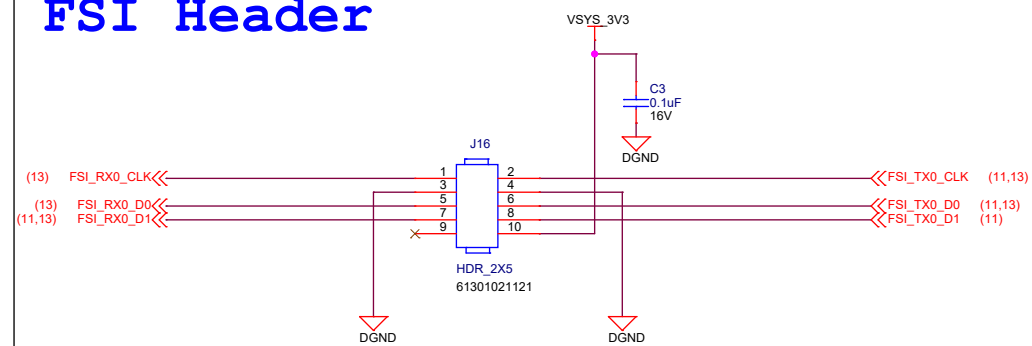
MCAN Transceiver & Header



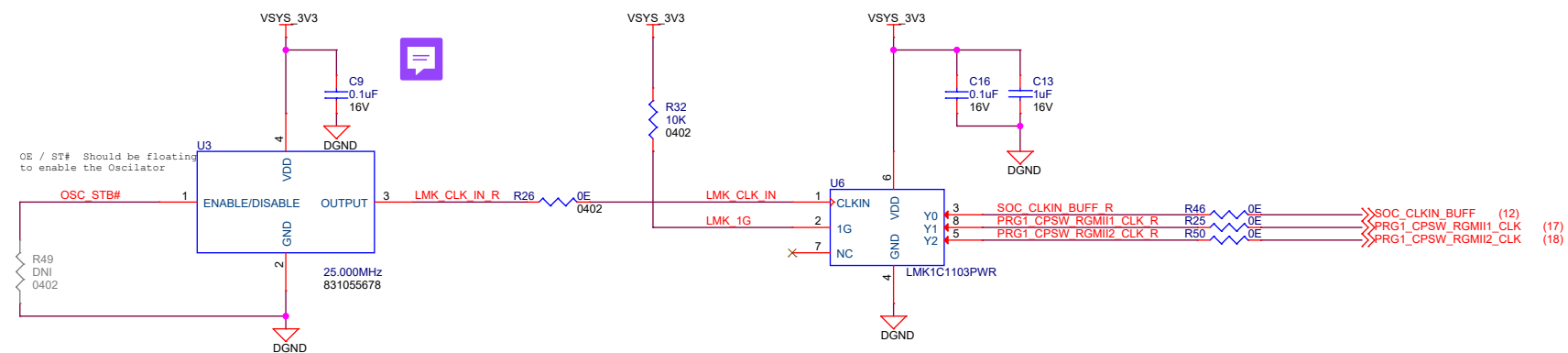
eQEP Headers



FSI Header



SoC and Ethernet PHY Clock Buffer



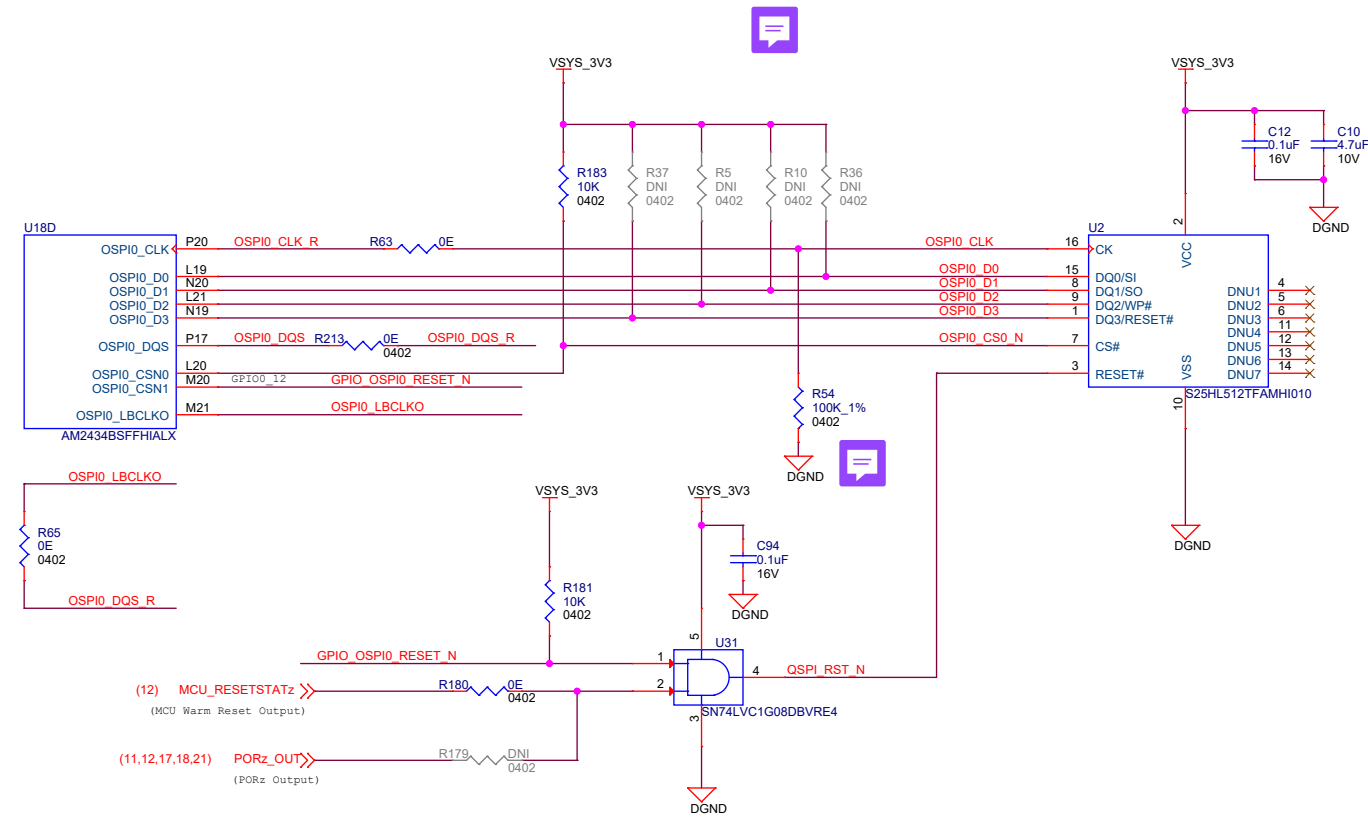
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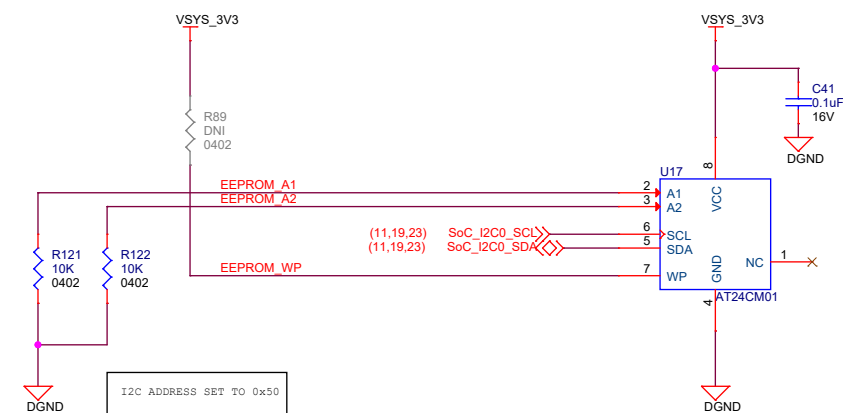
Title: CAN_eQEP_FSI_HEADERS & CLOCK BUFFER

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QSPI FLASH



Board ID EEPROM



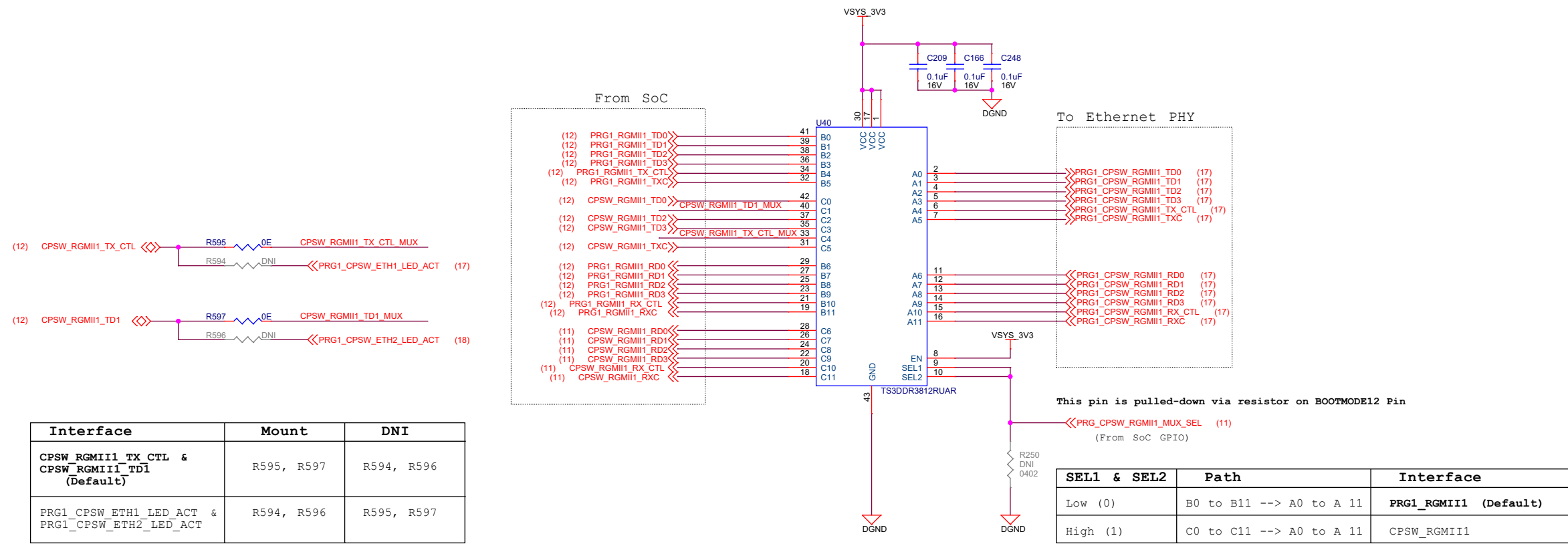
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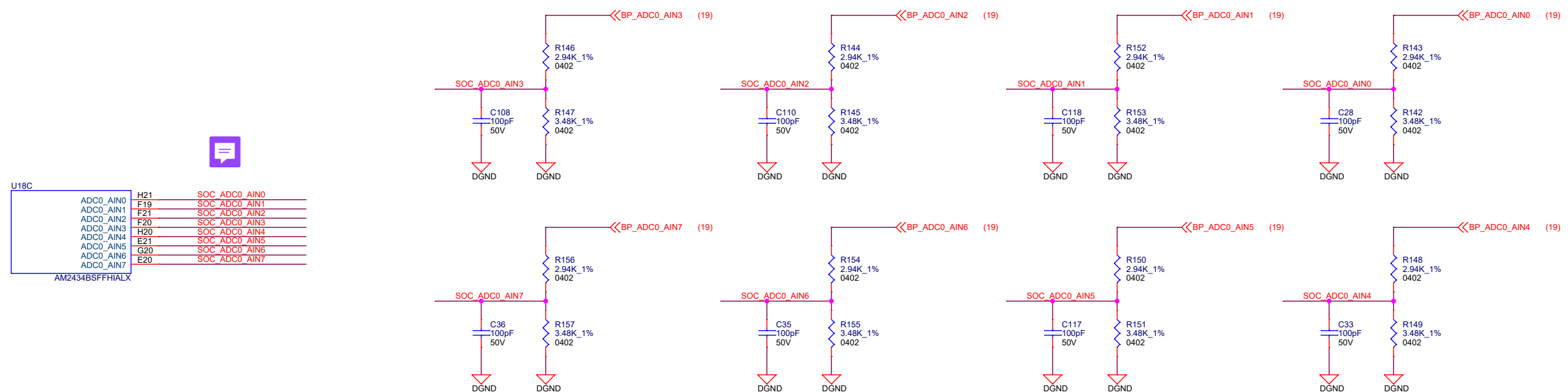
Title: QSPI_BOARD_ID_EEPROM

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CPSW or PRG RGMII1 Ethernet Data MUX



ADC Inputs



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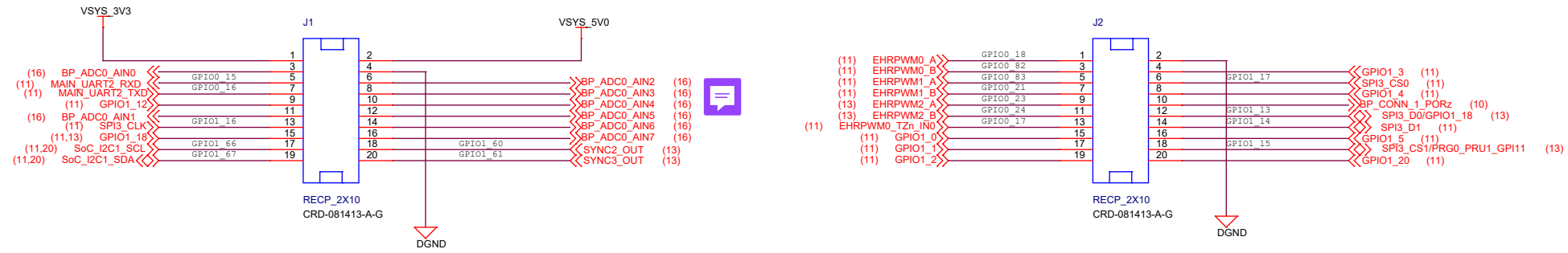


Title ETHERNET DATA MUX & ADC INPUTS

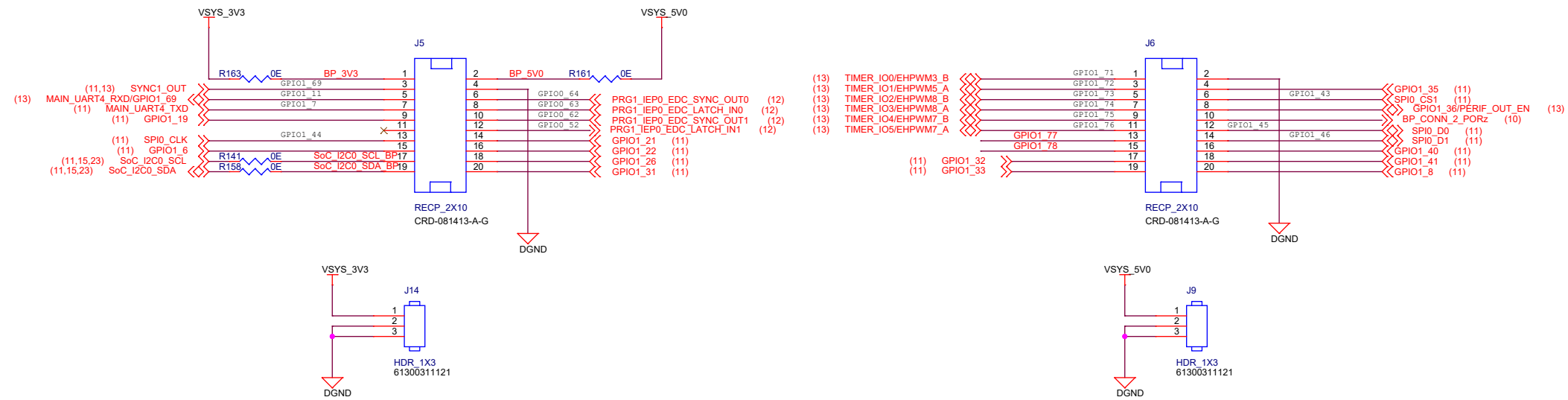
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Booster Pack Header

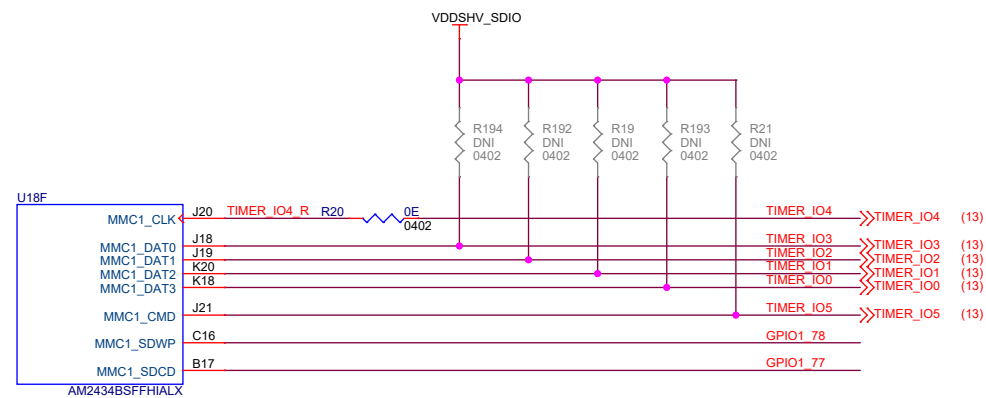
Boosterpack Header Site - 1



Boosterpack Header Site - 2



SoC MMC1 Connection to BP Header



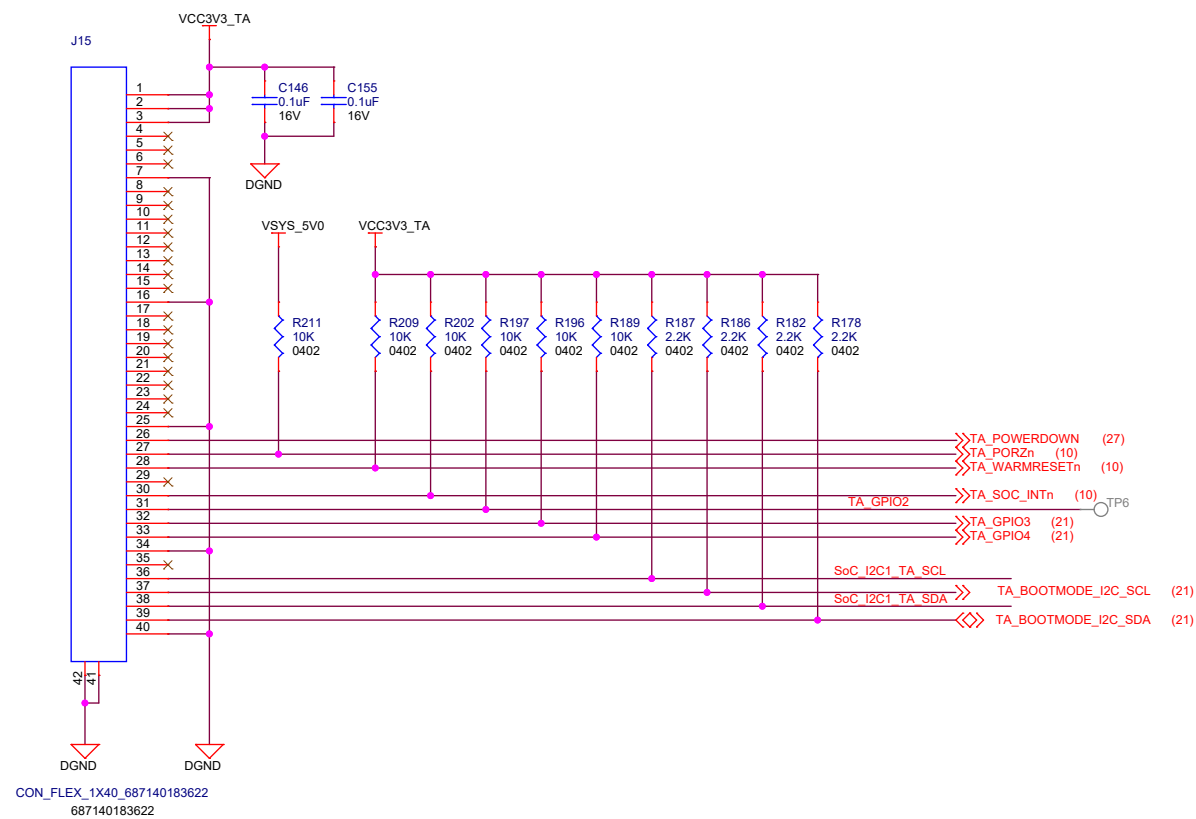
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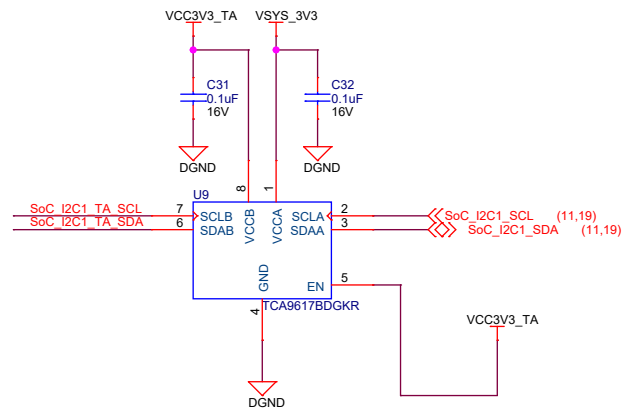
Title: BOOSTERPACK CONNECTOR

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40 - Pin Test Automation Header



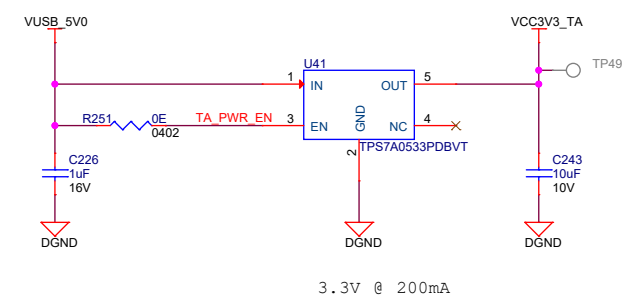
I2C Buffer for TA Header



Test Automation GPIO Mapping

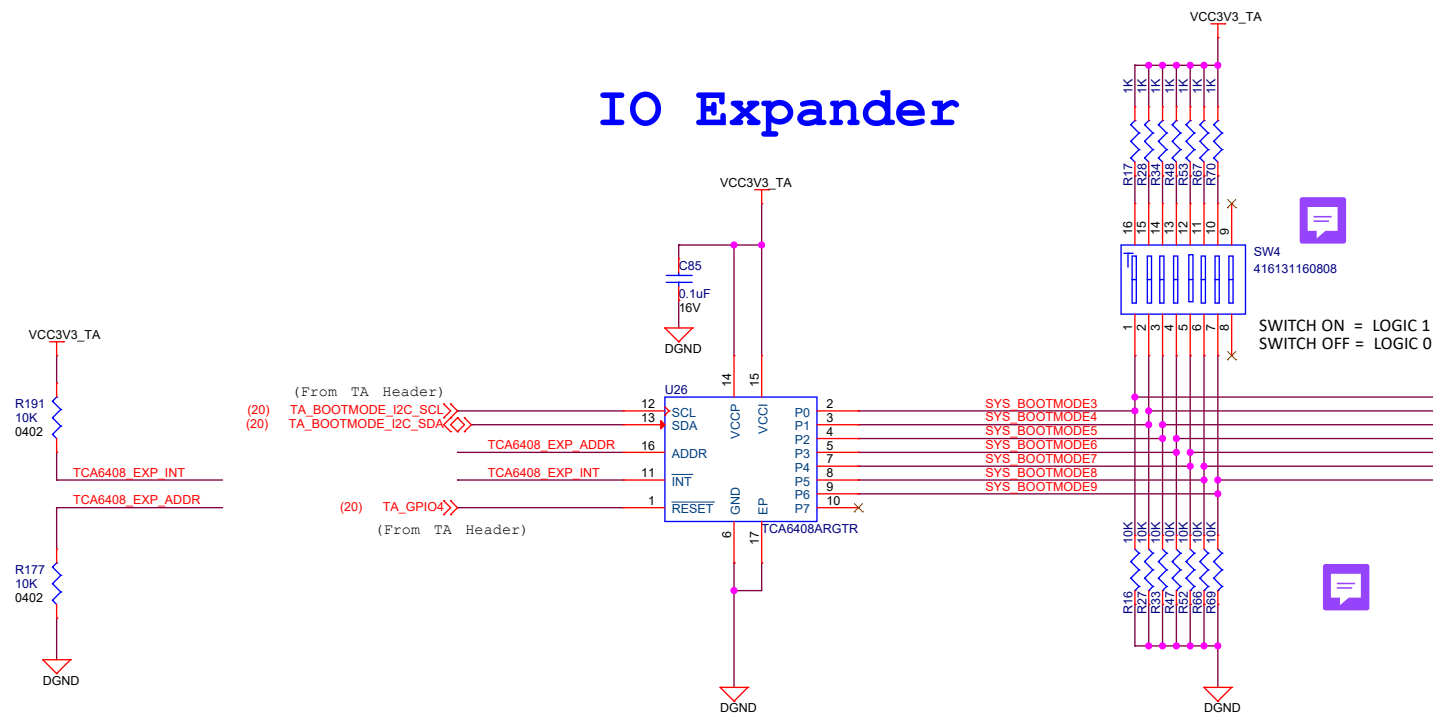
SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External FU/PD states
TA_POWERDOWN	Used to Powerdown the Board	OUTPUT	External Pullup
TA_PORZn	Used to Reset the SoC PORZ	OUTPUT	External Pullup
TA_WARMRESETh	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TA_GPIO3	Used to Disable the BOOTMODE Buffer	OUTPUT	External Pullup
TA_GPIO4	Used to Reset the BOOTMODE IO Expander	OUTPUT	External Pullup
TA_SOC_INTn	Interrupt to SoC	OUTPUT	External Pullup

Test Automation Board Power

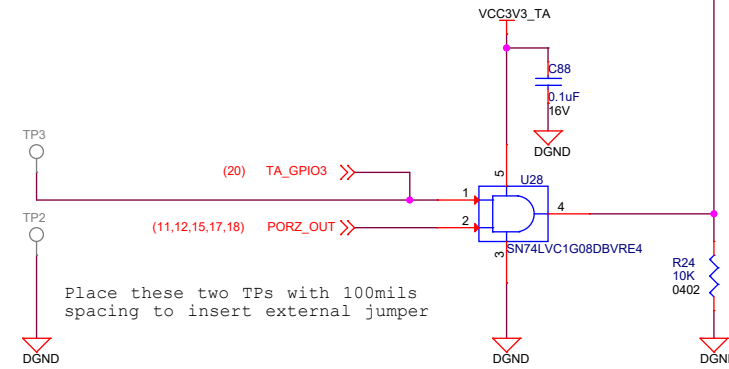
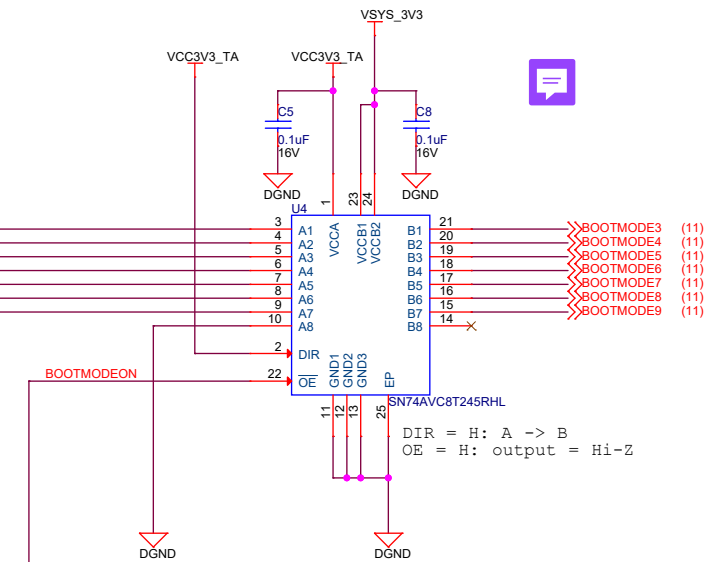


BOOT Mode Switch

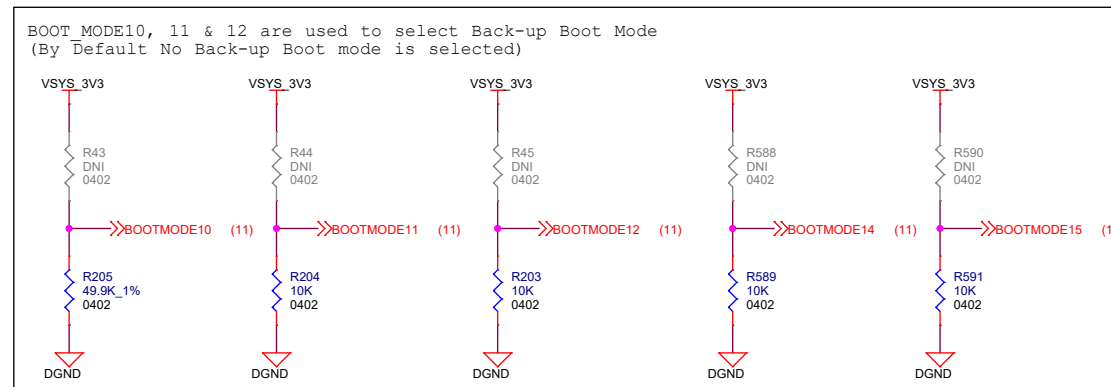
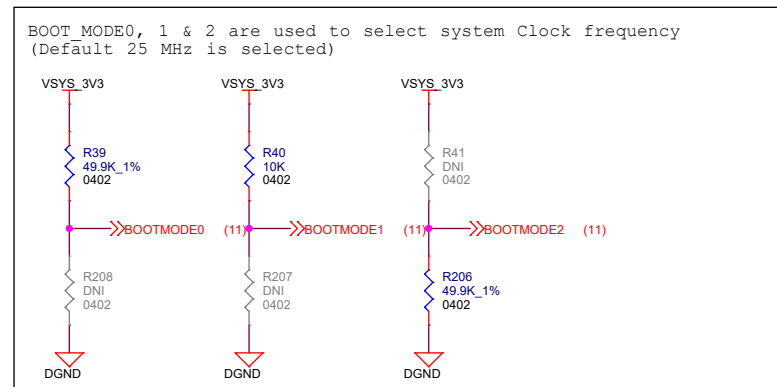
IO Expander



BOOT Mode Buffer



AM243x LP - Boot-Mode selection table							
Boot Modes Supported							
	SW4.1	SW4.2	SW4.3	SW4.4	SW4.5	SW4.6	SW4.7
QSPI FLASH	0	1	0	0	0	1	0
MMC1/SD Card	0	0	0	1	0	0	1
UART	1	1	1	0	0	0	0
USB - DFU	0	1	0	1	0	0	0
No Boot	1	1	1	1	0	0	0



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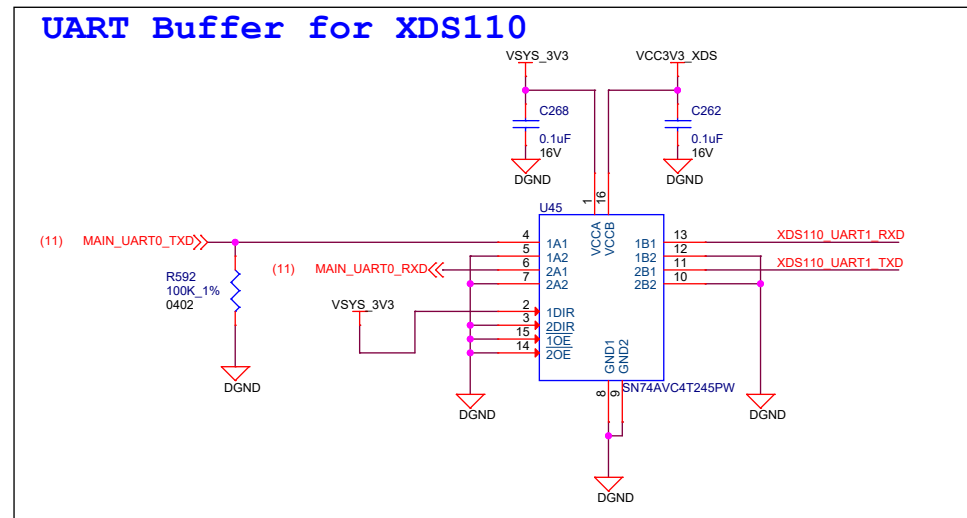
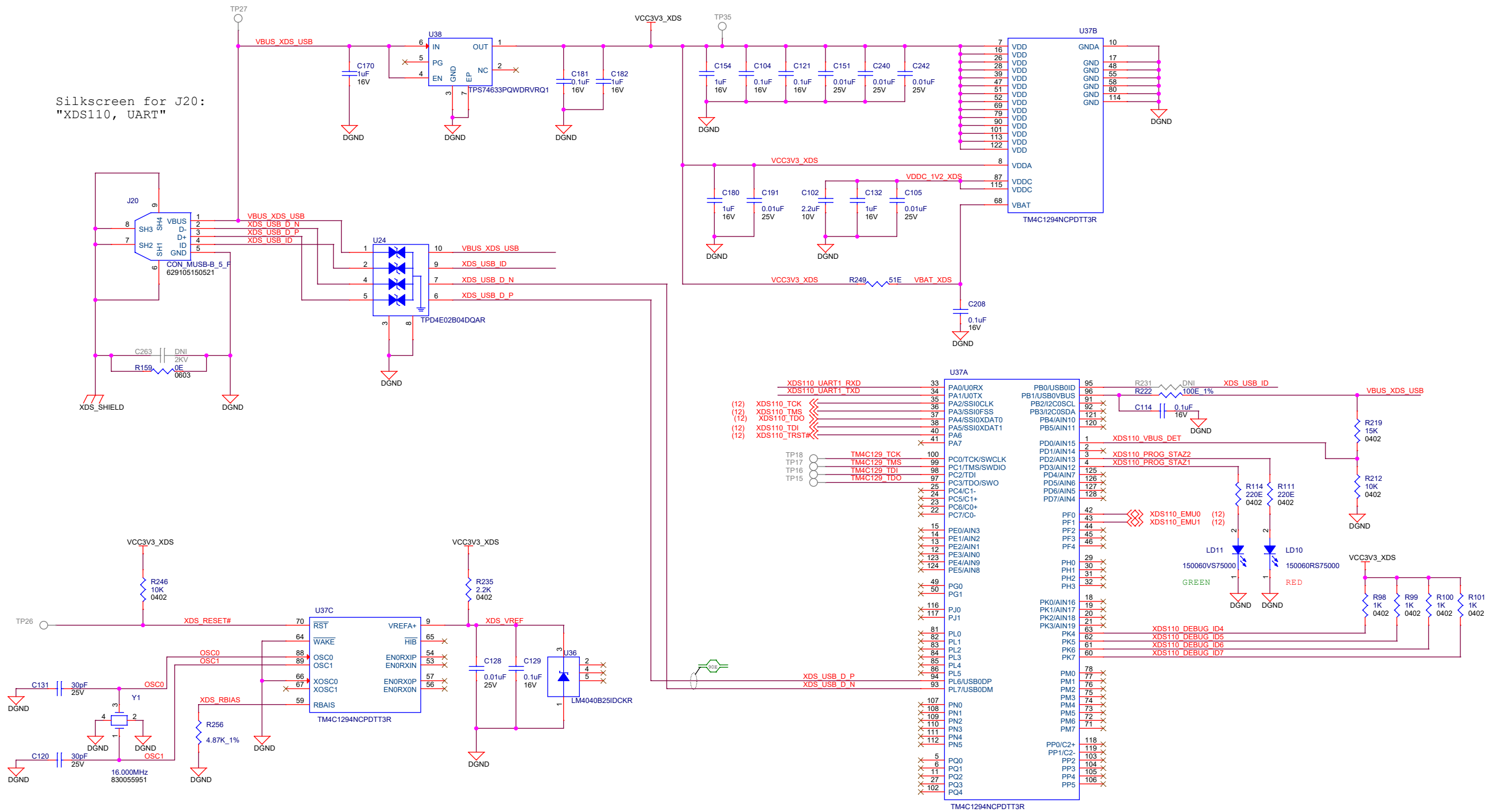


Title: BOOT MODE BUFFER & SWITCHES

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XDS110 Debugger

Silkscreen for J20:
"XDS110, UART"

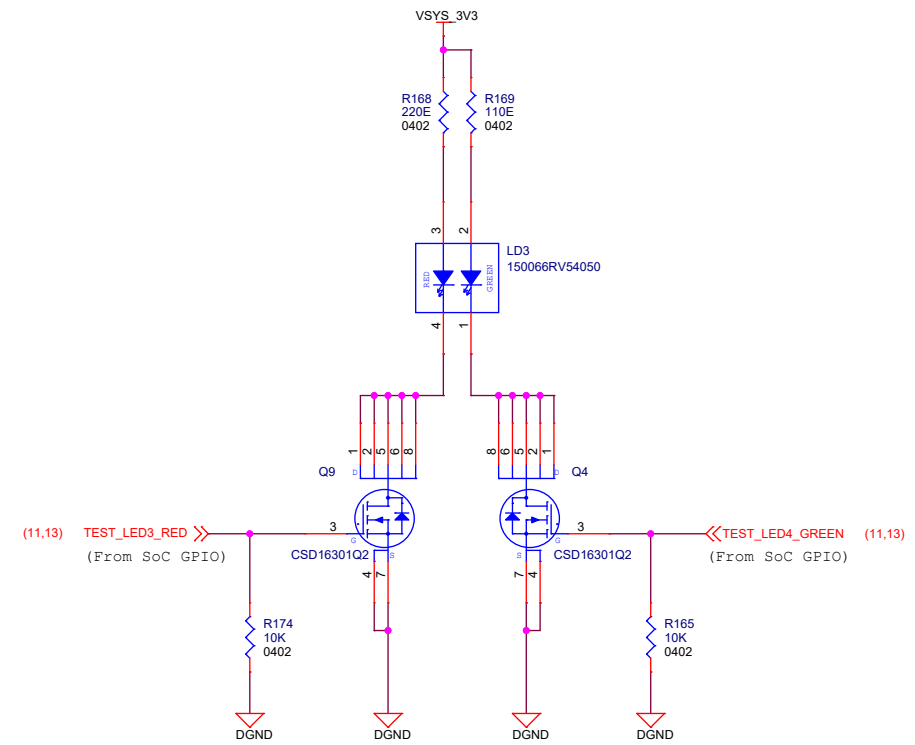
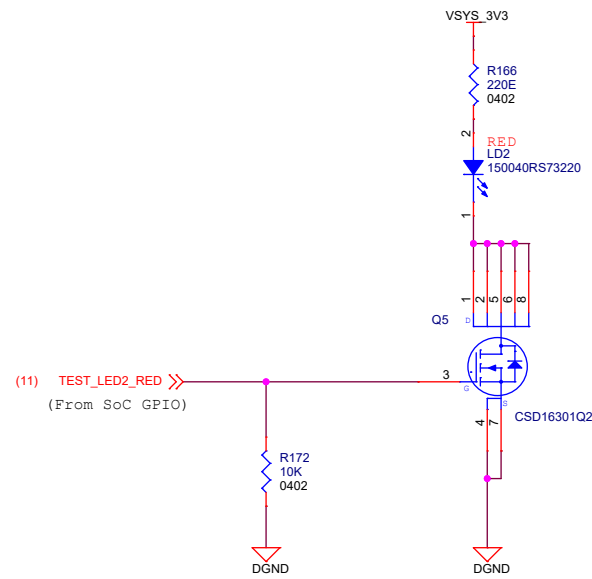
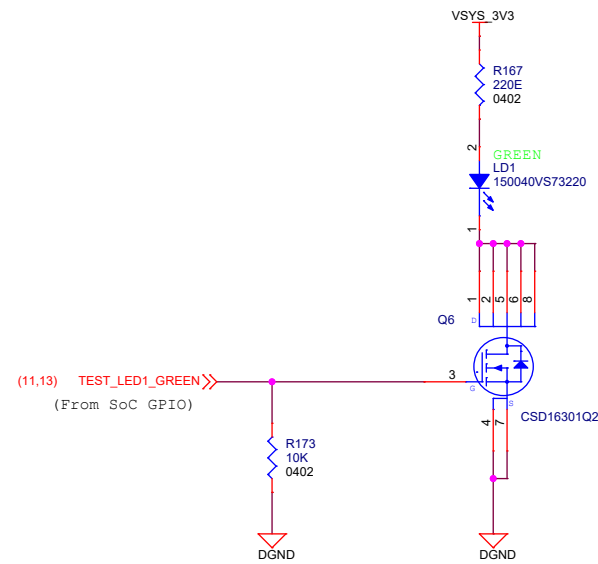
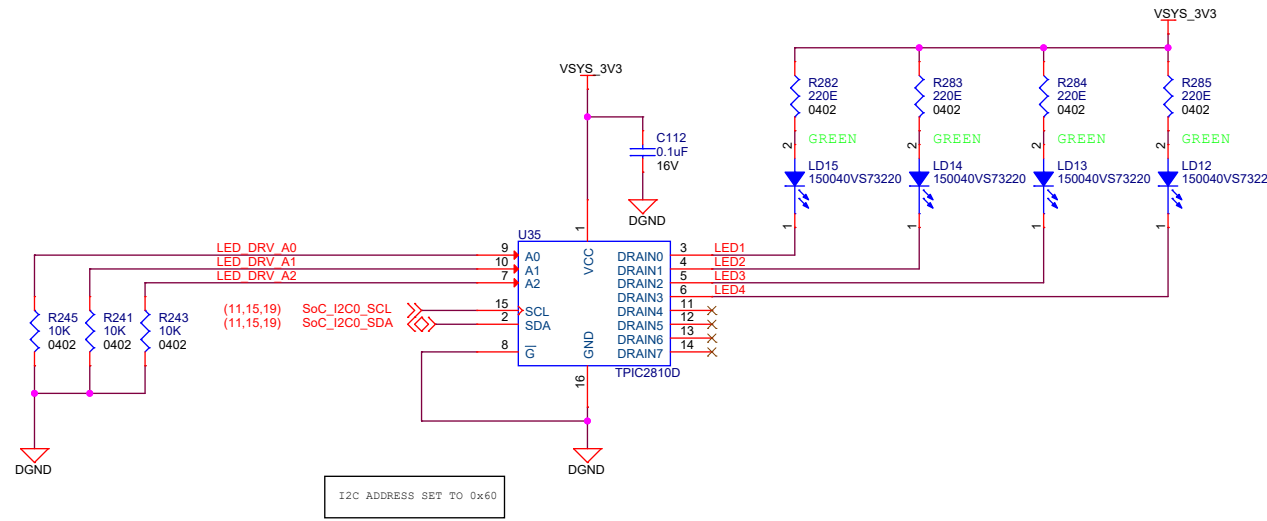


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Title		XDS110 DEBUGGER	
Size	PROC109 LP AM243	Rev	A
Date:	Wednesday, September 13, 2023	Sheet	22 of 29

Industrial Communication LEDs



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Title INDUSTRIAL COMMUNICATION LEDs

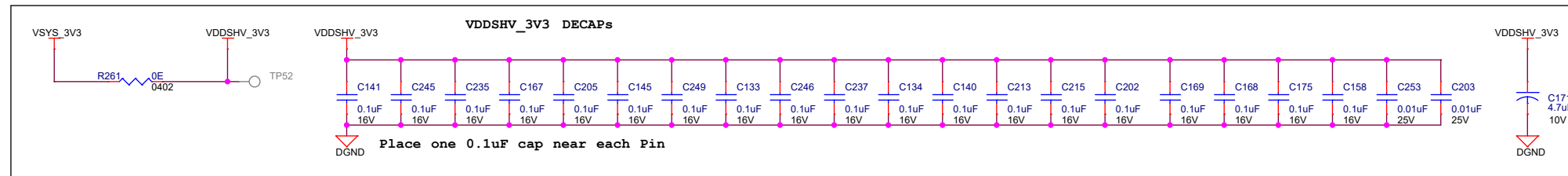
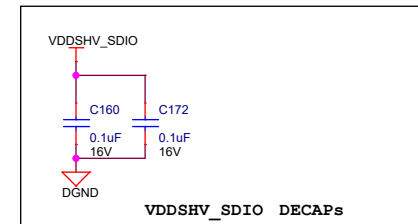
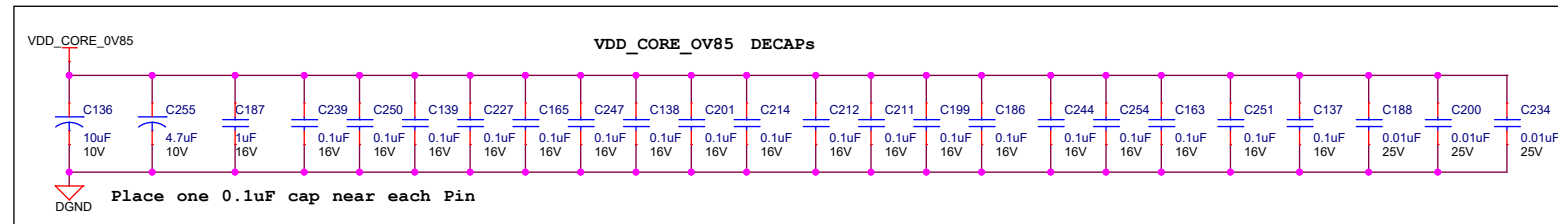
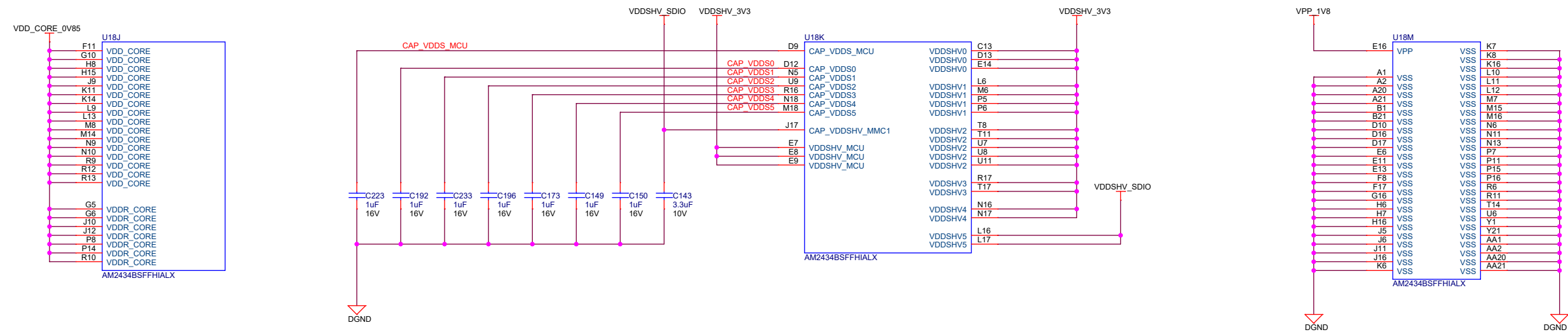
Size PROC109 LP AM243

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SoC Digital POWER & DECAPS

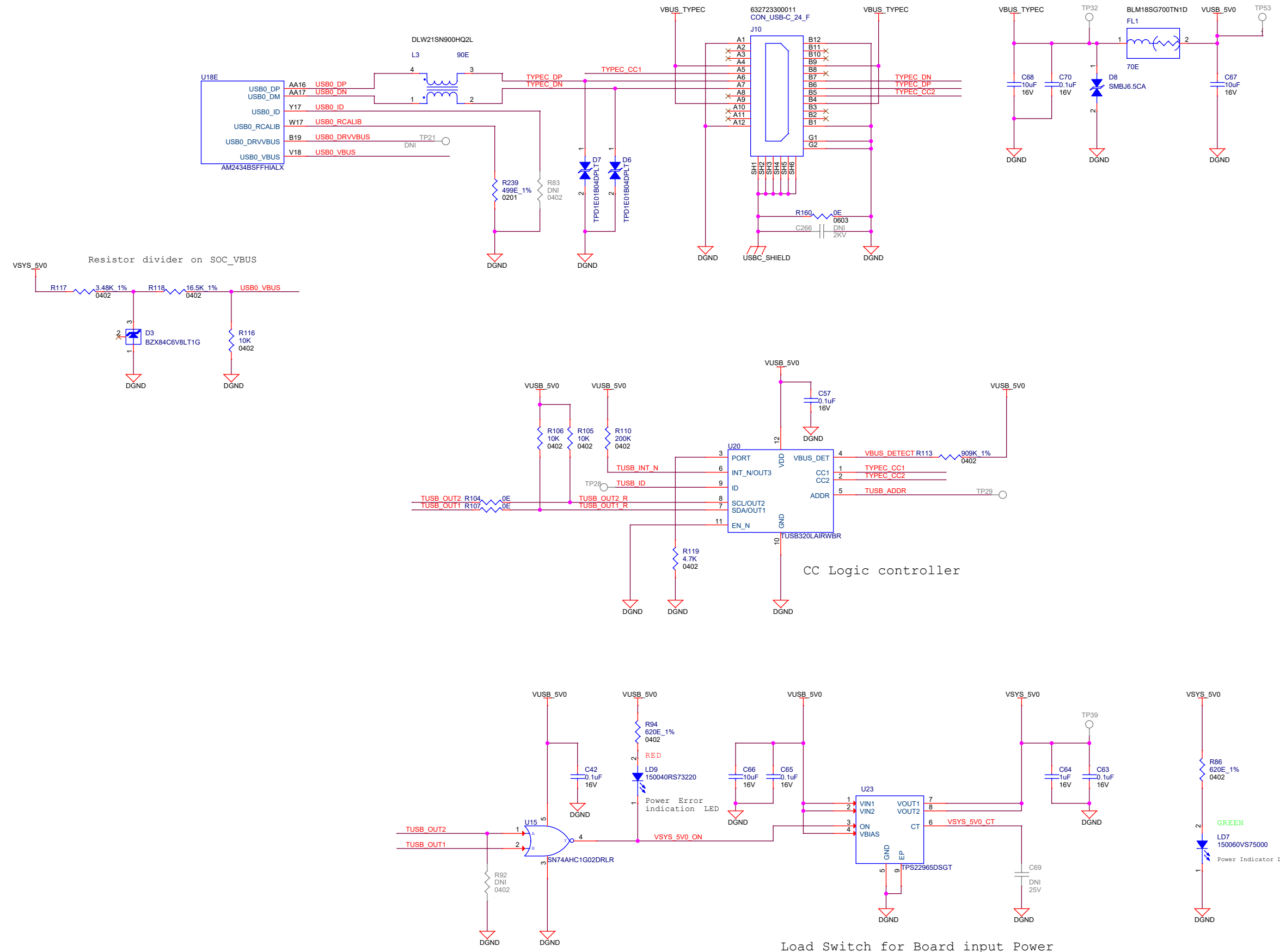


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Title		SoC Digital POWER & DECAPS	
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Type C Connector for Power Input & USB2.0



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Title BOARD POWER INPUT & USB2.0

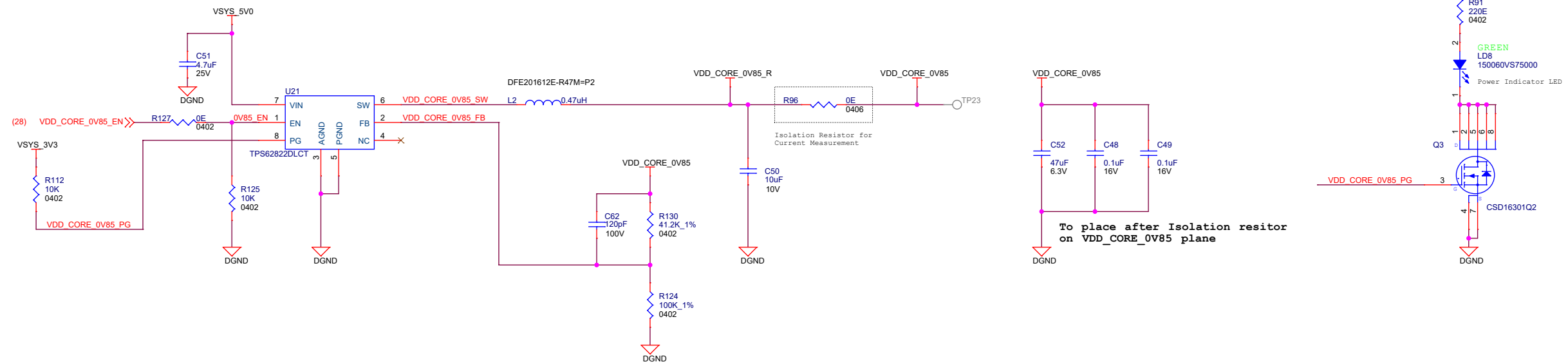
Size PROC109 LP AM243

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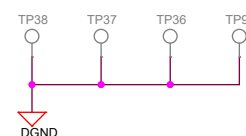
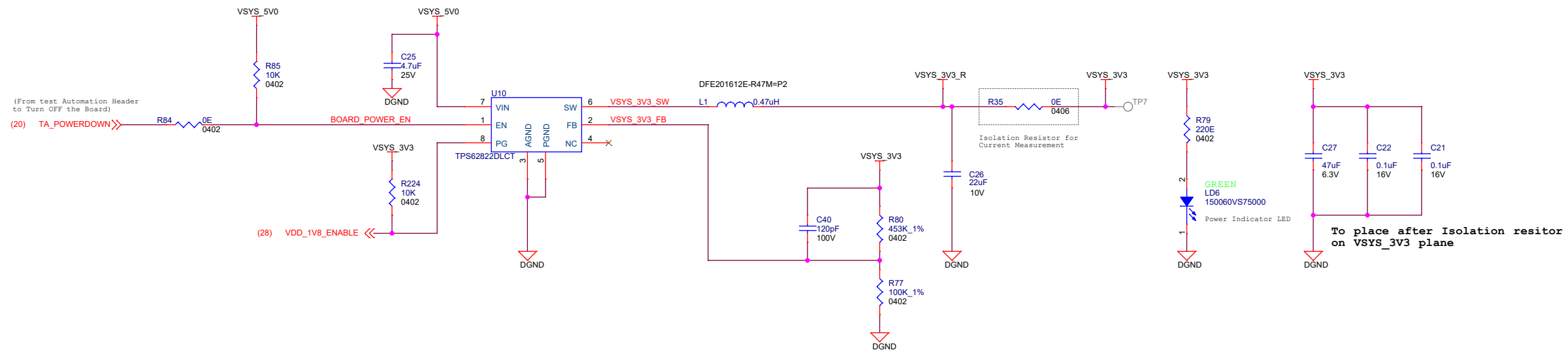
Core Voltage Generator

(0.85V, 2A)



Peripheral Voltage Generator

(3.3V, 2A)



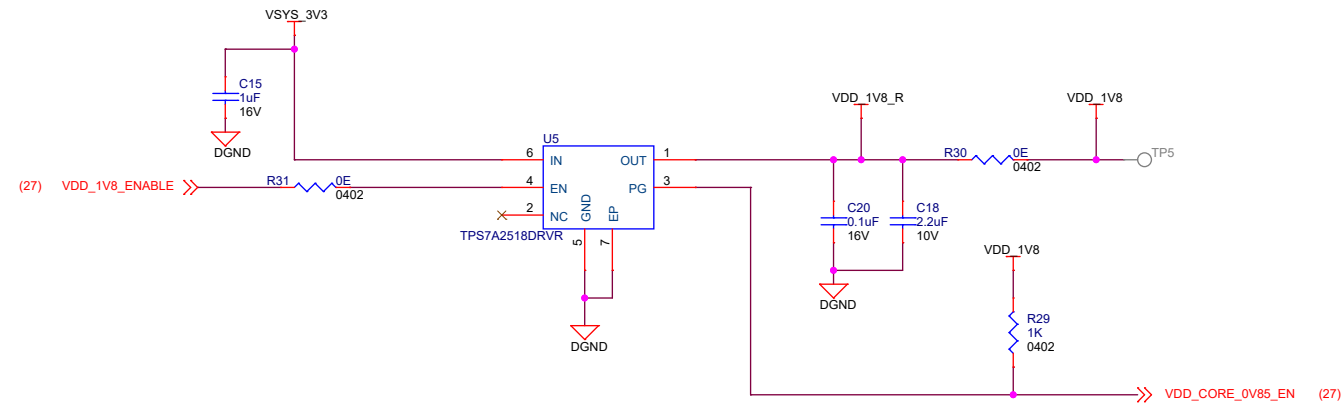
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Title		BOARD POWER_01	
Size	PROC109 LP AM243	Rev	A
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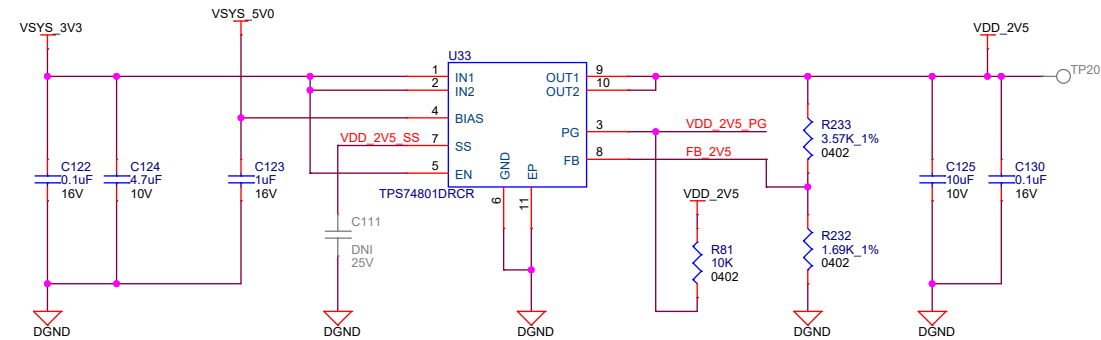
Analog Voltage LDO

(1.8V, 300mA)

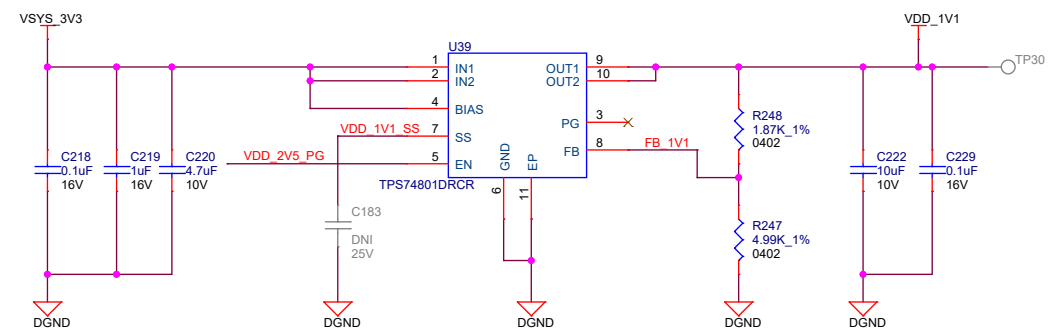


EPHY LDOs

3.3V to 2.5V

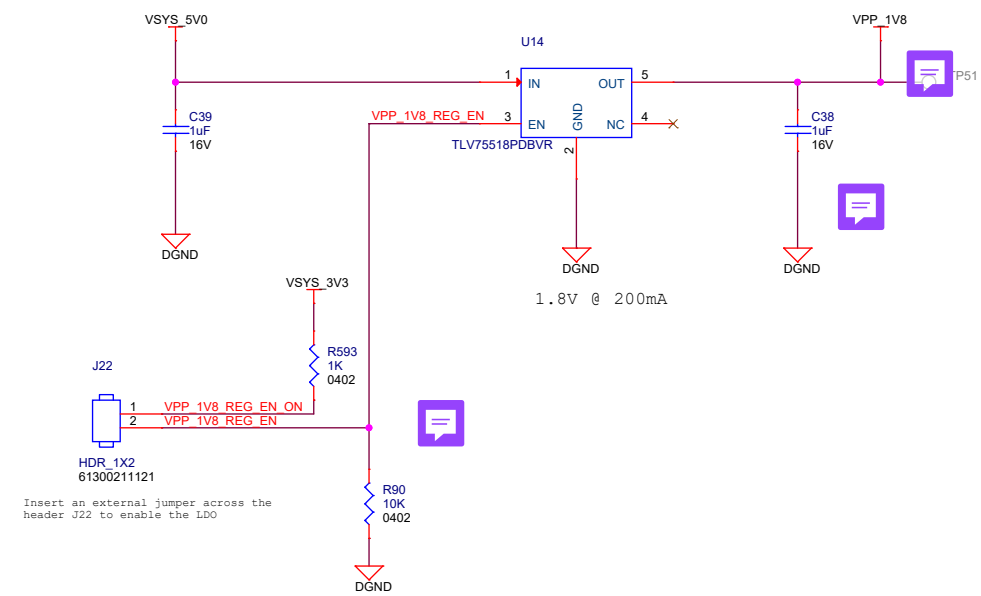


3.3V to 1.1V



eFUSE Programming Voltage LDO

(1.8V, 200mA)



HARDWARE SCHEMATICS

ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.
2. PCB should be baked at 120 degree for 8 hours.
3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
4. These assemblies are ESD sensitive, ESD precautions shall be observed.
5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
6. Provide serial numbers to the assembled boards for identification.
7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

Fiducials

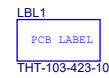


BARE PCB



LABELS

Board Serial No.



Assembly Revision



LOGOs

PCB LOGO
DNI
Texas Instruments

PCB LOGO
DNI
TI Launch Pad Logo with web link

PCB LOGO
DNI
Mistral Solutions

PCB LOGO
DNI
WEEE Mark

PCB LOGO
DNI
CE Mark

PCB LOGO
DNI
For Evaluation only; not FCC approved for resale

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Title: HARDWARE SCHEMATICS

Size: C
PROC109 LP AM243

Rev: A

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