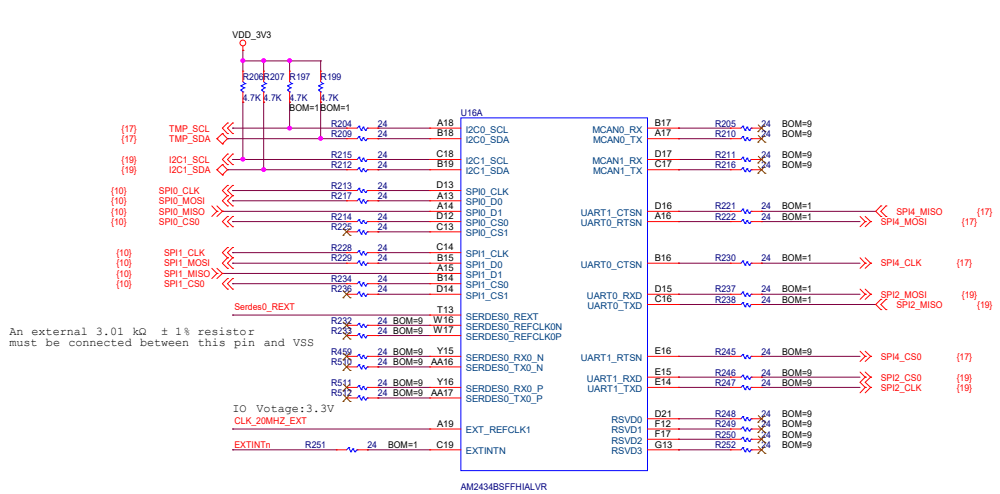
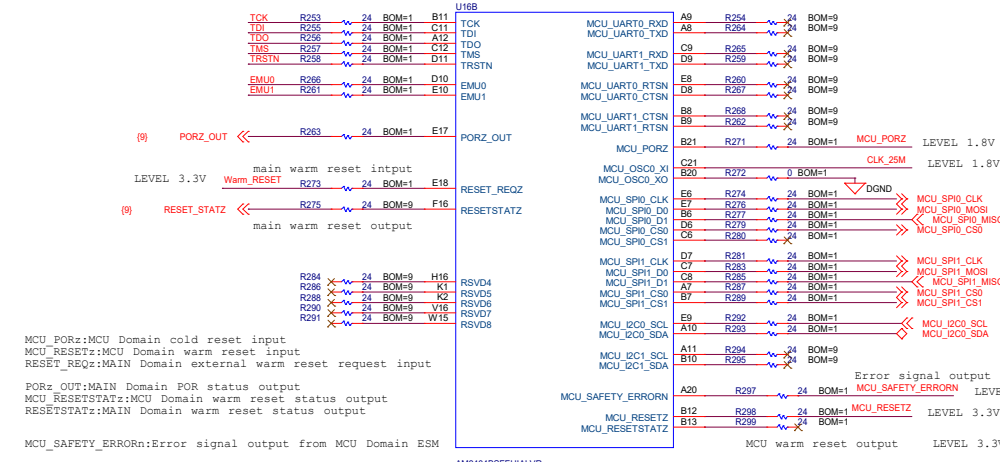




An external 3.01 kΩ ± 1% resistor must be connected between this pin and VSS

TO Voltage: 3.3V
CLK_20MHz_EXT

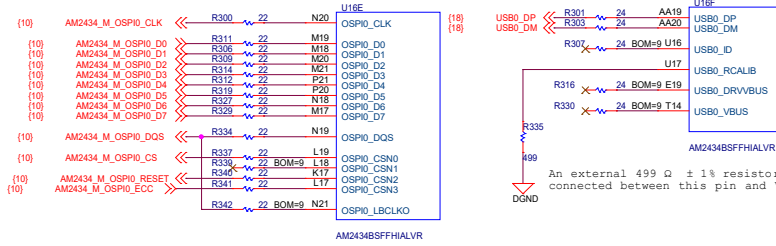
Terminate external warm reset inputs MCU RESETz and RESET REQz as per the Pin Connectivity Requirements section of the device-specific data sheet. Warm reset inputs (LVCMOS type I/Os) have input slew rate requirements. Connecting a capacitor directly at the input is not recommended due to the slow input ramp. A schmitt trigger based debouncing logic is recommended. Refer device-specific EVM schematics for implementing the debouncing logic.



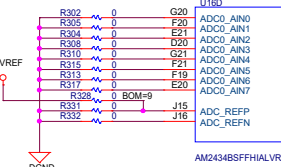
MCU PORZ:MCU Domain cold reset input
MCU RESETz:MCU Domain warm reset input
RESET REQz:MAIN Domain external warm reset request input

PORz_OUT:MAIN Domain POR status output
MCU RESETSTATz:MCU Domain warm reset status output
RESETSTATz:MAIN Domain warm reset status output

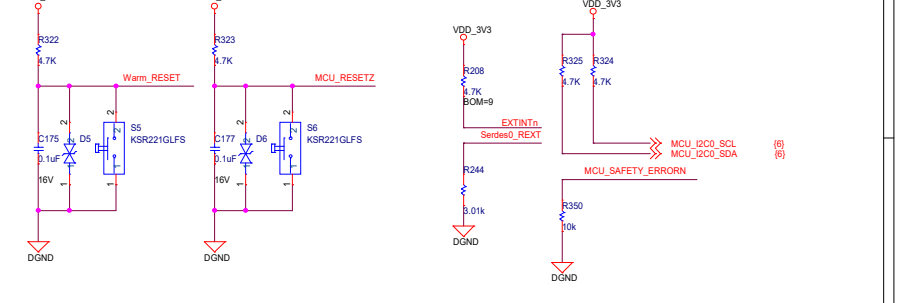
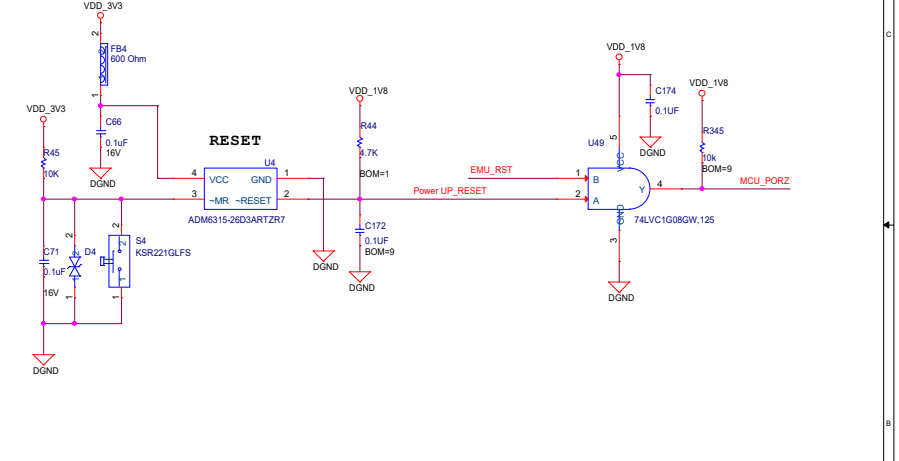
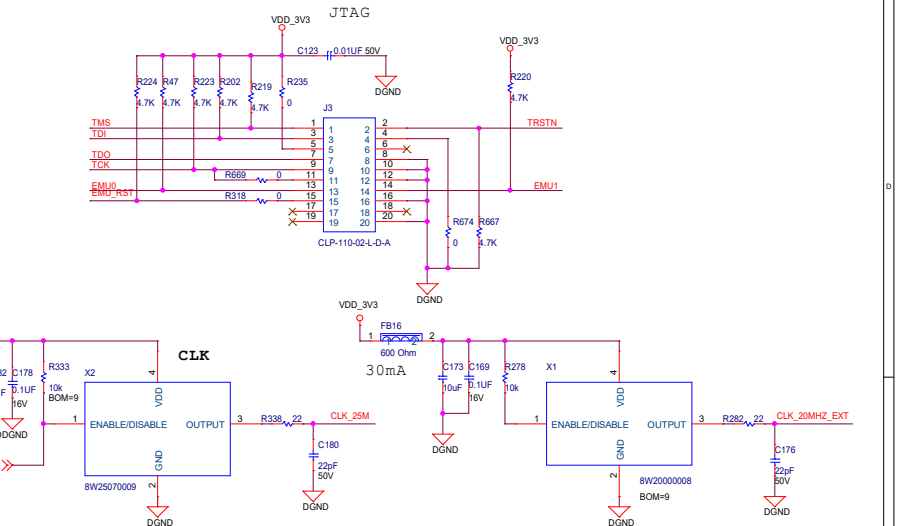
MCU SAFETY_ERRORn:Error signal output from MCU Domain ESM

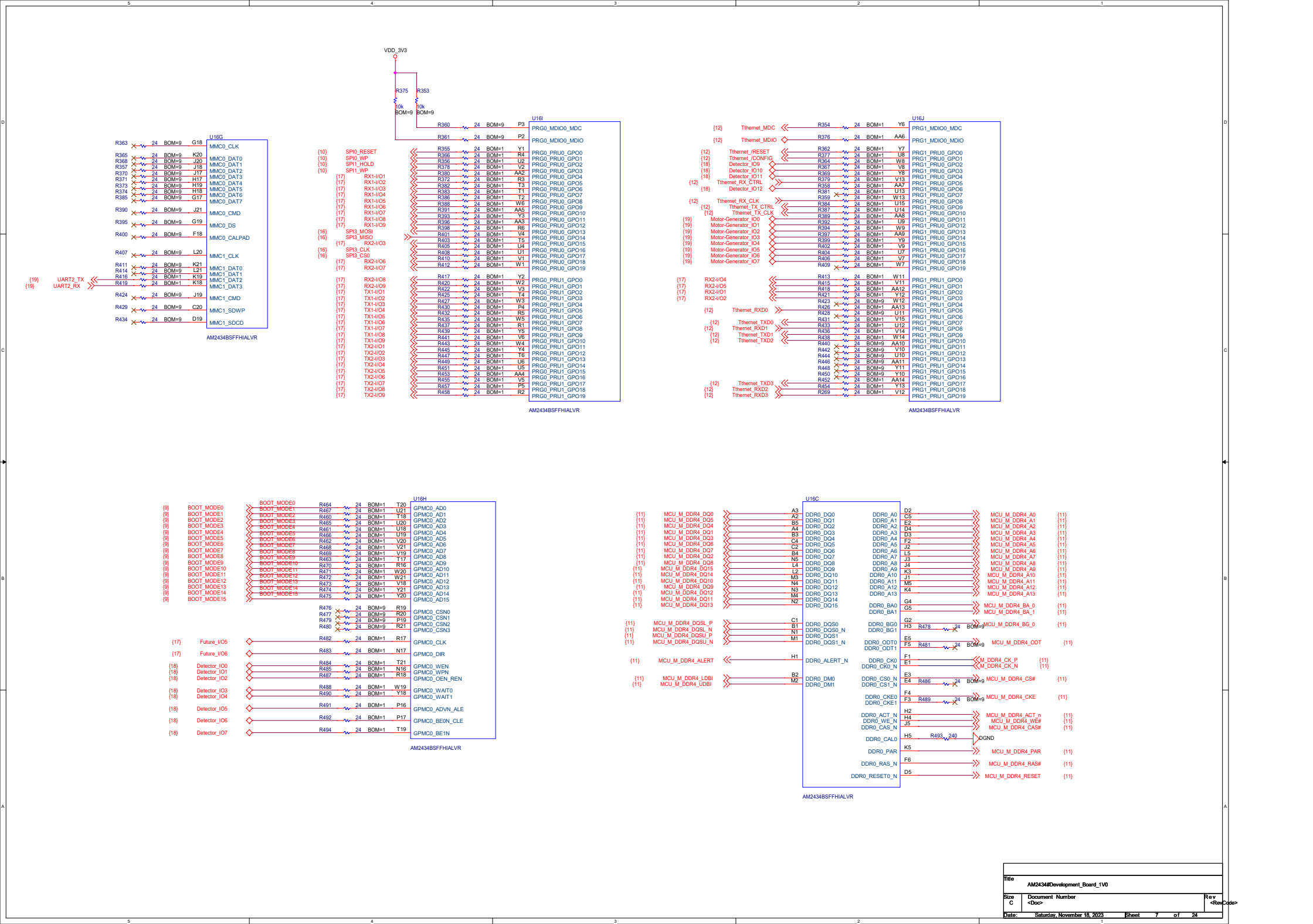


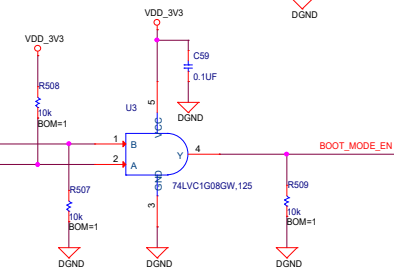
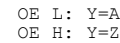
An external 499 Ω ± 1% resistor must be connected between this pin and VSS.



If the entire ADC0 is not used, each of these balls must be connected directly to VSS.







15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Reserved	Backup Boot Mode Config	Backup Boot Mode			Primary Boot Mode			Primary Boot Mode			PLL Config			

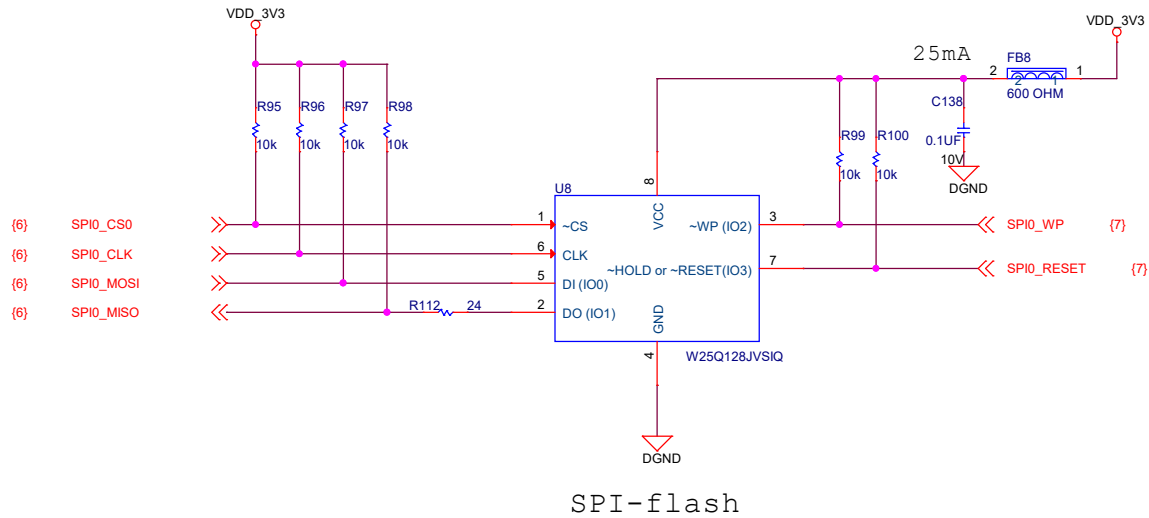
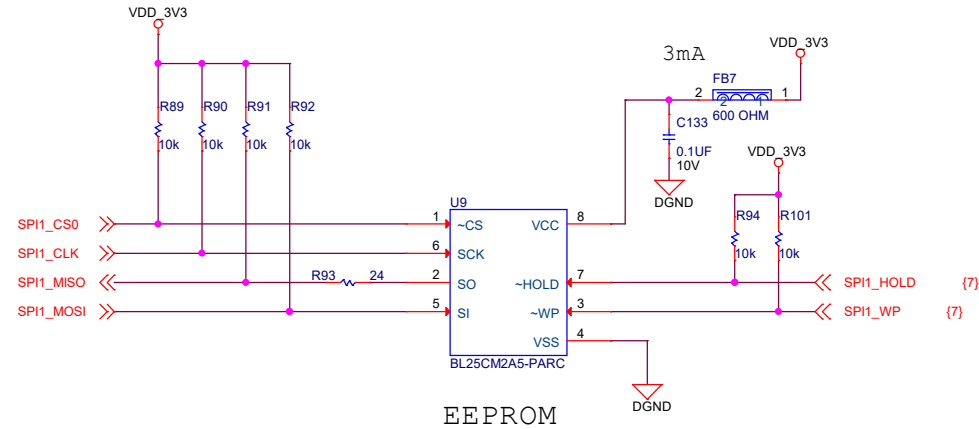
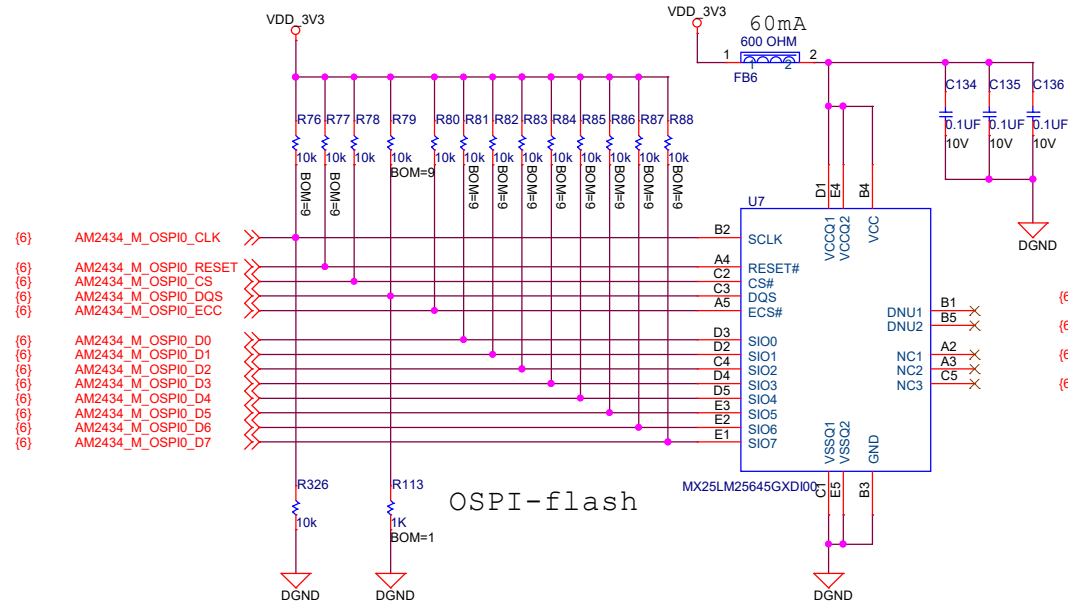
PLL Config Pins			Ref Clock (MHz)
B2	B1	B0	
0	1	1	25

Primary Boot Mode Config							Primary Boot Mode
B9	B8	B7	B6	B5	B4	B3	
Reserved	Reserved	Reserved	1	0	0	1	eMMC Boot
Core Volt	Mode	Lane Swap	1	0	1	0	USB
Reserved	Reserved	Reserved	1	0	1	1	GPFC NAND
Reserved	Reserved	Reserved	1	0	0	0	GPFC MGR
Reserved	Reserved	Clocking	1	1	0	1	PCIe
SFPD	Read Cmd	Mode	1	1	1	0	xSPI
Reserved	Reserved	NoDev	1	1	1	1	No-Boot/Dev boot

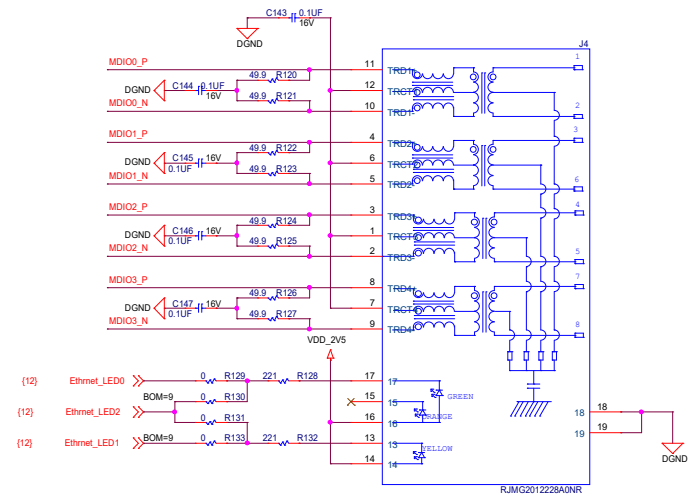
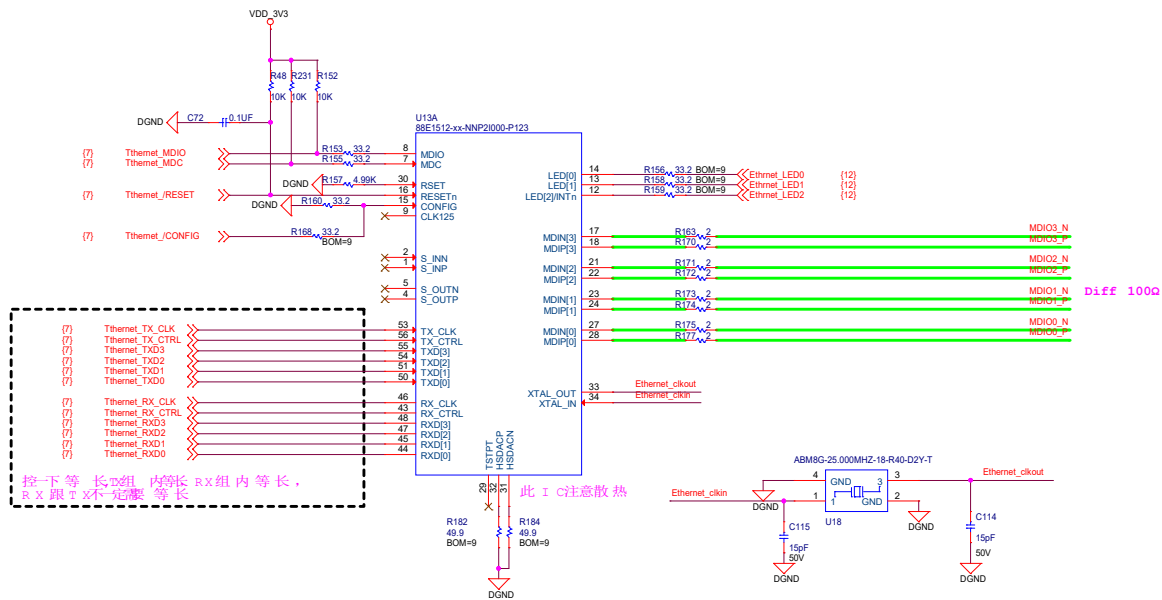
Primary Boot Mode Config							Primary Boot Mode
B9	B8	B7	B6	B5	B4	B3	
Reserved	Reserved	Reserved	0	0	0	0	Reserved
Reserved	lck	Csel	0	0	0	1	CSPI
Reserved	lck	Csel	0	0	1	0	CSPI
Reserved	Mode	Csel	0	0	1	1	SP1
Clkout	0	Link Info	0	1	0	0	Ethernet RGMII
Clkout	Clk src	0	1	1	0	1	Ethernet RMII
Bus reset	Reserved	Addr	0	1	1	0	UART
Reserved	Reserved	Reserved	0	1	1	1	I2C
Port	Reserved	Fstrw	1	0	0	0	MMC/SD Boot (SD Card Boot or eMMC Boot using UDA)

Backup Boot Config	Backup Boot Mode Selection				Backup Boot Mode Selected
B13	B12	B11	B10		
Reserved	0	0	0		None
Mode	0	0	1		USB
Reserved	0	1	0		Reserved
Reserved	0	1	1		UART
IF	1	0	0		Ethernet
Port	1	0	1		MMCSD Boot (SD Card Boot or eMMC Boot)
Reserved	1	1	0		SPI
Reserved	1	1	1		I2C

BOOTMODE PIN Mapping															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Reserved	Backup Boot Mode Config	Backup Boot Mode			Primary Boot Mode Config			Primary Boot Mode				PLL Config		
0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1
															OSPI



Title		
AM2434#Development_Board_1V0		
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On power-up, no special power supply sequencing is required.

