AM263x CC Bootmode Isolation Example

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AM263x Device Requirements

This document describes the HW mechanisms used on the AM263x Control Card to implement bootmode/SOP pin functionality without interfering with the application-based default functionality of the pin.

The system requirements are described below based on IC/Function:

AM263x SoC Requirements:

AM263x attempts to simplify the power reset requirements from previous Sitara MCU devices.

There is no sequencing requirement with respect to the primary core digital VDD 1.2-V and I/O power 3.3-V rails.

A pair of on-die LDO are supplied through the VDDS33 power net. These on-die LDO generate the required VDDS1V8 and VDDA1V8 1.8V digital and **analog** power.

The AM263x does require the minimum ramp time be respected for 3.3-V power-on.

Additional PORz and SOP boot mode latch timing must be respected by the **HW** design as well.

Table 7-3. AM263x Power-On Sequencing

TIMING PARAMETER	MIN (ms)	MAX (ms)	COMMENTS
$t_{Startup}$	-	-	Time for 1.2-V and 3.3-V DC-DC converters to startup after initial 5.0-V power on. This is an arbitrary amount of time - no constraint imposed by the device.
t_{PGood}	-	-	Time for Power Good signals to be generated from DC-DC converters after rails are stable. This is an arbitrary amount of time - no constraint imposed by the device.
t_{Ramp_3V3}	0.1		Ramp time of the VDDS3V3 and VDDA3V3 supplies. This is a requirement imposed by the device.
t_{PORz}	-	-	Time from 1.2-V and 3.3-V power good generation to de-assertion of PORz. This is an arbitrary amount of time - no constraint imposed by the device.
$t_{SOP\_Sampled}$	1.0		Time from PORz de-assertion until the SOP[3:0] pins are sampled. This is a requirement imposed by the device.
t_{SU_SOP}	TBD	TBD	Setup time relative to SOP sample time.
t_{H_SOP}	TBD	TBD	Hold time relative to SOP sample time.
$t_{WARMRSTz}$	2.0	-	Time from PORz de-assertion until the device de-asserts the WARMRESETz signal.
t_{XO_Stable}	TBD	TBD	Time from PORz de-assertion until the device has a stable reference frequency from the attached XTAL.

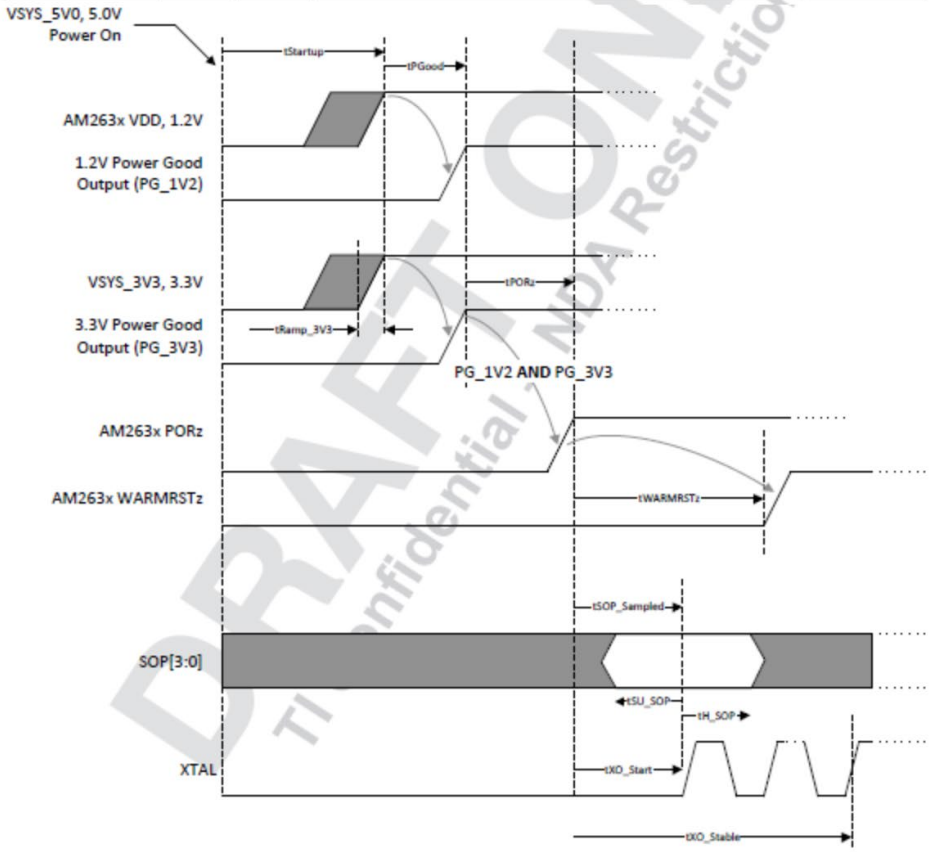


Figure 7-1. Power-Up Sequencing

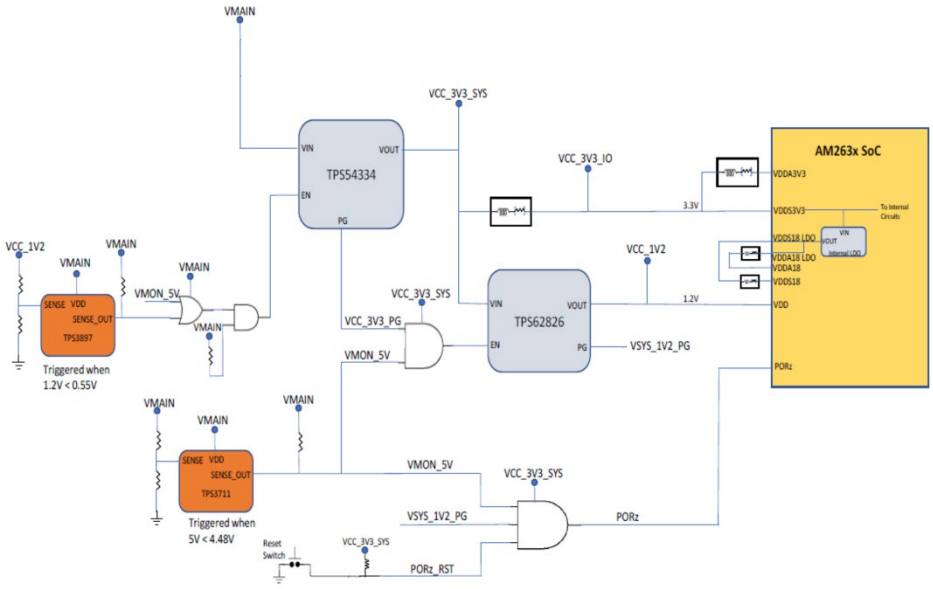
SOP pins and PORz Reset

-SOP pins must be latched in accordance with PORz device requirements as described in the device datasheet.

AM263x EVM HW Expectations

The following set of steps shall occur on AM263x EVM HW to boot the device from power-on reset.
1. PORz is held low by the external power supply monitor.
2. VDD core digital 1.2V and VDDS3V3/VDDA3V3 3.3V supplies ramp to their nominal voltages.
    a. This requires a logical AND be applied to the power good signal generated from each supply.
3. SOP[3:0] pins held in their boot latch state.
4. After PCB supplied power nets are stable, the external supply monitor will de-assert PORz.
5. Device will startup 1.8V on-die LDO.
6. After internal supply monitors show externally and internally generated supplies are stable, the SOP[3:0] pin states are latched.
7. Device starts XTAL oscillator.
8. R5F cores are unhalted and SOP selected boot ROM execution begins.

Click here to expand AM263x CC Simplified Power Diagram...



HW Implementation Details

This diagram demonstrates the AM263x Control Card HW mechanisms used to implement bootmode/SOP pins. One of the critical requirements of the SOP pins is that the bootmode latch **does not** interfere with the default functionality of the pin outside of the PORz reset.

In the schematic extraction below, this functional isolation is enabled by the QSPI0_D0 (SOP0) and QSPI_D1 (SOP1) channels.

AM263x Control Card (TMDSCNCD263) Design Files: https://www.ti.com/lit/zip/sprcak1

AM263x Control Card EVM User Guide: https://www.ti.com/lit/pdf/spruj09

S25FL128S (QSPI Flash Device)

Product Link: https://www.infineon.com/cms/en/product/memories/nor-flash/standard-spi-nor-flash/quad-spi-flash/s25fl128sagnfi001

Datasheet Link: https://www.infineon.com/dgdl/Infineon-S25FL128S_S25FL256S_128_Mb_(16_MB)_256_Mb_(32_MB)_3.0V_SPI_Flash_Memory-DataSheet-v18_00-EN.pdf?fileId=8ac78c8c7d0d8da4017d0ecfb6a64a17

SN74AVC4T245 (4-bit dual-supply bus transceiver)

Product Link: https://www.ti.com/product/SN74AVC4T245

Datasheet Link: https://www.ti.com/lit/gpn/sn74avc4t245

Note: A newer version of this 4-bit dual-supply bus transceiver is available with increased performance: https://www.ti.com/product/SN74AXC4T245

The SN74AVC4T245 will drive the #B# pins to a high impedance (Hi-Z) state when BOOTMODEON is driven high (Functional-Mode/Truth-Table included below for reference).

8.4 Device Functional Modes

Table 1. Function Table
(Each 2-Bit Section)(1)

CONTROL INPUTS		OUTPUT CIRCUITS		
$\overline{OE}$	DIR	A PORT	B PORT	OPERATION
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

(1) Input circuits of the data I/Os are always active.

Chronological Power-On/PORz Steps:

Work-In-Progress (TBC)

1. VMAIN On (Board Power is applied)
2. VMAIN applied to VIN for TPS54334 (VCC_3V3_SYS)
3. TBD
4. …
5. TBD
6. BOOTMODEON signal high is delayed by the network highlighted in green
7. During delay SOP pins (set by SW3) latch
8. High (1) applied to (OE) pin of SN74AVC4T245
9. B PORT pins connected to QSPI0_D0/D1 network set to high impedance branch to allow proper functioning of QSPI channels post-boot.