AM263x ADC PSPICE Models

2023-11-08

Summary

- Assembled PSPICE based models of the AM263x SAR ADC
  - Parasitics based on datasheet typical values
  - Models can be used to test attached op-amp and RC charge-bucket filter circuit performance to minimize sampling error
  - Various sample-rate, acquisition and hold timings can be setup
  - Single-ended model available now, can be extended to differential mode model
- PSPICE models assembled using the Cadence PSPICE for TI toolset
  - See: https://www.ti.com/tool/PSPICE-FOR-TI
- Comprehensive SAR ADC circuit selection guide (applicable to AM263x devices) is available here:
  - https://www.ti.com/lit/an/spract6a/spract6a.pdf
  - Written with TINA-TI SPICE simulator in mind, but the concepts are all applicable

Model Description

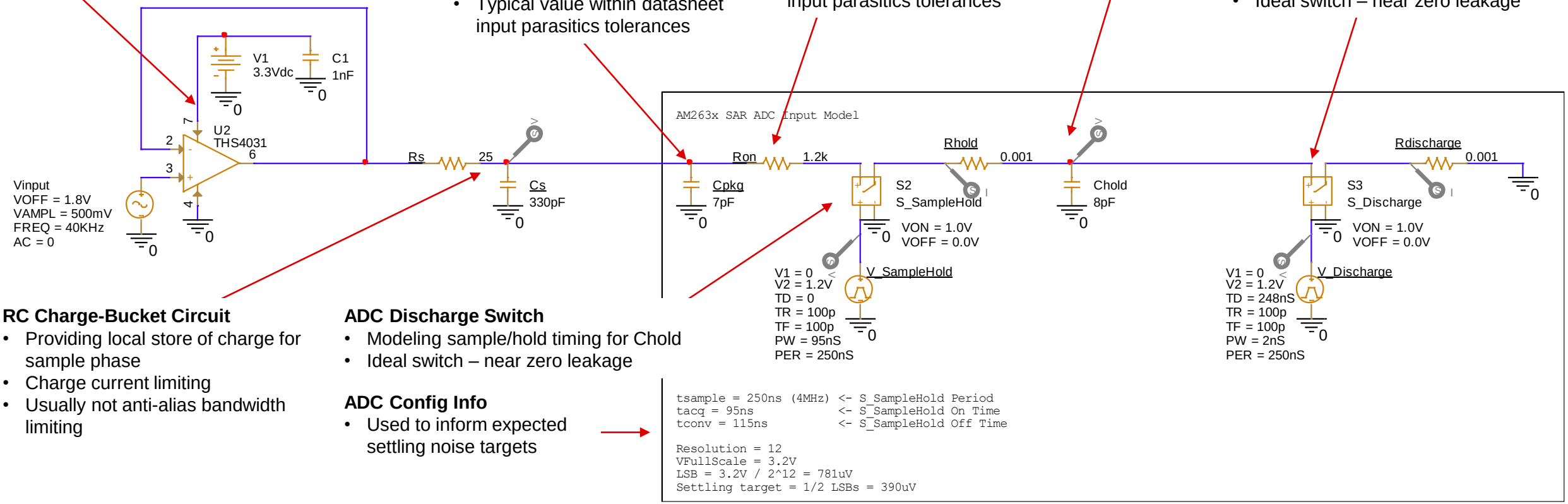
AC Source
- Typical op-amp driver circuit – should be replaced with whatever driver is present in target system
- Should output signal range compatible with datasheet voltage limits

Package Capacitance
- Typical value within datasheet input parasitics tolerances

ADC On Resistance
- Typical value within datasheet input parasitics tolerances

ADC Hold Capacitance
- Typical value within datasheet input tolerances
- Acquisition logic samples this voltage during conversion

ADC Discharge Switch
- Modeling discharge timing for Chold
- Ideal switch – near zero leakage



RC Charge-Bucket Circuit
- Providing local store of charge for sample phase
- Charge current limiting
- Usually not anti-alias bandwidth limiting

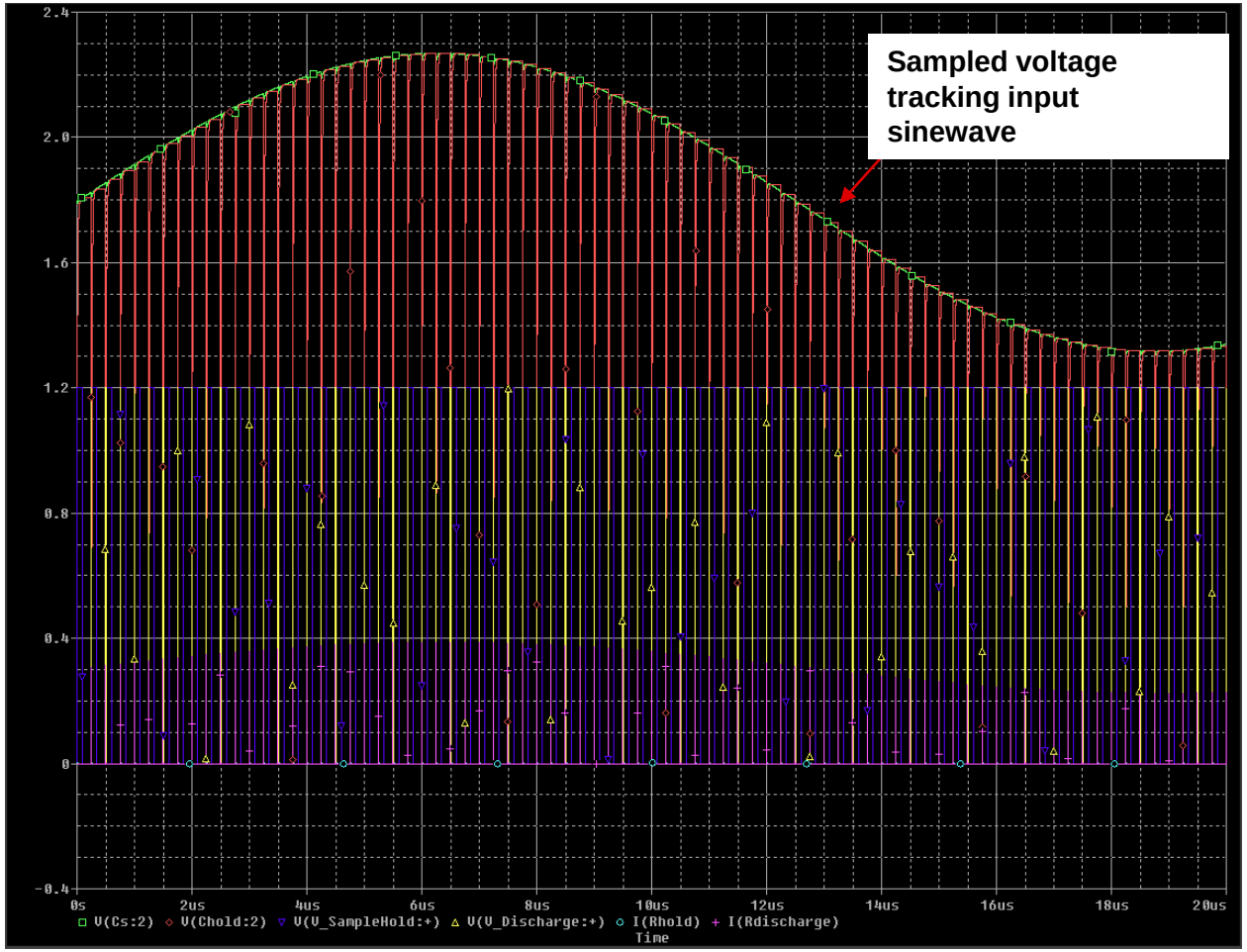
ADC Discharge Switch
- Modeling sample/hold timing for Chold
- Ideal switch – near zero leakage

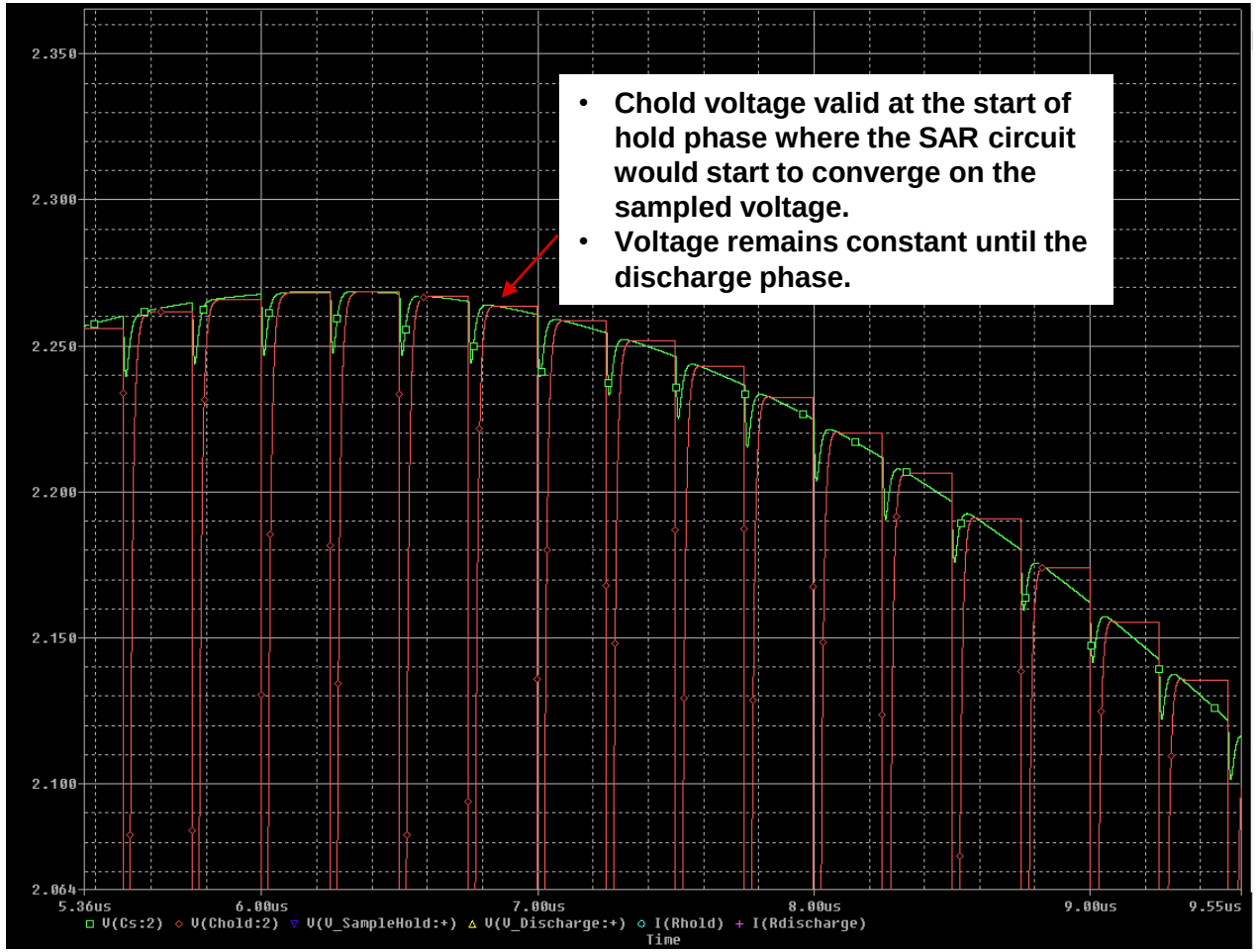
ADC Config Info
- Used to inform expected settling noise targets

```
tsample = 250ns (4MHz) <- S_SampleHold Period
tacq = 95ns            <- S_SampleHold On Time
tconv = 115ns          <- S_SampleHold Off Time

Resolution = 12
VFullScale = 3.2V
LSB = 3.2V / 2^12 = 781uV
Settling target = 1/2 LSBs = 390uV
```

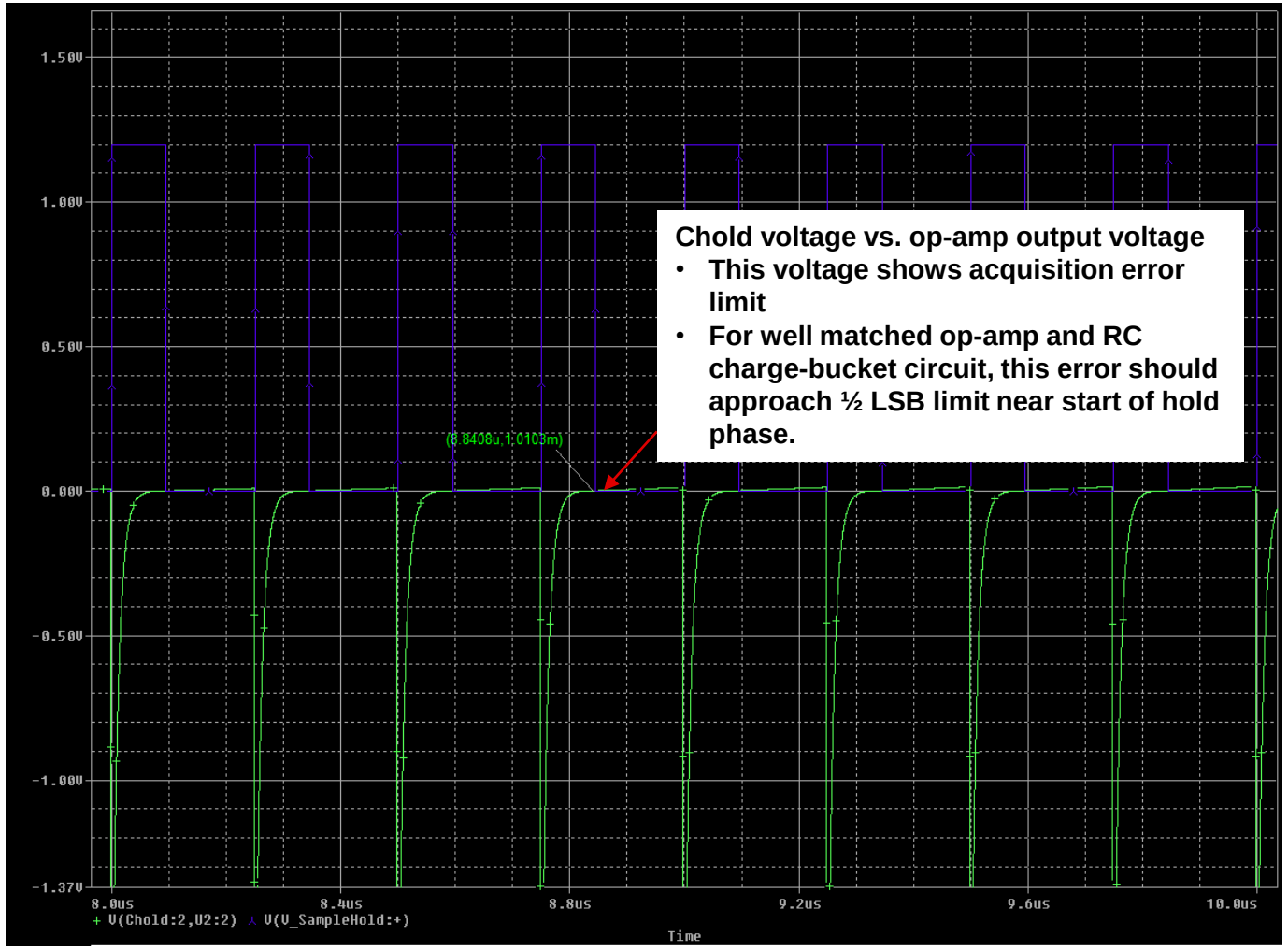
Model Output Example





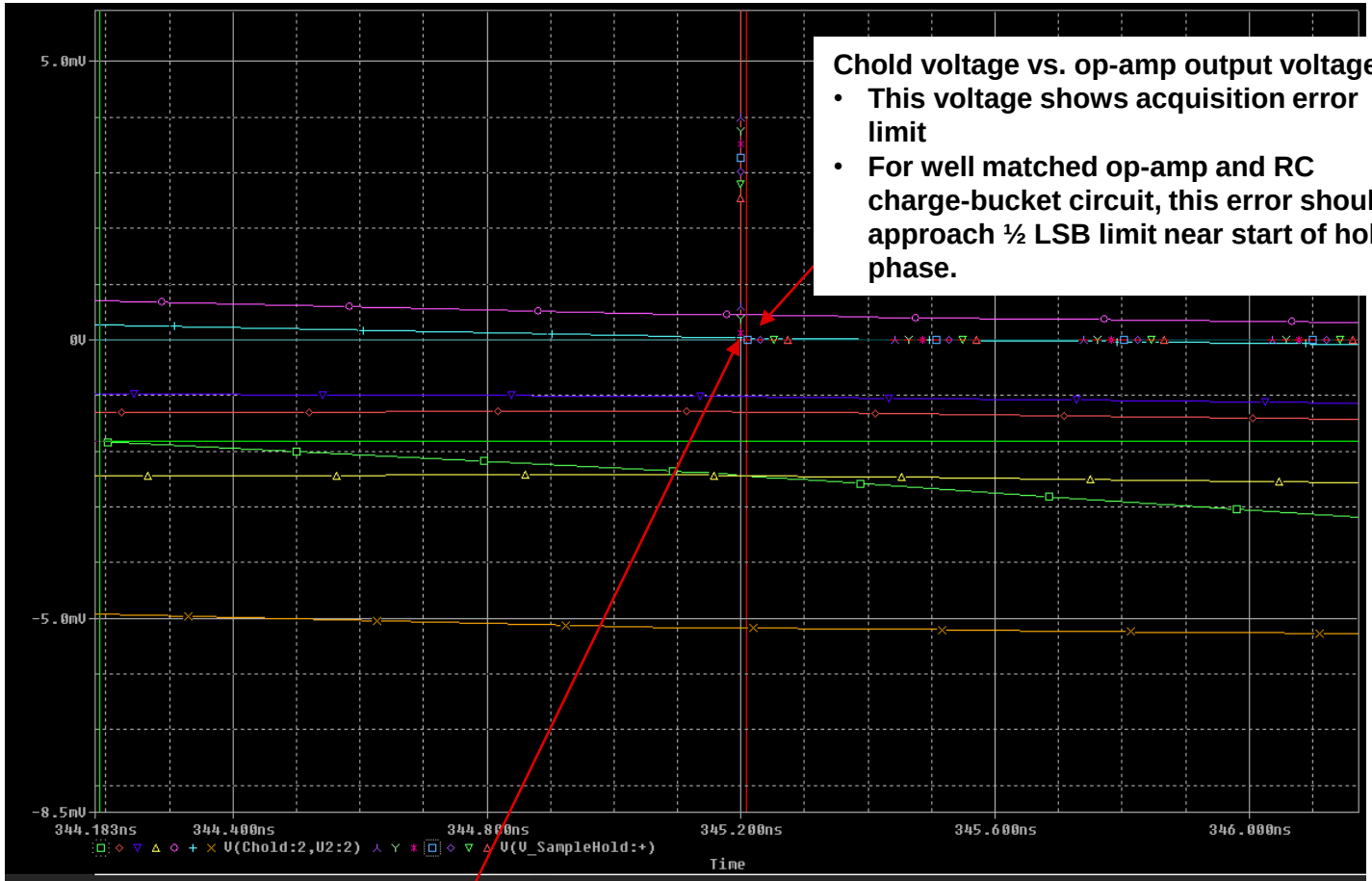
Model Output Example

- Simulated ADC settling error can be evaluated by measuring the difference in voltage from op-amp output to the Chold capacitor after the sample and hold switch has opened.
  - This would be the beginning of the conversion phase
- In the example shown, the settled acquisition error is show to be close to 1mV (no RC charge-bucket circuit optimizations were made)
- If further reduction in settled error is needed a parametric sweep of Rs and Cs values van be run



Model Output Example – Parametric Sweep

- For best value sweep starting points See SAR ADC circuit selection guide (applicable to AM263x devices) available here:
  - https://www.ti.com/lit/an/spract6a/spract6a.pdf
- Keeping Cs constant at 200pF and sweeping across Rs values from 1mOhm to 100Ohm
  - Rs = 80 minimized error after sample and hold switch closed to less than 33uV
- Specific RC values are dependent on op-amp driver and timing selected since both with change the settling behavior during sample phase



Chold voltage vs. op-amp output voltage
- **This voltage shows acquisition error limit**
- **For well matched op-amp and RC charge-bucket circuit, this error should approach ½ LSB limit near start of hold phase.**

Trace Color	Trace Name	Y1	Y2	Y1 - Y2	Y1(Cursor1) - Y2(Cursor2)		1.8194m		
	X Values	345.209n	344.190n	1.0191n	Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
CURSOR 2	V(Chold:2,U2:2)	-2.4393m	-1.8194m	-619.870u	-2.4393m	0.000	-1.8194m	-2.4393m	-2.1293m
	V(Chold:2,U2:2)	-1.2937m	-1.2947m	979.481n	-1.2937m	524.689u	-1.2937m	-1.2947m	-1.2942m
	V(Chold:2,U2:2)	-1.0181m	-971.957u	-46.114u	-1.0181m	847.443u	-971.957u	-1.0181m	-0.9950m
	V(Chold:2,U2:2)	-2.4363m	-2.4401m	3.7822u	-2.4363m	-620.701u	-2.4363m	-2.4401m	-2.4382m
	V(Chold:2,U2:2)	449.908u	711.104u	-261.196u	449.908u	2.5305m	711.104u	449.908u	580.506u
	V(Chold:2,U2:2)	33.358u	264.522u	-231.165u	33.358u	2.0839m	264.522u	33.358u	148.940u
	V(Chold:2,U2:2)	-5.1706m	-4.9158m	-254.809u	-5.1706m	-3.0964m	-4.9158m	-5.1706m	-5.0432m
	V(V_SampleHold:+)	0.000	1.2000	1.2000	0.000	1.2018	1.2000	0.000	600.000m