# Header File Value:

**0x01010101**

## 1 EMIF_CTLCFG_DENALI_PI_199 Register (Offset = 231Ch) [reset = 0h]

Return to Summary Table

**Table 14-14374. Instance Table**

| Instance Name | Physical Address |
|---|---|
| DDR16SS0 | 0F30 A31Ch |

**Figure 14-4752. EMIF_CTLCFG_DENALI_PI_199 Name Register**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | PI_TMRZ_F0 | | | | |
| NONE | | | R/W | | | | 1 |
| 0h | | | 0h | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | PI_CALVL_EN_F2 | |
| NONE | | | | | | R/W | 1 |
| 0h | | | | | | 0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | PI_CALVL_EN_F1 | |
| NONE | | | | | | R/W | 1 |
| 0h | | | | | | 0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | PI_CALVL_EN_F0 | |
| NONE | | | | | | R/W | 1 |
| 0h | | | | | | 0h | |

**Table 14-14376. EMIF_CTLCFG_DENALI_PI_199 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 31:29 | RESERVED | NONE | 0h | Reserved |
| 28:24 | PI_TMRZ_F0 | R/W | 0h | Defines the delay between a MRW CA exit command and the DQ tristate in memory clocks for frequency set 0.<br>Reset Source: ctl_amod_g_rst_n |
| 23:18 | RESERVED | NONE | 0h | Reserved |
| 17:16 | PI_CALVL_EN_F2 | R/W | 0h | Enable the PI CA training module. Bit[1] represents the support when non-initialization for frequency set 2. Bit[0]represents the support when initialization. Set to 1 to enable.<br>Reset Source: ctl_amod_g_rst_n |
| 15:10 | RESERVED | NONE | 0h | Reserved |
| 9:8 | PI_CALVL_EN_F1 | R/W | 0h | Enable the PI CA training module. Bit[1] represents the support when non-initialization for frequency set 1. Bit[0]represents the support when initialization. Set to 1 to enable.<br>Reset Source: ctl_amod_g_rst_n |
| 7:2 | RESERVED | NONE | 0h | Reserved |
| 1:0 | PI_CALVL_EN_F0 | R/W | 0h | Enable the PI CA training module. Bit[1] represents the support when non-initialization for frequency set 0. Bit[0]represents the support when initialization. Set to 1 to enable.<br>Reset Source: ctl_amod_g_rst_n |

## Header File Value:

**0x321E3200**

### 1 EMIF_CTLCFG_DENALI_PI_207 Register (Offset = 233Ch) [reset = 0h]

Return to Summary Table

**Table 14-14398. Instance Table**

| Instance Name | Physical Address |
|---|---|
| DDR16SS0 | 0F30 A33Ch |

**Figure 14-4760. EMIF_CTLCFG_DENALI_PI_207 Name Register**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| RESERVED | PI_CALVL_VREF_INITIAL_STOP_POINT_F1 | | | | | | |
| NONE | R/W | | | | | | |
| 0h | 0h | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | PI_CALVL_VREF_INITIAL_START_POINT_F1 | | | | | | |
| NONE | R/W | | | | | | |
| 0h | 0h | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | PI_CALVL_VREF_INITIAL_STOP_POINT_F0 | | | | | | |
| NONE | R/W | | | | | | |
| 0h | 0h | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | PI_CALVL_VREF_INITIAL_START_POINT_F0 | | | | | | |
| NONE | R/W | | | | | | |
| 0h | 0h | | | | | | |

50 30 50 0

**Table 14-14400. EMIF_CTLCFG_DENALI_PI_207 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 31 | RESERVED | NONE | 0h | Reserved |
| 30:24 | PI_CALVL_VREF_INITIAL_STOP_POINT_F1 | R/W | 0h | The end point of initial training for the Vref[ca] training for frequency set 1 { vrefca_range, vref_ca_setting[5:0]}.<br>Reset Source: ctl_amod_g_rst_n |
| 23 | RESERVED | NONE | 0h | Reserved |
| 22:16 | PI_CALVL_VREF_INITIAL_START_POINT_F1 | R/W | 0h | The start point of initial training for the Vref[ca] training for frequency set 1 { vrefca_range, vref_ca_setting[5:0]}.<br>Reset Source: ctl_amod_g_rst_n |
| 15 | RESERVED | NONE | 0h | Reserved |
| 14:8 | PI_CALVL_VREF_INITIAL_STOP_POINT_F0 | R/W | 0h | The end point of initial training for the Vref[ca] training for frequency set 0 { vrefca_range, vref_ca_setting[5:0]}.<br>Reset Source: ctl_amod_g_rst_n |
| 7 | RESERVED | NONE | 0h | Reserved |
| 6:0 | PI_CALVL_VREF_INITIAL_START_POINT_F0 | R/W | 0h | The start point of initial training for the Vref[ca] training for frequency set 0 { vrefca_range, vref_ca_setting[5:0]}.<br>Reset Source: ctl_amod_g_rst_n |

# Header File Value:

**0x0101321E**

## 1 EMIF_CTLCFG_DENALI_PI_208 Register (Offset = 2340h) [reset = 0h]

Return to Summary Table

**Table 14-14401. Instance Table**

| Instance Name | Physical Address |
|---|---|
| DDR16SS0 | 0F30 A340h |

**Figure 14-4761. EMIF_CTLCFG_DENALI_PI_208 Name Register**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | PI_CALVL_VREF_DELTA_F1 | | | |
| NONE | | | | R/W | | | |
| 0h | | | | 0h | | | 1 |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | PI_CALVL_VREF_DELTA_F0 | | | |
| NONE | | | | R/W | | | |
| 0h | | | | 0h | | | 1 |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | PI_CALVL_VREF_INITIAL_STOP_POINT_F2 | | | | | | |
| NONE | R/W | | | | | | |
| 0h | 0h | | | | | | 50 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | PI_CALVL_VREF_INITIAL_START_POINT_F2 | | | | | | |
| NONE | R/W | | | | | | |
| 0h | 0h | | | | | | 30 |

**Table 14-14403. EMIF_CTLCFG_DENALI_PI_208 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 31:28 | RESERVED | NONE | 0h | Reserved |
| 27:24 | PI_CALVL_VREF_DELTA_F1 | R/W | 0h | The delta fro the current CA vref for non-initial CA training for frequency set 1.<br>Reset Source: ctl_amod_g_rst_n |
| 23:20 | RESERVED | NONE | 0h | Reserved |
| 19:16 | PI_CALVL_VREF_DELTA_F0 | R/W | 0h | The delta fro the current CA vref for non-initial CA training for frequency set 0.<br>Reset Source: ctl_amod_g_rst_n |
| 15 | RESERVED | NONE | 0h | Reserved |
| 14:8 | PI_CALVL_VREF_INITIAL_STOP_POINT_F2 | R/W | 0h | The end point of initial training for the Vref[ca] training for frequency set 2 { vrefca_range, vref_ca_setting[5:0]}.<br>Reset Source: ctl_amod_g_rst_n |
| 7 | RESERVED | NONE | 0h | Reserved |
| 6:0 | PI_CALVL_VREF_INITIAL_START_POINT_F2 | R/W | 0h | The start point of initial training for the Vref[ca] training for frequency set 2 { vrefca_range, vref_ca_setting[5:0]}.<br>Reset Source: ctl_amod_g_rst_n |

1

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