轨道电路

发送器CPU板 原理图

文件名	ZPW.F-CPU_A.dsn		
版本号		发布日期	2024年6月24日
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审核		日期	
批准		日期	

CRSC 中国通号 北京全路通信信号研究设计院集团有限公司
Beijing National Railway Research & Design Institute of Signal & Communiciation Group Co., Ltd

标题 <Title>		
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修订历史

版本	描述	日期	设计者
V0.0.1	初建	2024.6.10	李自生
V0.1.0	完成项目组评审	2024.6.25	李自生

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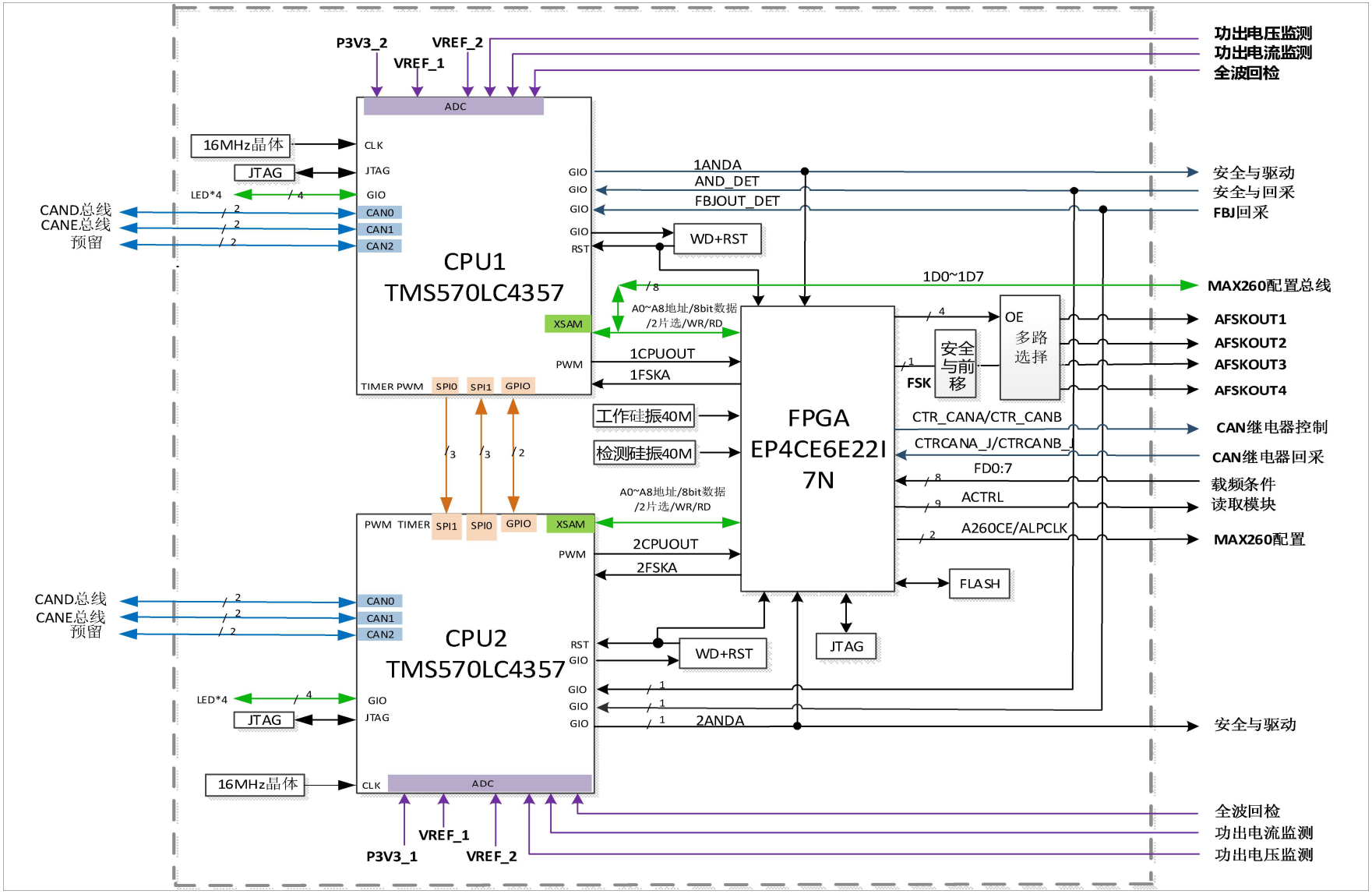

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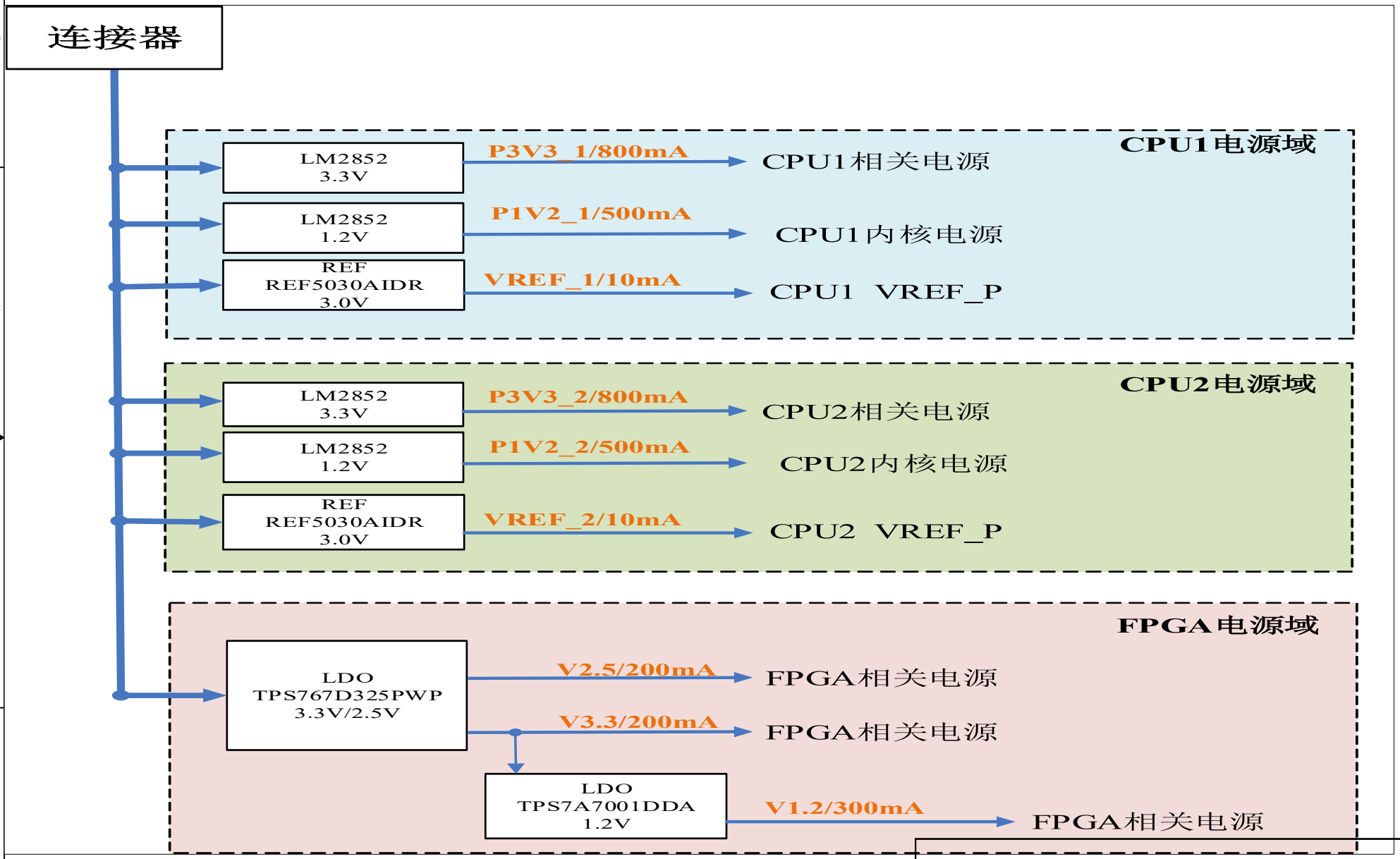

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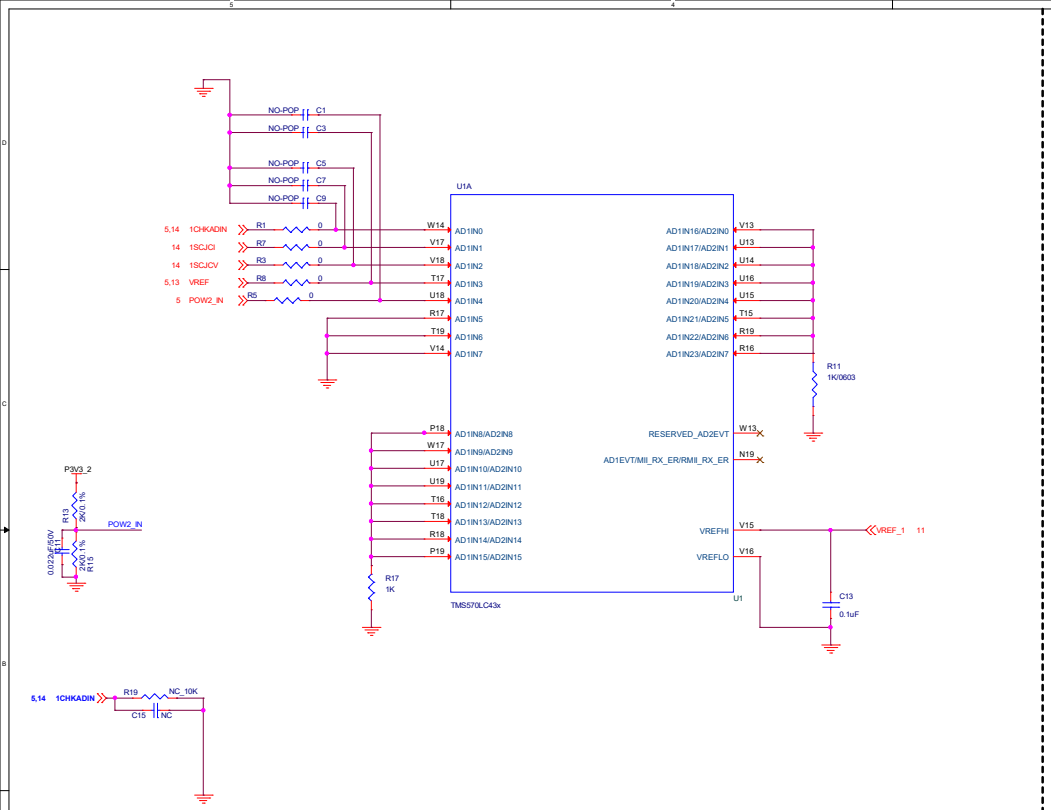

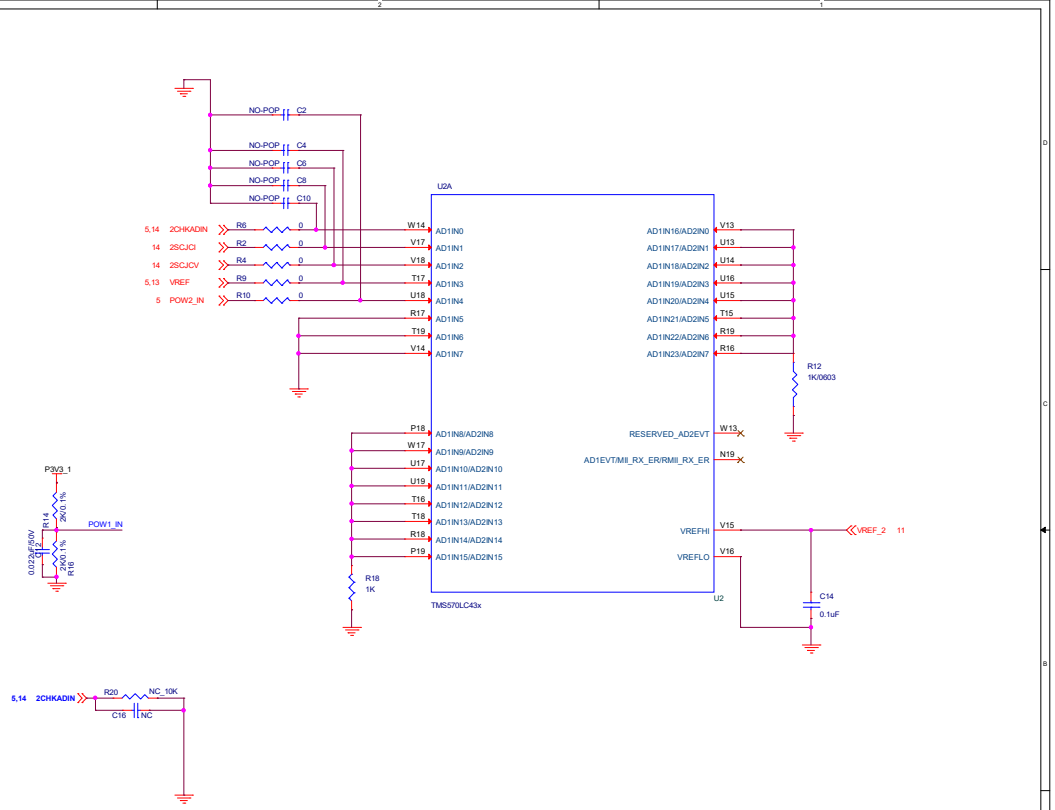

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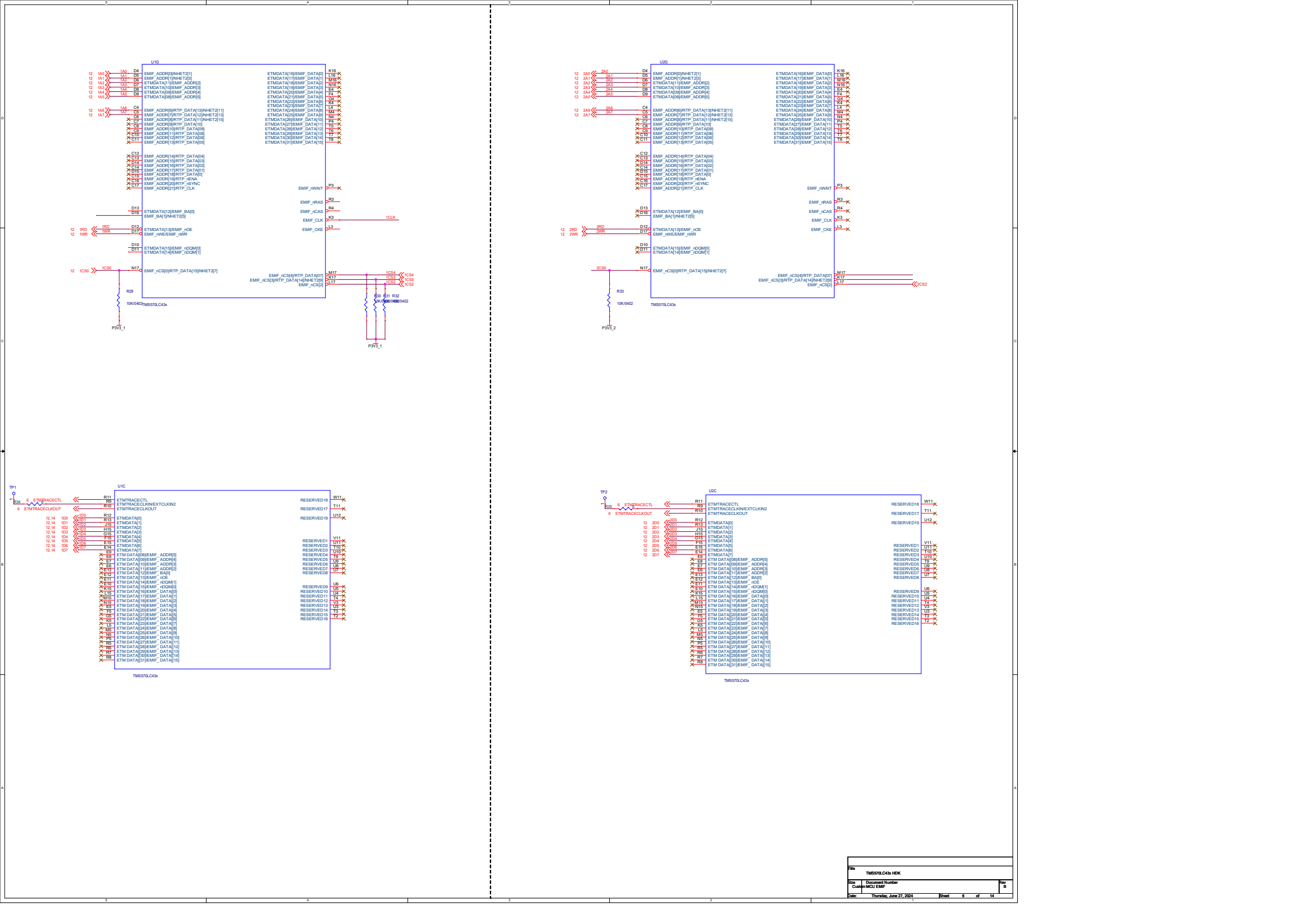
U1G
TMS570LC43x
U2G
TMS570LC43x
U1C
TMS570LC43x
U2C
TMS570LC43x
TP1
TP2
R29
R33
P3V3_1
P3V3_2
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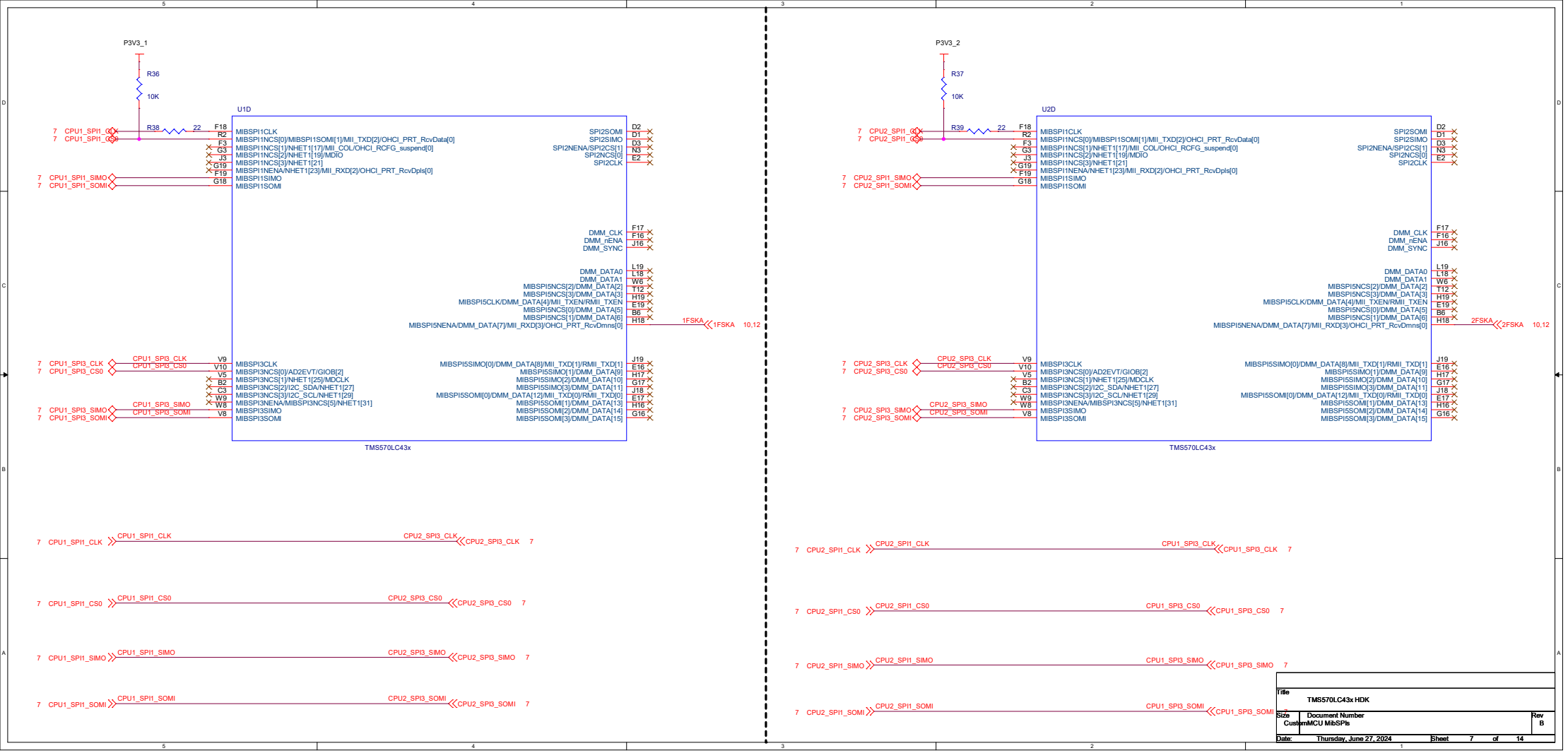
P3V3_1
R36
10K
U1D
R38
22
CPU1_SPI1_CLK
CPU1_SPI1_CS0
CPU1_SPI1_SIMO
CPU1_SPI1_SOMI
MIBSPI1CLK
MIBSPI1NCS[0]/MIBSPI1SOMI[1]/MII_TXD[2]/OHCI_PRT_RcvData[0]
MIBSPI1NCS[1]/NHET1[17]/MII_COL/OHCI_RCFG_suspend[0]
MIBSPI1NCS[2]/NHET1[19]/MDIO
MIBSPI1NCS[3]/NHET1[21]
MIBSPI1NENA/NHET1[23]/MII_RXD[2]/OHCI_PRT_RcvDpls[0]
MIBSPI1SIMO
MIBSPI1SOMI
SPI2SOMI
SPI2SIMO
SPI2NENA/SPI2CS[1]
SPI2NCS[0]
SPI2CLK
DMM_CLK
DMM_nENA
DMM_SYNC
DMM_DATA0
DMM_DATA1
MIBSPI5NCS[2]/DMM_DATA[2]
MIBSPI5NCS[3]/DMM_DATA[3]
MIBSPI5CLK/DMM_DATA[4]/MII_TXEN/RMII_TXEN
MIBSPI5NCS[0]/DMM_DATA[5]
MIBSPI5NCS[1]/DMM_DATA[6]
MIBSPI5NENA/DMM_DATA[7]/MII_RXD[3]/OHCI_PRT_RcvDmns[0]
1FSKA
10,12
CPU1_SPI3_CLK
CPU1_SPI3_CS0
CPU1_SPI3_SIMO
CPU1_SPI3_SOMI
MIBSPI3CLK
MIBSPI3NCS[0]/AD2EVT/GIOB[2]
MIBSPI3NCS[1]/NHET1[25]/MDCLK
MIBSPI3NCS[2]/I2C_SDA/NHET1[27]
MIBSPI3NCS[3]/I2C_SCL/NHET1[29]
MIBSPI3NENA/MIBSPI3NCS[5]/NHET1[31]
MIBSPI3SIMO
MIBSPI3SOMI
MIBSPI5SIMO[0]/DMM_DATA[8]/MII_TXD[1]/RMII_TXD[1]
MIBSPI5SIMO[1]/DMM_DATA[9]
MIBSPI5SIMO[2]/DMM_DATA[10]
MIBSPI5SIMO[3]/DMM_DATA[11]
MIBSPI5SOMI[0]/DMM_DATA[12]/MII_TXD[0]/RMII_TXD[0]
MIBSPI5SOMI[1]/DMM_DATA[13]
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TMS570LC43x
CPU1_SPI1_CLK
CPU2_SPI3_CLK
CPU1_SPI1_CS0
CPU2_SPI3_CS0
CPU1_SPI1_SIMO
CPU2_SPI3_SIMO
CPU1_SPI1_SOMI
CPU2_SPI3_SOMI
P3V3_2
R37
10K
U2D
R39
22
CPU2_SPI1_CLK
CPU2_SPI1_CS0
CPU2_SPI1_SIMO
CPU2_SPI1_SOMI
MIBSPI1CLK
MIBSPI1NCS[0]/MIBSPI1SOMI[1]/MII_TXD[2]/OHCI_PRT_RcvData[0]
MIBSPI1NCS[1]/NHET1[17]/MII_COL/OHCI_RCFG_suspend[0]
MIBSPI1NCS[2]/NHET1[19]/MDIO
MIBSPI1NCS[3]/NHET1[21]
MIBSPI1NENA/NHET1[23]/MII_RXD[2]/OHCI_PRT_RcvDpls[0]
MIBSPI1SIMO
MIBSPI1SOMI
SPI2SOMI
SPI2SIMO
SPI2NENA/SPI2CS[1]
SPI2NCS[0]
SPI2CLK
DMM_CLK
DMM_nENA
DMM_SYNC
DMM_DATA0
DMM_DATA1
MIBSPI5NCS[2]/DMM_DATA[2]
MIBSPI5NCS[3]/DMM_DATA[3]
MIBSPI5CLK/DMM_DATA[4]/MII_TXEN/RMII_TXEN
MIBSPI5NCS[0]/DMM_DATA[5]
MIBSPI5NCS[1]/DMM_DATA[6]
MIBSPI5NENA/DMM_DATA[7]/MII_RXD[3]/OHCI_PRT_RcvDmns[0]
2FSKA
10,12
CPU2_SPI3_CLK
CPU2_SPI3_CS0
CPU2_SPI3_SIMO
CPU2_SPI3_SOMI
MIBSPI3CLK
MIBSPI3NCS[0]/AD2EVT/GIOB[2]
MIBSPI3NCS[1]/NHET1[25]/MDCLK
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MIBSPI5SOMI[1]/DMM_DATA[13]
MIBSPI5SOMI[2]/DMM_DATA[14]
MIBSPI5SOMI[3]/DMM_DATA[15]
TMS570LC43x
CPU2_SPI1_CLK
CPU1_SPI3_CLK
CPU2_SPI1_CS0
CPU1_SPI3_CS0
CPU2_SPI1_SIMO
CPU1_SPI3_SIMO
CPU2_SPI1_SOMI
CPU1_SPI3_SOMI
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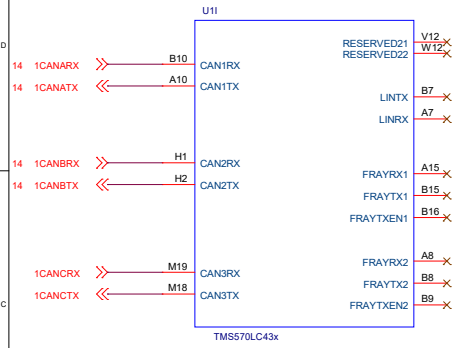

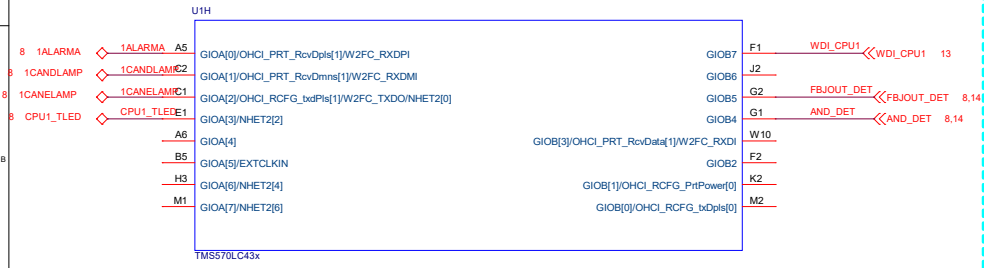

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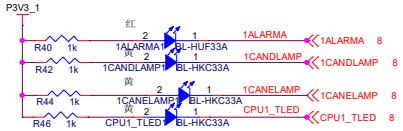
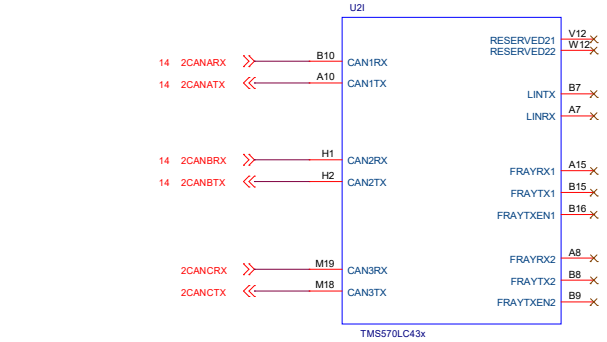
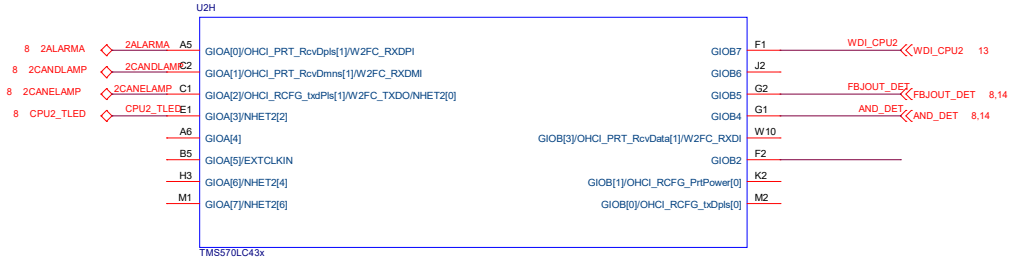
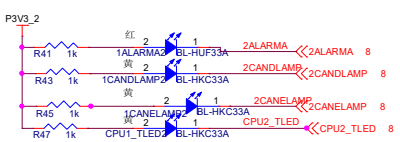






LED



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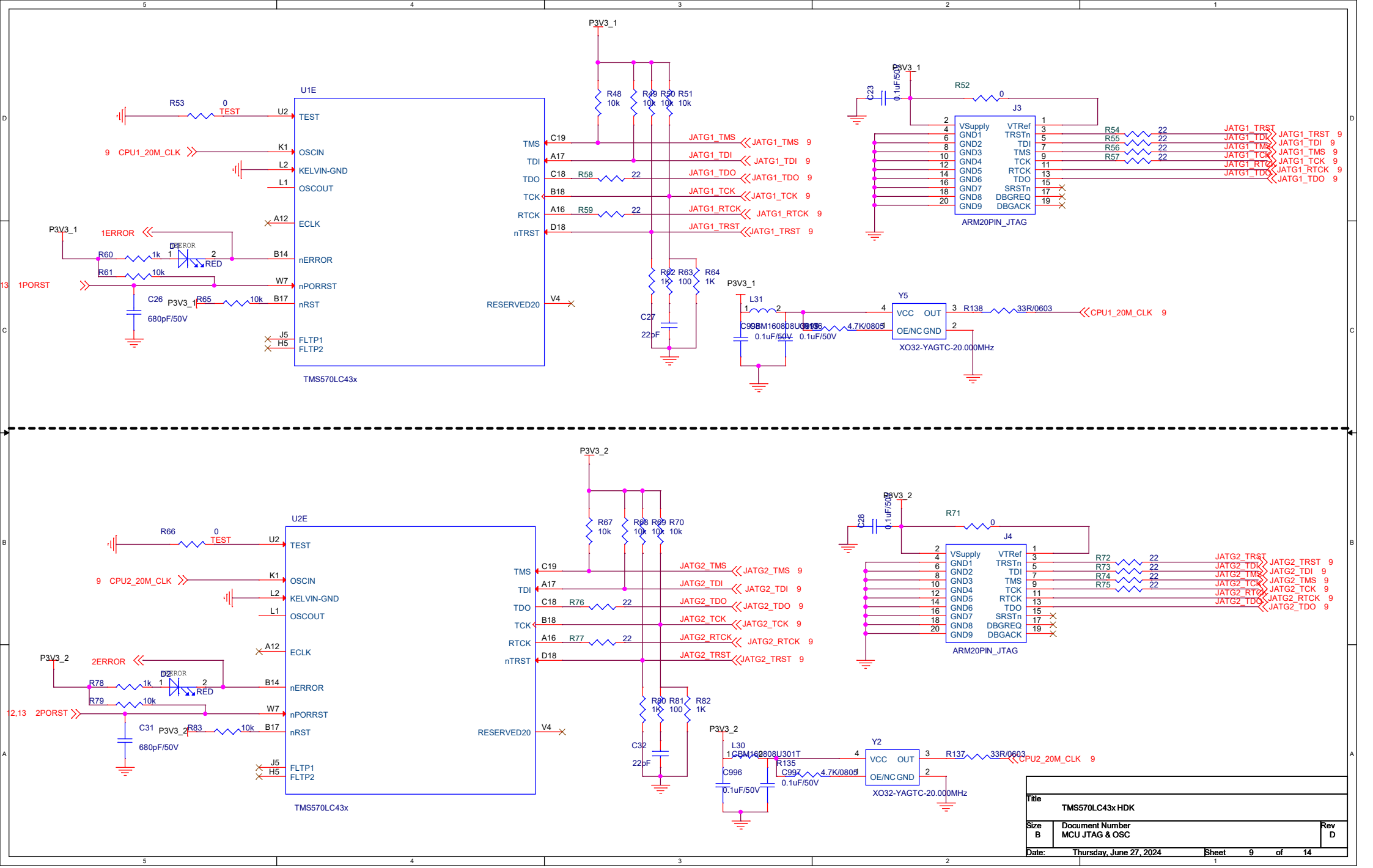

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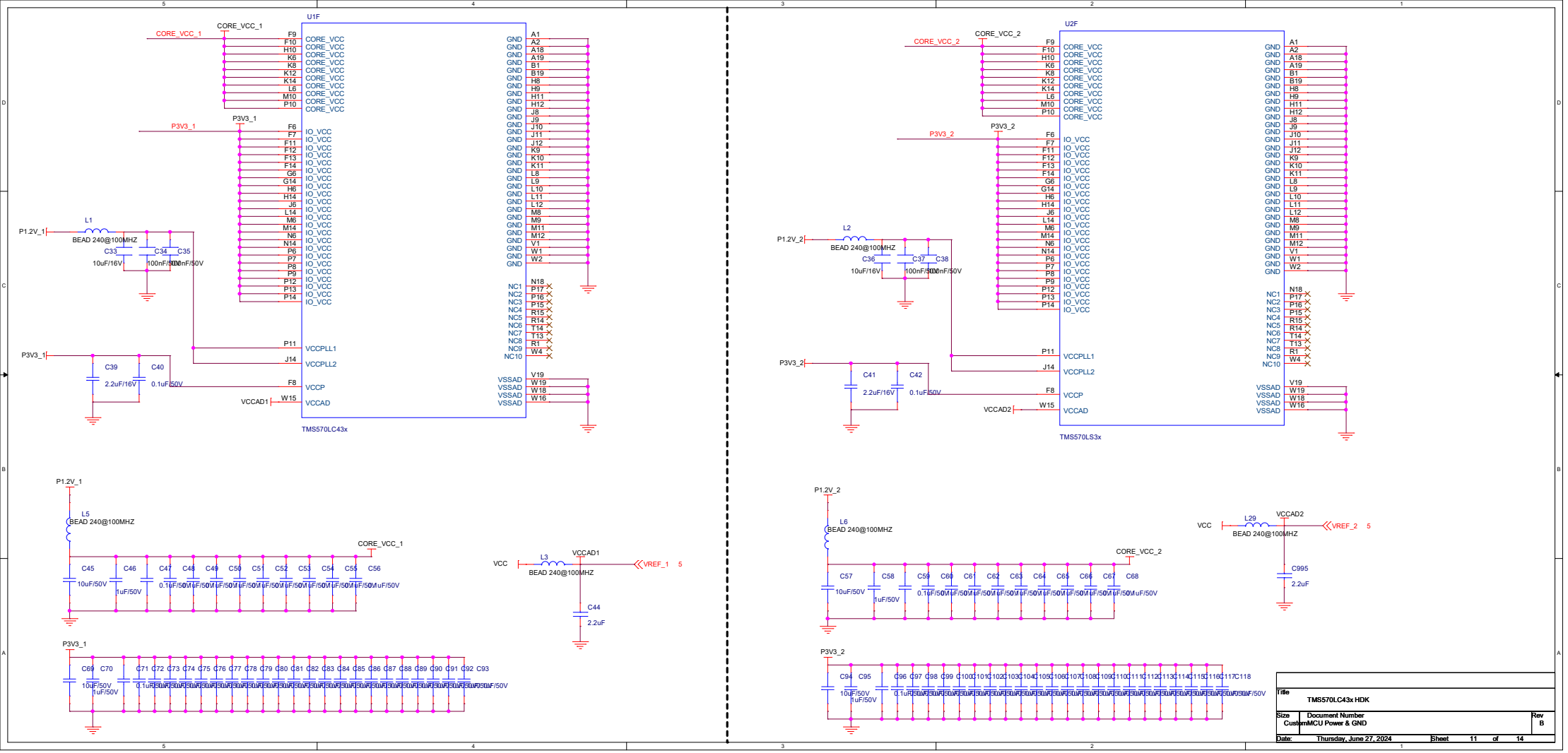
U1F
TMS570LC43x
U2F
TMS570LS3x
CORE_VCC_1
CORE_VCC_2
P3V3_1
P3V3_2
P1.2V_1
P1.2V_2
VCC
VCCAD1
VCCAD2
VREF_1 5
VREF_2 5
L1
L2
L3
L5
L6
L29
BEAD 240@100MHZ
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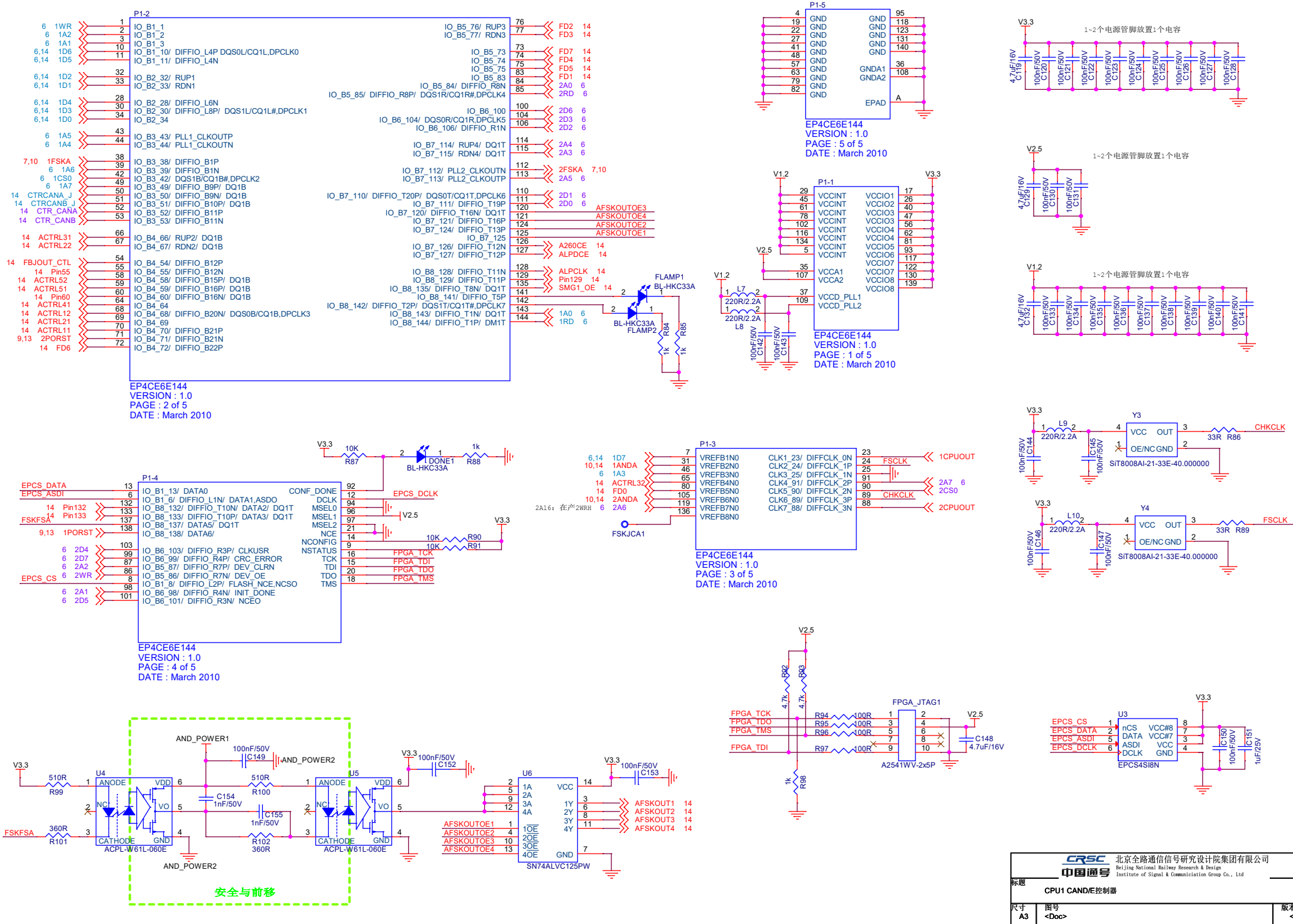
P1-2
IO_B1_1
IO_B1_2
IO_B1_3
IO_B1_10/ DIFFIO_L4P DQS0L/CQ1L,DPCLK0
IO_B1_11/ DIFFIO_L4N
IO_B2_32/ RUP1
IO_B2_33/ RDN1
IO_B2_28/ DIFFIO_L6N
IO_B2_30/ DIFFIO_L8P/ DQS1L/CQ1L#,DPCLK1
IO_B2_34
IO_B3_43/ PLL1_CLKOUTP
IO_B3_44/ PLL1_CLKOUTN
IO_B3_38/ DIFFIO_B1P
IO_B3_39/ DIFFIO_B1N
IO_B3_42/ DQS1B/CQ1B#,DPCLK2
IO_B3_49/ DIFFIO_B9P/ DQ1B
IO_B3_50/ DIFFIO_B9N/ DQ1B
IO_B3_51/ DIFFIO_B10P/ DQ1B
IO_B3_52/ DIFFIO_B11P
IO_B3_53/ DIFFIO_B11N
IO_B4_66/ RUP2/ DQ1B
IO_B4_67/ RDN2/ DQ1B
IO_B4_54/ DIFFIO_B12P
IO_B4_55/ DIFFIO_B12N
IO_B4_58/ DIFFIO_B15P/ DQ1B
IO_B4_59/ DIFFIO_B16P/ DQ1B
IO_B4_60/ DIFFIO_B16N/ DQ1B
IO_B4_64
IO_B4_68/ DIFFIO_B20N/ DQS0B/CQ1B,DPCLK3
IO_B4_69
IO_B4_70/ DIFFIO_B21P
IO_B4_71/ DIFFIO_B21N
IO_B4_72/ DIFFIO_B22P
IO_B5_76/ RUP3
IO_B5_77/ RDN3
IO_B5_73
IO_B5_74
IO_B5_75
IO_B5_83
IO_B5_84/ DIFFIO_R8N
IO_B5_85/ DIFFIO_R8P/ DQS1R/CQ1R#,DPCLK4
IO_B6_100
IO_B6_104/ DQS0R/CQ1R,DPCLK5
IO_B6_106/ DIFFIO_R1N
IO_B7_114/ RUP4/ DQ1T
IO_B7_115/ RDN4/ DQ1T
IO_B7_112/ PLL2_CLKOUTN
IO_B7_113/ PLL2_CLKOUTP
IO_B7_110/ DIFFIO_T20P/ DQS0T/CQ1T,DPCLK6
IO_B7_111/ DIFFIO_T19P
IO_B7_120/ DIFFIO_T16N/ DQ1T
IO_B7_121/ DIFFIO_T16P
IO_B7_124/ DIFFIO_T13P
IO_B7_125
IO_B7_126/ DIFFIO_T12N
IO_B7_127/ DIFFIO_T12P
IO_B8_128/ DIFFIO_T11N
IO_B8_129/ DIFFIO_T11P
IO_B8_135/ DIFFIO_T8N/ DQ1T
IO_B8_141/ DIFFIO_T5P
IO_B8_142/ DIFFIO_T2P/ DQS1T/CQ1T#,DPCLK7
IO_B8_143/ DIFFIO_T1N/ DQ1T
IO_B8_144/ DIFFIO_T1P/ DM1T
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BL-HKC33A
BL-HKC33A
FLAMP2
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GND
GNDA1
GNDA2
EPAD
EP4CE6E144
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P1-1
VCCINT
VCCA1
VCCA2
VCCD_PLL1
VCCD_PLL2
VCCIO1
VCCIO2
VCCIO3
VCCIO4
VCCIO5
VCCIO6
VCCIO7
VCCIO8
L7
L8
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P1-4
EPCS_DATA
EPCS_ASDI
EPCS_CS
IO_B1_13/ DATA0
IO_B1_6/ DIFFIO_L1N/ DATA1,ASDO
IO_B8_132/ DIFFIO_T10N/ DATA2/ DQ1T
IO_B8_133/ DIFFIO_T10P/ DATA3/ DQ1T
IO_B8_137/ DATA5/ DQ1T
IO_B8_138/ DATA6/
IO_B6_103/ DIFFIO_R3P/ CLKUSR
IO_B6_99/ DIFFIO_R4P/ CRC_ERROR
IO_B5_87/ DIFFIO_R7P/ DEV_CLRN
IO_B5_86/ DIFFIO_R7N/ DEV_OE
IO_B1_8/ DIFFIO_L2P/ FLASH_NCE,NCSO
IO_B6_98/ DIFFIO_R4N/ INIT_DONE
IO_B6_101/ DIFFIO_R3N/ NCEO
CONF_DONE
DCLK
MSEL0
MSEL1
MSEL2
NCE
NCONFIG
NSTATUS
TCK
TDI
TDO
TMS
DONE1
EPCS_DCLK
FPGA_TCK
FPGA_TDI
FPGA_TDO
FPGA_TMS
EP4CE6E144
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P1-3
VREFB1N0
VREFB2N0
VREFB3N0
VREFB4N0
VREFB5N0
VREFB6N0
VREFB7N0
VREFB8N0
CLK1_23/ DIFFCLK_0N
CLK2_24/ DIFFCLK_1P
CLK3_25/ DIFFCLK_1N
CLK4_91/ DIFFCLK_2P
CLK5_90/ DIFFCLK_2N
CLK6_89/ DIFFCLK_3P
CLK7_88/ DIFFCLK_3N
FSKJCA1
1CPUOUT
FSCLK
2A7
2CS0
CHKCLK
2CPUOUT
EP4CE6E144
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Y3
SiT8008AI-21-33E-40.000000
Y4
SiT8008AI-21-33E-40.000000
CHKCLK
FSCLK
AND_POWER1
AND_POWER2
U4
U5
ACPL-W61L-060E
U6
SN74ALVC125PW
AFSKOUTOE1
AFSKOUTOE2
AFSKOUTOE3
AFSKOUTOE4
AFSKOUT1
AFSKOUT2
AFSKOUT3
AFSKOUT4
安全与前移
FPGA_JTAG1
A2541WV-2x5P
U3
EPCS4SI8N
北京全路通信信号研究设计院集团有限公司
Beijing National Railway Research & Design Institute of Signal & Communication Group Co., Ltd
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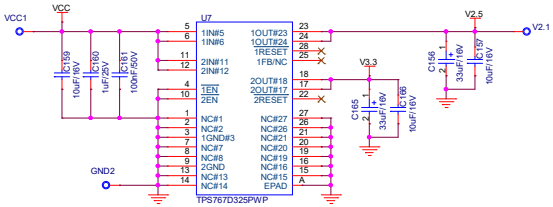
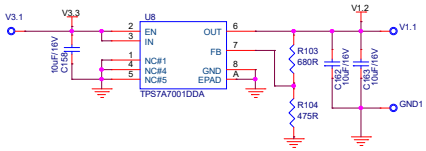
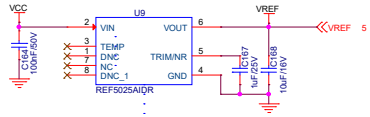
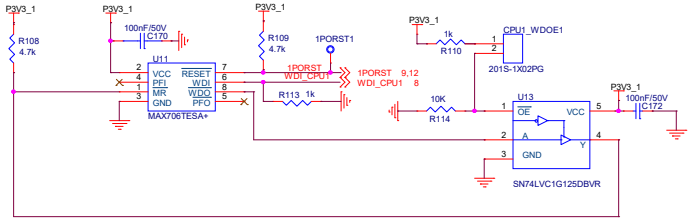


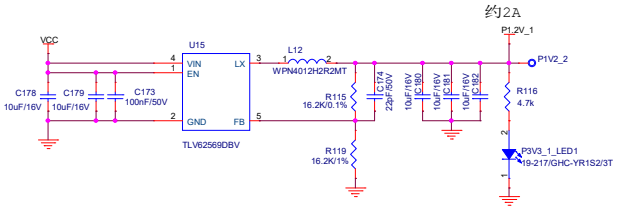


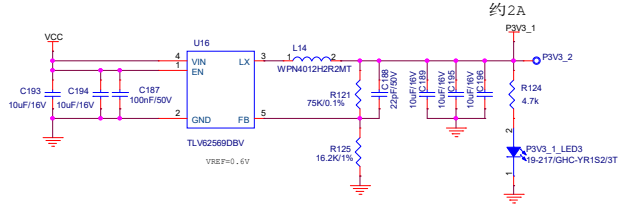
FPGA电源及参考源



CPU1参考源及复位电路







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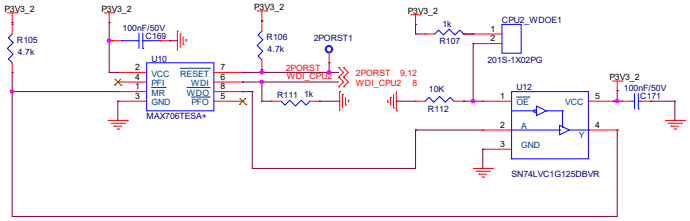

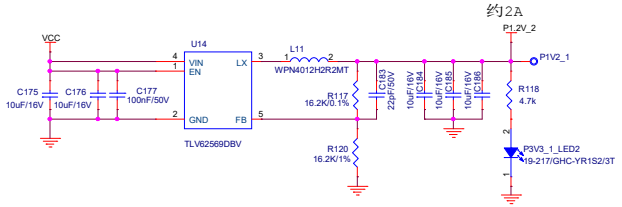

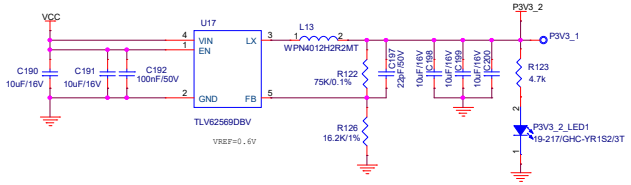

系统名称	智轨平台		
功能模块名	主控板		
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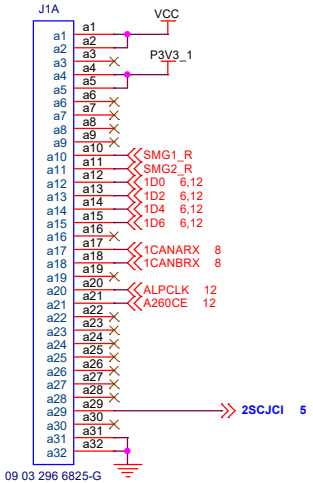
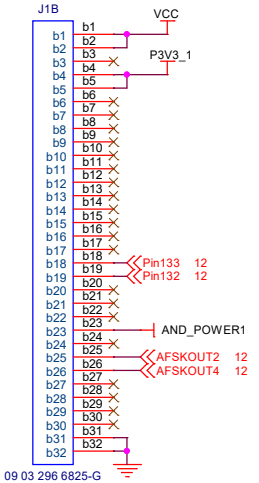
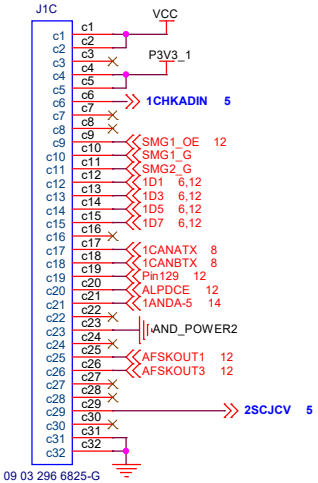
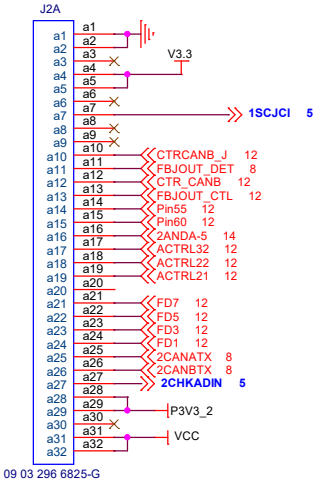
版本号	V1.0.0.0	日期	2023-05-20
设计者		页码	13 / 14
审核者		CRSC	
相关负责人			

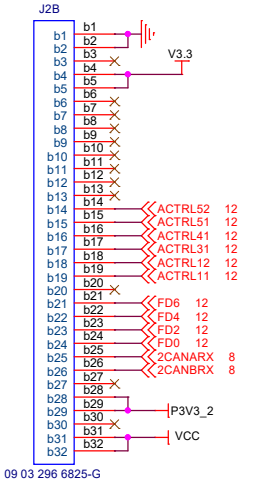


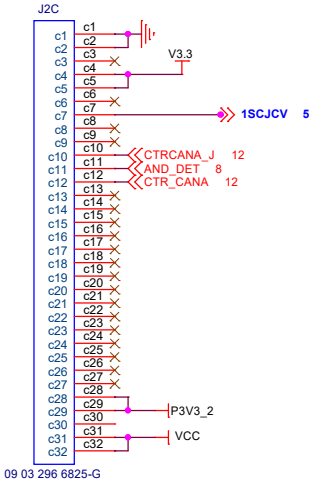




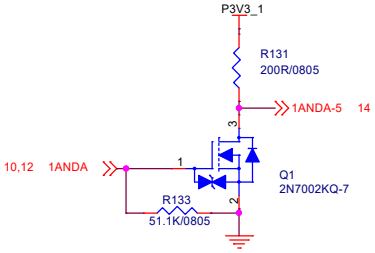
SZ板中：1SCJCV和2SCJCV是一个网络，1SCJCI和2SCJCI是一个网络

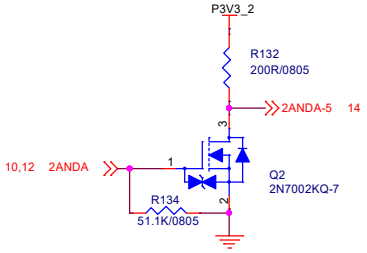






ACTRL51 52继电编码才用到





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Beijing National Railway Research & Design Institute of Signal & Communication Group Co., Ltd

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日期: Thursday, June 27, 2024	Sheet 14 of 14	