Eason Zhou *over 2 years ago in reply to Alan*

TI__Mastermind 39775 points ✓

Here is the reply from our design, Please check if you have any additional quesitons.

Source address	clock cycles without CPU access	clock cycles with CPU access at the same time	DMA Trigger type
SRAM without ECC	• 6 cycles in first dma transfer • 3 cycles there after in subsequent transfer	• 6 cycles in first dma transfer, • 3 cycles there after in subsequent transfer	software trigger
SRAM with ECC	• 6 cycles in first dma transfer, • 3 cycles there after in subsequent transfer	• 6 cycles in first dma transfer, • 3 cycles there after in subsequent transfer	software trigger
Flash (WS 2)	• 8 cycles in first dma transfer, • 5 cycles there after in subsequent transfer	• 8 extra cycles in first dma transfer, • 6 cycles there after in subsequent transfer (1 extra cycle)	software trigger