EMIF- Multiple pulses in write enable with single 16 bit data transfer

Jabir VS
192.91.66.186
Prodigy 210 points
Texas Instruments

Other Parts Discussed in Thread: HALCOGEN

Hi All,

Our customer MEDHA has finished their board design and started testing each peripheral section. At this point they are facing some issue in bringing up EMIF interface. I am stating the issue below. Please suggest an immediate solution for the same.

Customer has connected an external FRAM(parallel) device to the EMIF interface. The design is using chip select 2,3 and 4 for the external devices connected to EMIF interface(asynchronous). The word size used is 16 bit from the halcogen menu while generating the code. After this they are trying to send a 16 bit data to the external device. We were able to see one cycle of chip select signal for the corresponding single memory area access. But total three write enable pulses on the WE line are visible for the same single chip enable cycle. Same time we are observing the BA0 and BA1 signals are automatically incrementing to the higher addresses.

Please let me know why this behavior and what we need to do to resolve this.

Thanks and Regards

-Jabir

over 10 years ago

Offline Sunil Oak 10.1.1.212 over 10 years ago

TI__Mastermind 49120 points

Jabir,

I answered this question in a separate email thread.

Regards,
Sunil

From: Jabir VS [mailto:bounce-1811316@e2e.ti.com]
Sent: Monday, July 01, 2013 10:40 AM
To: tms570_internal@e2e.ti.com
Subject: [INT - Internal Hercules Forum] EMIF- Multiple pulses in write enable with single 16 bit data transfer

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Thanks and Regards

-Jabir

Young Hu 192.163.20.232 over 8 years ago in reply to Sunil Oak TI__Expert 4185 points

Hi Sunil,
My customer is facing the same issue, would you kindly send the answer to me? My Email address is young-hu@ti.com.
Thanks a lot.

BR,
Young

Offline Sunil Oak 73.32.209.238 over 8 years ago in reply to Young Hu TI__Mastermind 49120 points

Configure the external memory range as strongly-ordered or device-type using the MPU.

Previewing Staged Changes