

Industry Council on ESD Target Levels

System Level ESD



Outline

- Background to the Problem
- Objectives of White Paper 3
- Content and Structure
- “System Efficient ESD Design”
- Highlights of White Paper 3 Part I
- Conclusions
- Plans for Part II
- Some common questions

Industry Wide Problem

There is a prevailing misunderstanding between the IC Suppliers and System Level Designers regarding:

- ESD test specification requirements of system vs. component providers;
- Understanding of the ESD failure / upset mechanisms and contributions to those mechanisms, from system specific vs. component specific constraints;
- Lack of acknowledged responsibility between system designers and component providers regarding proper system level ESD protection for their respective end products.

Why is the Industry Council addressing Non-Correlation issues between Device Level and System Level testing?

Answer:

- **The common misconception that higher than necessary component ESD levels will yield higher levels of system level ESD robustness is hindering efforts to properly address system level protection design.**
- **Component ESD protection circuits are not designed to protect from system level events.**
- **However, component protection circuits can work synergistically with system protection products if properly understood and integrated into a comprehensive design**

System Level ESD

- **What is an ESD Event?**
 - Object becomes charged -> discharges to another
 - Charging levels range from 1 V to 50,000 V
 - Discharge currents range from 1A to 60 A or more
- **What is a System Level ESD Event?**
 - An electrical system experiences an ESD Event
- **What can happen in a System Level ESD Event?**
 - The system continues to work without problem
 - The system experiences upset/lockup, but no physical failure.
 - Typically referred to as “Soft Error”
 - May or may not require user intervention
 - The system experiences physical damage
 - Typically referred to as “Hard Failure”

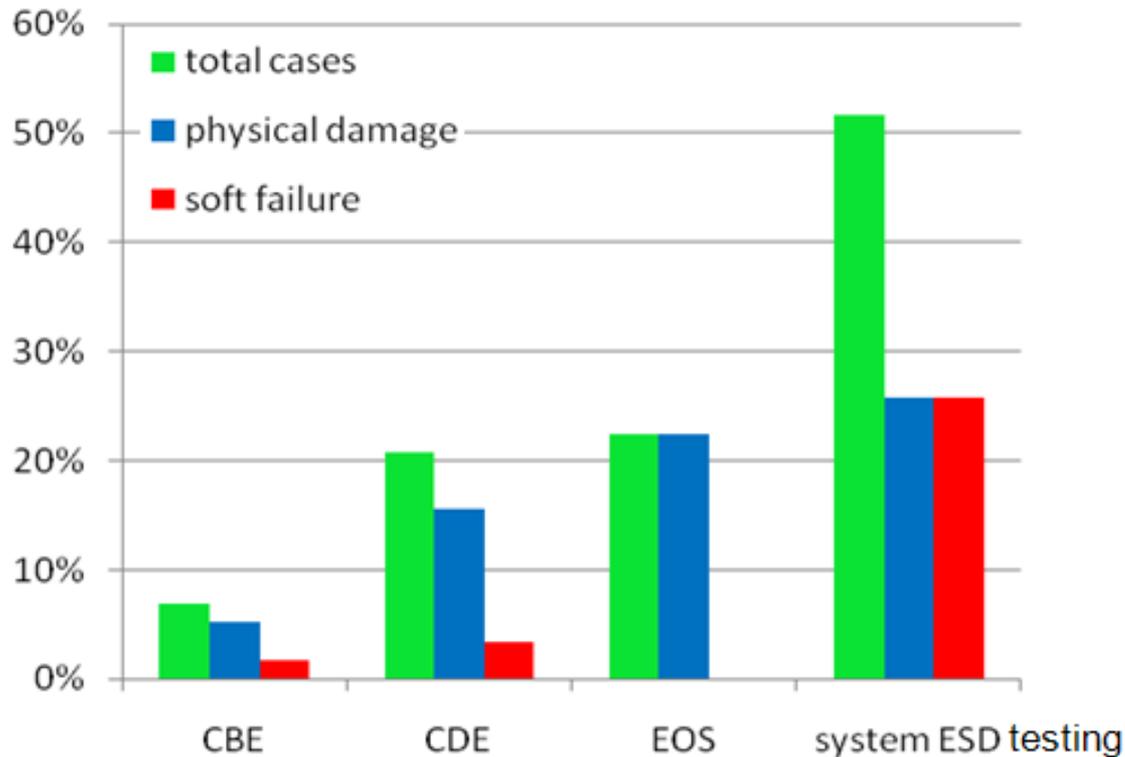
System Level ESD

- **What are some sources of System ESD Events?**
 - Charged Humans
 - Charged Humans with a Metallic Tools
 - Charged cables (Charger, Headset, USB, HDMI,..)
 - Charged Products themselves
- **How is the Event Transmitted to the System?**
 - Direct contact to a system I/O pin
 - Direct contact to a system's case
 - An arc through a vent hole or seam to a circuit board
 - Pickup of EM radiation from ESD

System Level ESD Testing

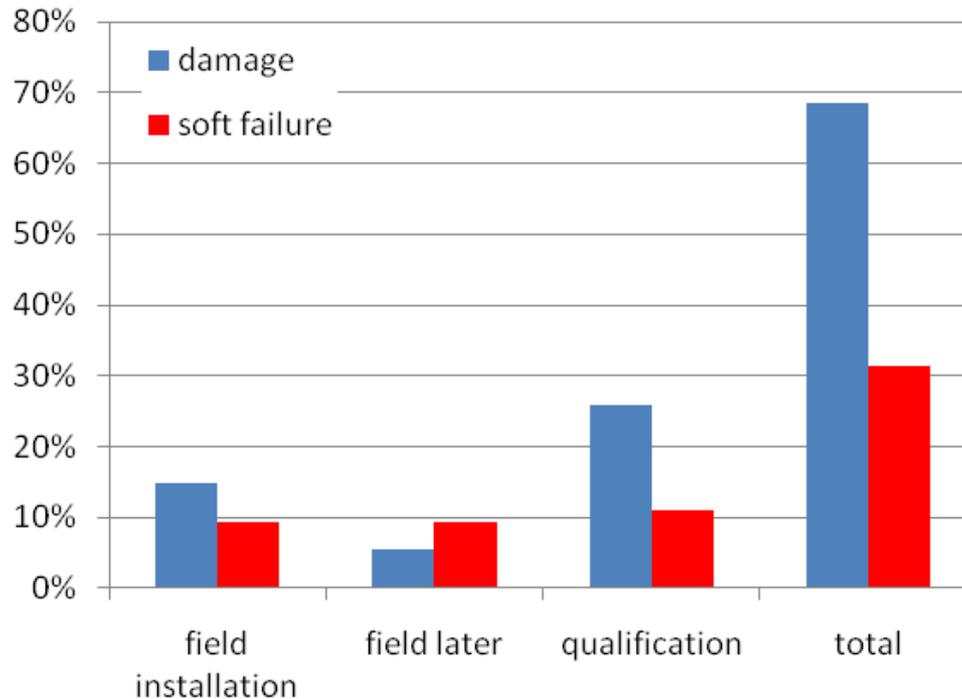
- **System level ESD (qualification) testing** is intended to ensure that finished products can continue normal operation during and after a system level ESD strike.
 - **The IEC 61000-4-2 ESD Test Method** is used to represent one particular scenario of a charged human holding a metal object to a discharge point
 - This is a common test method used to assess the ESD robustness of the system
 - Other test standards (e.g., ISO10605 for automotive, DO-160 for avionics) are used, depending on the application
- **System Level ESD Test Results**
 - Pass: System continues to work without interruption
 - Soft error that corrects on its own
 - Soft error requiring intervention (reboot, power cycle, ...)
 - Physical failure

Case Studies



- Common reported causes of system failure are:
 - Charged Board Events (CBE)
 - Cable Discharge Events (CDE)
 - Electrical Overstress (EOS)
 - IEC System Level ESD testing

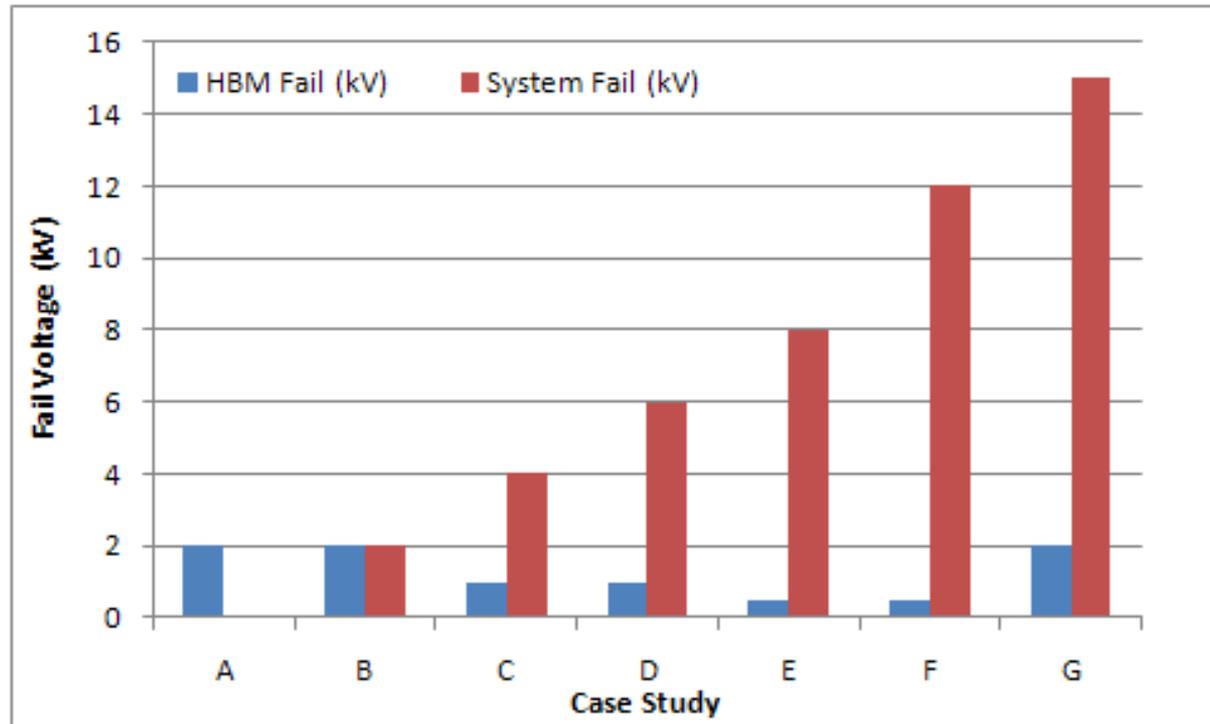
Case Studies



- Physical damage was reported more frequently in the 58 case studies tallied by the Industry Council.
- However, system manufacturers report that physical damage occurred less frequently than soft failure.
- System manufacturers do not always report soft failures to suppliers. Because most of the case studies were provided by suppliers, data tends to be weighted towards physical damage.

- *Aren't Integrated Circuits Tested for ESD?*
- Yes, they are Tested for HBM & CDM
- *Doesn't that mean they will be fine in a system?*
- No, they are tested to assure that they can survive manufacture in an controlled ESD environment
- *But won't that help?*
- No, this is a misconception. Good component ESD does not mean a system is comparably protected.

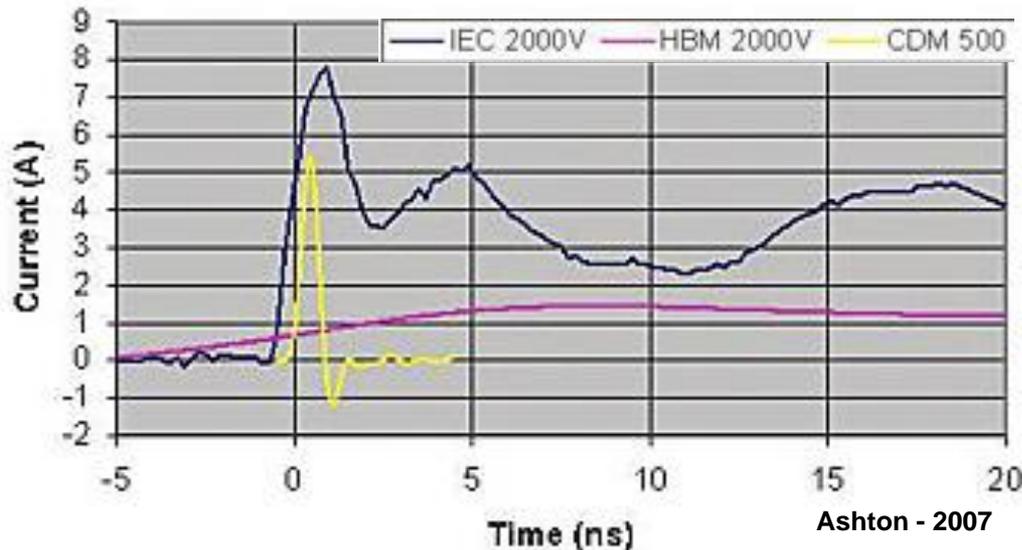
Component Vs. System Test Result Correlation



Case Study	HBM Fail (kV)	System Fail (kV)
A	2	0
B	2	2
C	1	4
D	1	6
E	0.5	8
F	0.5	12
G	2	15

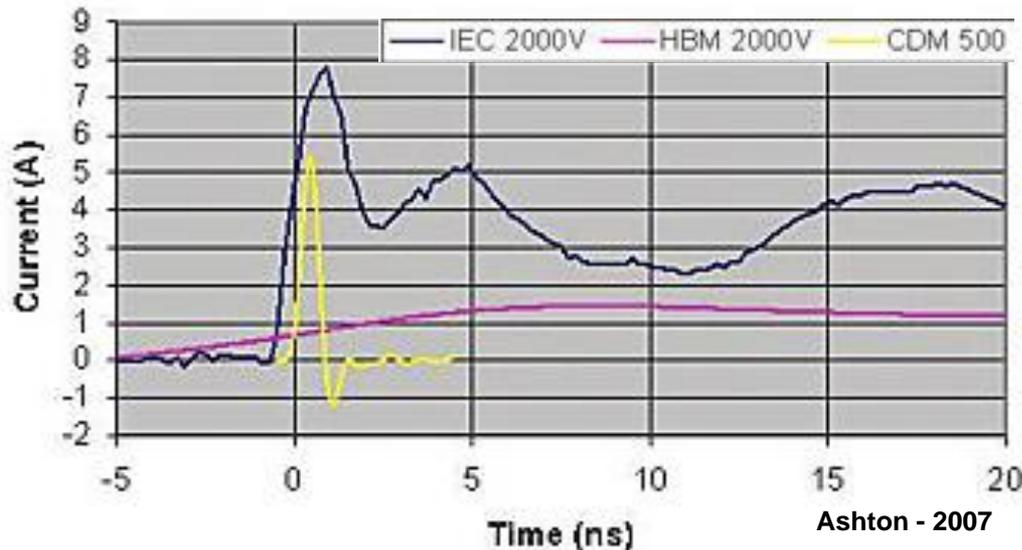
- Case studies A through G represent data on products which had failure voltages characterized for both HBM and IEC based system level test.
- Data indicates no correlation of HBM failure voltage to IEC failure voltage. Why?
- Need to understand what drives this disparity between the two test methods.

Component Vs. System ESD Comparison



- **HBM Test**: closed circuit test where the ESD pulse is applied between 2 or more pins of an unpowered part.
- **CDM Test**: charge is built up on the product and then extracted from a single pin of an unpowered part.
- **System Level Test**: a part is mounted in an application on a board and typically powered up.
 - Stress is applied between specific locations on the system and the power supply reference ground.
 - Peak currents, rise time and discharge duration differ from HBM/CDM.

Component Vs. System ESD Comparison

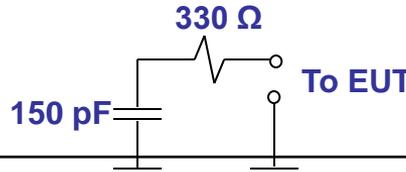
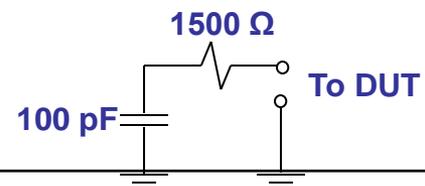


- **Pass/Fail Criteria**

- **HBM/CDM**: based on physical damage
- **System Level ESD**: based on temporary system upset and/or physical damage

➔ **The discharge paths and the associated currents will be different for these stress methods, therefore NO correlation can be expected**

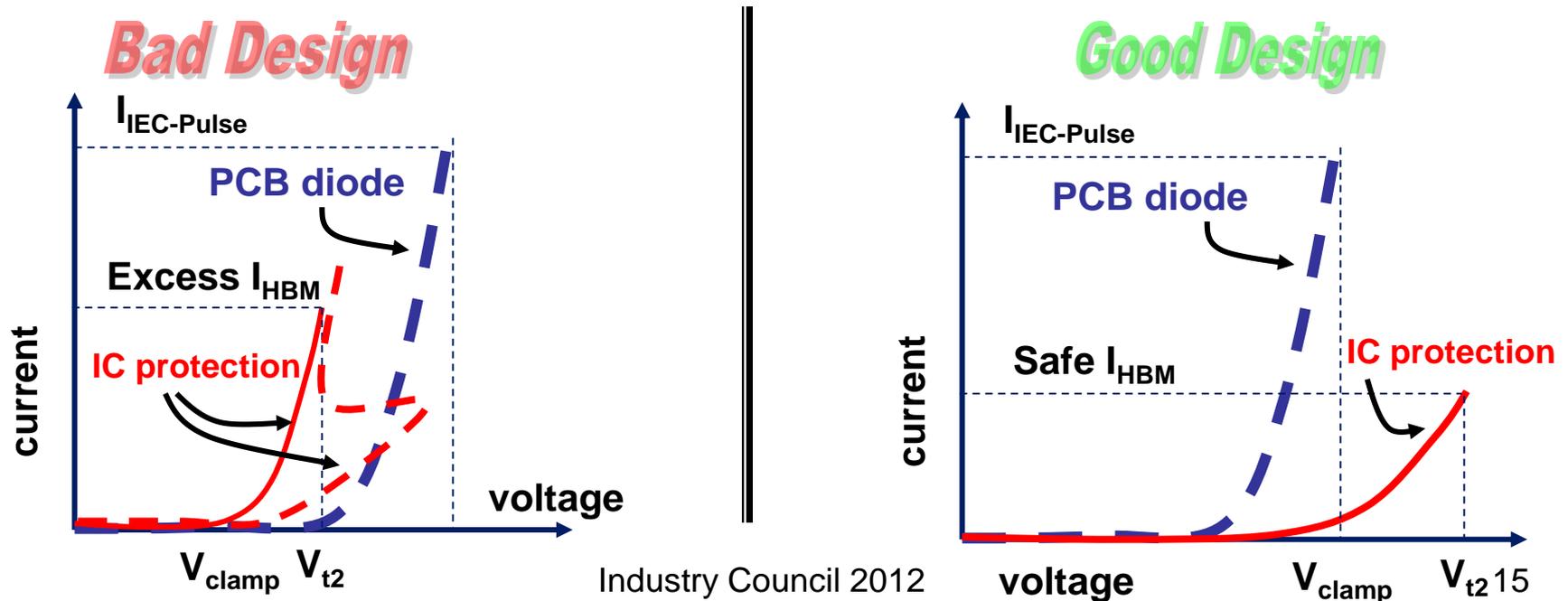
System level ESD vs. Component level ESD

Parameter	System level ESD - IEC	Component level ESD HBM
Event example	Charged human discharging through a metallic tool to a system	Charged human discharging through the skin to a component (IC)
Model	IEC system level ESD	Human Body Model (HBM)
Environment	End customer's normal operation	Factory assembly
Standard example Test	IEC 61000-4-2 (Powered) ISO 10605 (Unpowered)	JS-001-1010 (Unpowered only)
R-C network		
Peak current	3.75 A / kV	0.7 A / kV
Typical requirement	8 KV	2 KV
Rise time	0.7 ~ 1 ns	2 ~ 10 ns
Pulse width	~50 ns	150 ns
Failures	Soft and Hard	Hard
Application	PC, Cell phone, Modem, etc...	IC
Tester examples	KeyTek Minizap, Noiseken ESS2000	KeyTek Zapmaster MK2, Oryx

➔ **The two tests are distinctly different and serve different purposes**

Why would designing for higher HBM on chip not be advantageous for system protection design?

- Designing high IC HBM involves lowering the clamp triggering level and its on-resistance to reduce power dissipation on chip. But these design changes often make it harder for on board protection to be successful.



Why System and Component ESD Do Not Correlate

- Improving HBM and CDM often makes Integrated Circuits harder to Protect
- HBM & CDM circuit design assumes no power to the circuits
- HBM and CDM do not address soft failures
- HBM & CDM circuit design assumes no external components
- System level ESD robustness is affected by all components and the board design

White Paper 3 Part I

The Industry Council has addressed these issues through a white paper

- Title: **Eliminating Misconceptions in the Design of Robust ESD Systems**

Authors: IC Suppliers, Consultants, System Experts, and OEM Advisors

Key OEM Advisors / Specialist Contributors:

Tim Cheung - RIM

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John Kinnear - IBM

Frederic Lefon- Valeo

Christian Lippert - Audi

Wolfgang Pfaff – Bosch

Pasi Tamminen - Nokia

Wolfgang Wilkening - Bosch

Rick Wong - Cisco

Purpose and Objectives for WP3

- Present the first comprehensive analysis of system ESD, including analysis of ESD related system failures and design for system robustness.
- Close the existing communication gap between the OEMs and IC providers by drawing on the expertise of OEM system design experts.
- Introduce “System-Efficient ESD Design” (SEED), that promotes a common understanding of OEM and component provider system level ESD requirements.

Approach for WP3

- WP3 is being done in two phases
- Part I: Develop a framework for sharing component / system level circuit information so that best practice ESD protection and controls can be co-developed and properly shared.
- Part II: Address system level ESD using the information in Part I. This information will be used to establish recommendations for component and system level manufacturers regarding proper ESD protection / controls and best practice ESD test methods for systems.
- Part II information can be used to properly assess system ESD and EMI related performance effects of system level testing.

Contents of WP3 Part I

Topics Covered: (✓ introduced in previous slides)

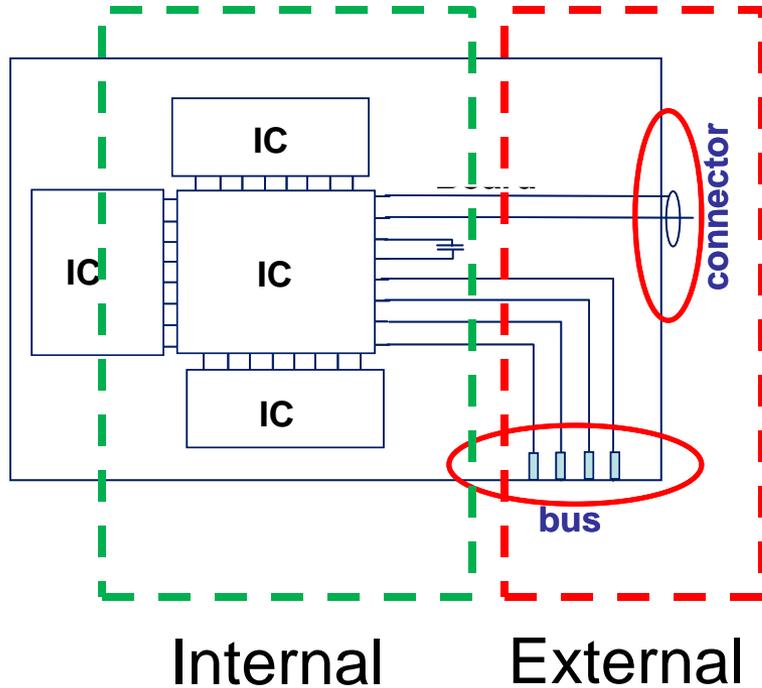
- ✓ Statement of the problem
- ✓ System ESD test methods and fields of application
- ✓ Proven System Level fails and classification of the failure statistics
- ✓ Analysis of the lack of correlation between HBM/CDM and the IEC 61000-4-2 ESD test
- Definition and classification of Internal Vs. External pins
- Identification of and practical agreement on OEM System Level needs and expectations
- Establishment of the relationship between IC Protection Design and system robustness
- Introduction of the new concept of System-Efficient ESD Design (SEED), that facilitates better co-design effort

Do all pins on a device need to be tested using system level events?

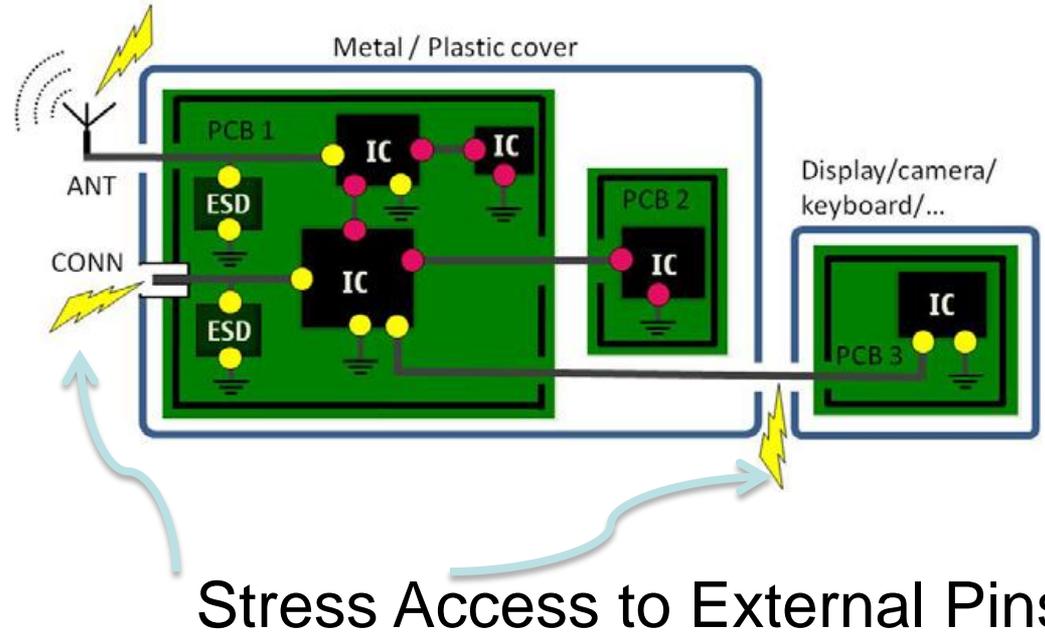
- **Only the external pins** (e.g. USB data lines, Vbus line, ID and other control lines; codec, and battery pins, etc) need to be tested if the IC is not to be protected with on board components. But if the pin is to be protected by on board components, TLP characterization of the pin is more useful.
- **Other internal ESD sensitive pins** (e.g. control pins, reset pins, and high speed data lines, etc.) can be inductively coupled during a discharge to the case and/or to an adjacent trace of an exposed pin undergoing system testing.
- These sensitive internal pins need to be identified and may need to be tested using system level events.

Differentiation of Internal Vs. External Pins

Circuit Board

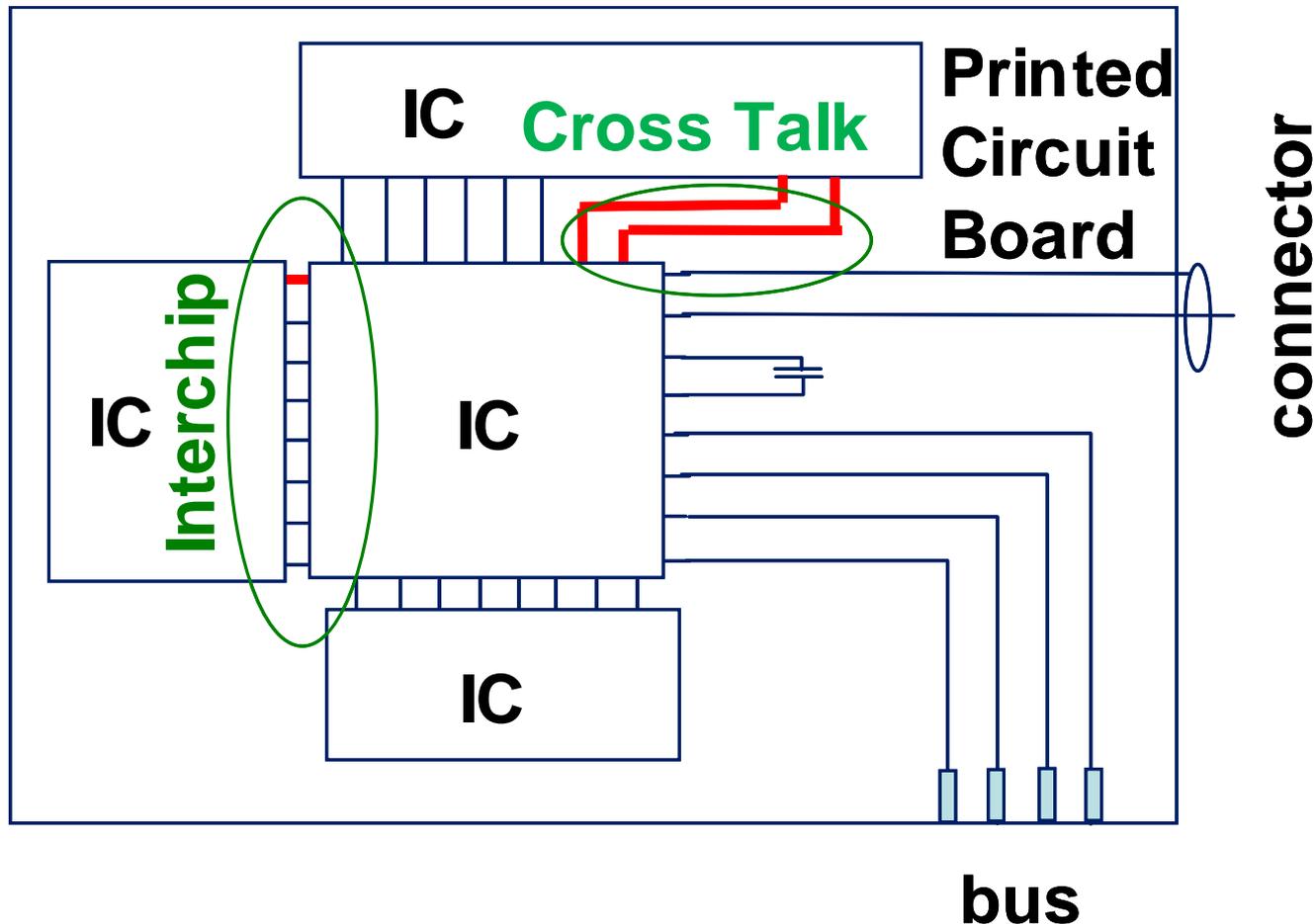


System



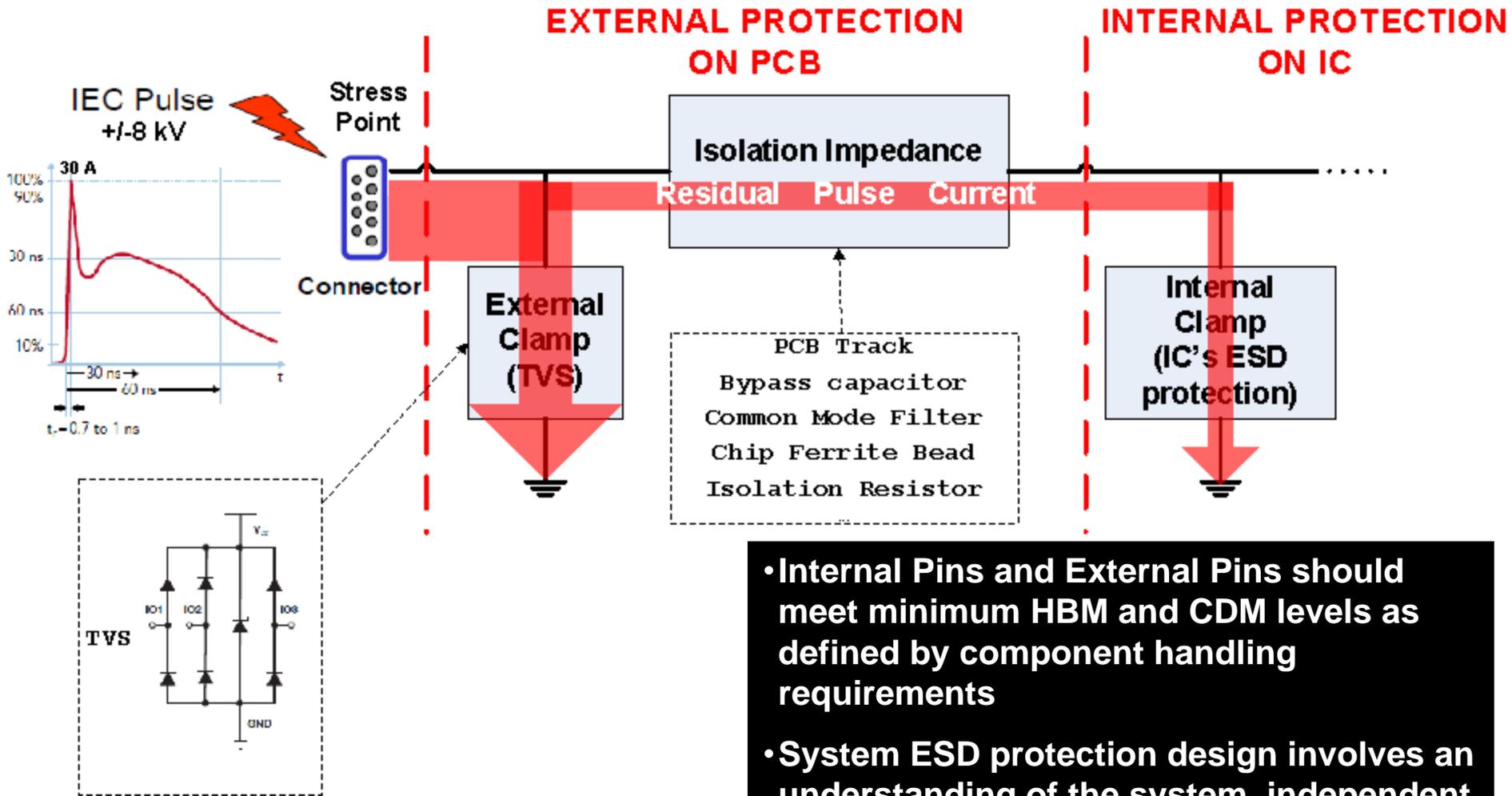
- Internal Pins and External Pins should meet minimum HBM and CDM levels as defined by component handling requirements
- But for achieving system level ESD robustness, the External Pins must be designed with a proper system protection strategy independent of their HBM/CDM protection levels

Differentiation of Internal Vs. External Pins



Other types of pins, including **Inter-chip**, and the effects of **Cross-Talk** have to be considered

Designing for the Overall System

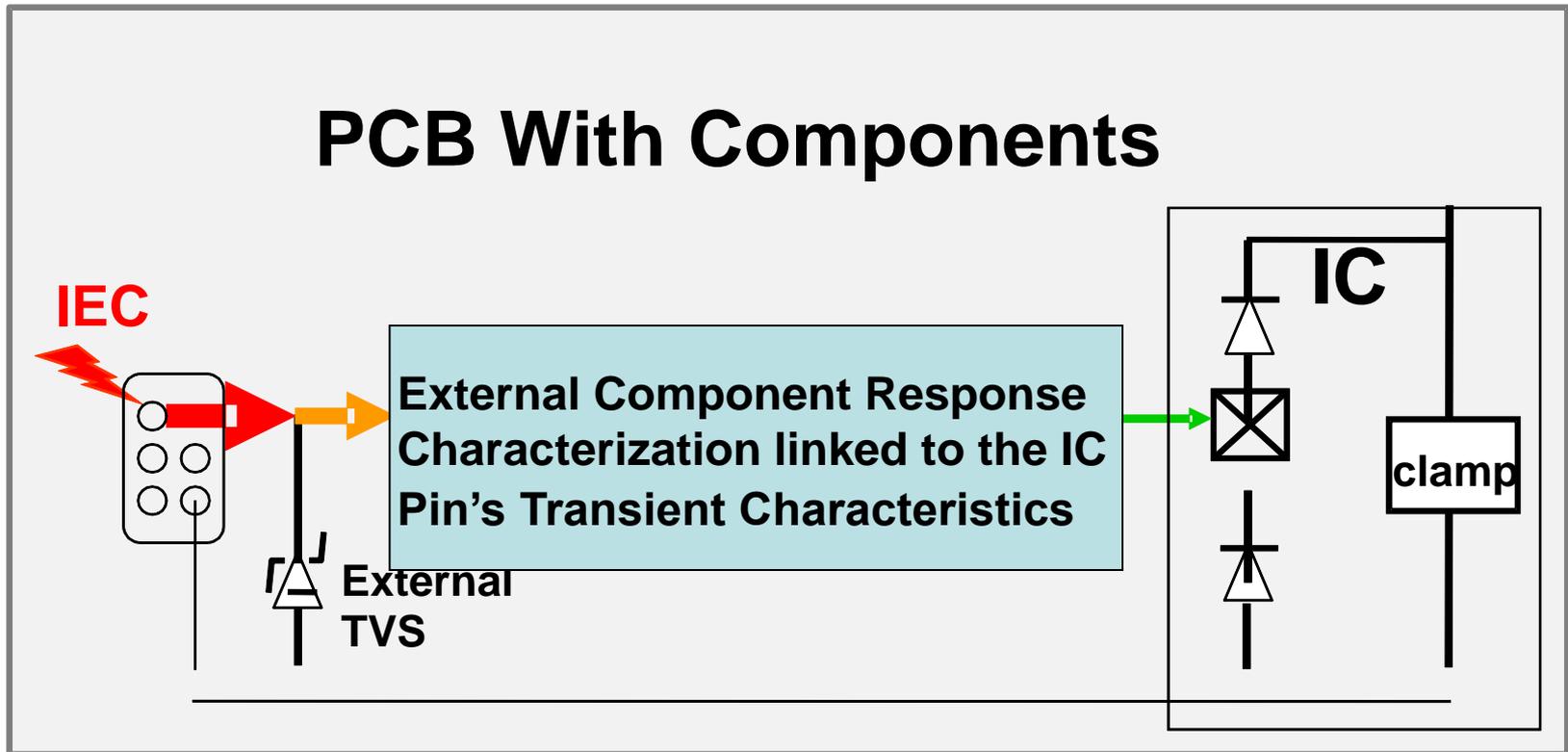


- Internal Pins and External Pins should meet minimum HBM and CDM levels as defined by component handling requirements
- System ESD protection design involves an understanding of the system, independent of component ESD levels

How can system/board designers get the required information about the IC IO behavior?

- **First, both the OEM and the IC supplier must define the ‘external pins’.**
- **Following this, the IC supplier provides the TLP curve of the pin under interest with either bias applied or without bias which would depend on the pin application in the overall system board.**
- **The measured TLP response at the pin will not only represent the pin’s internal ESD clamp behavior, but it will also include the IO design behavior to the transient pulse analysis.**

System-Efficient ESD Design (SEED) Concept



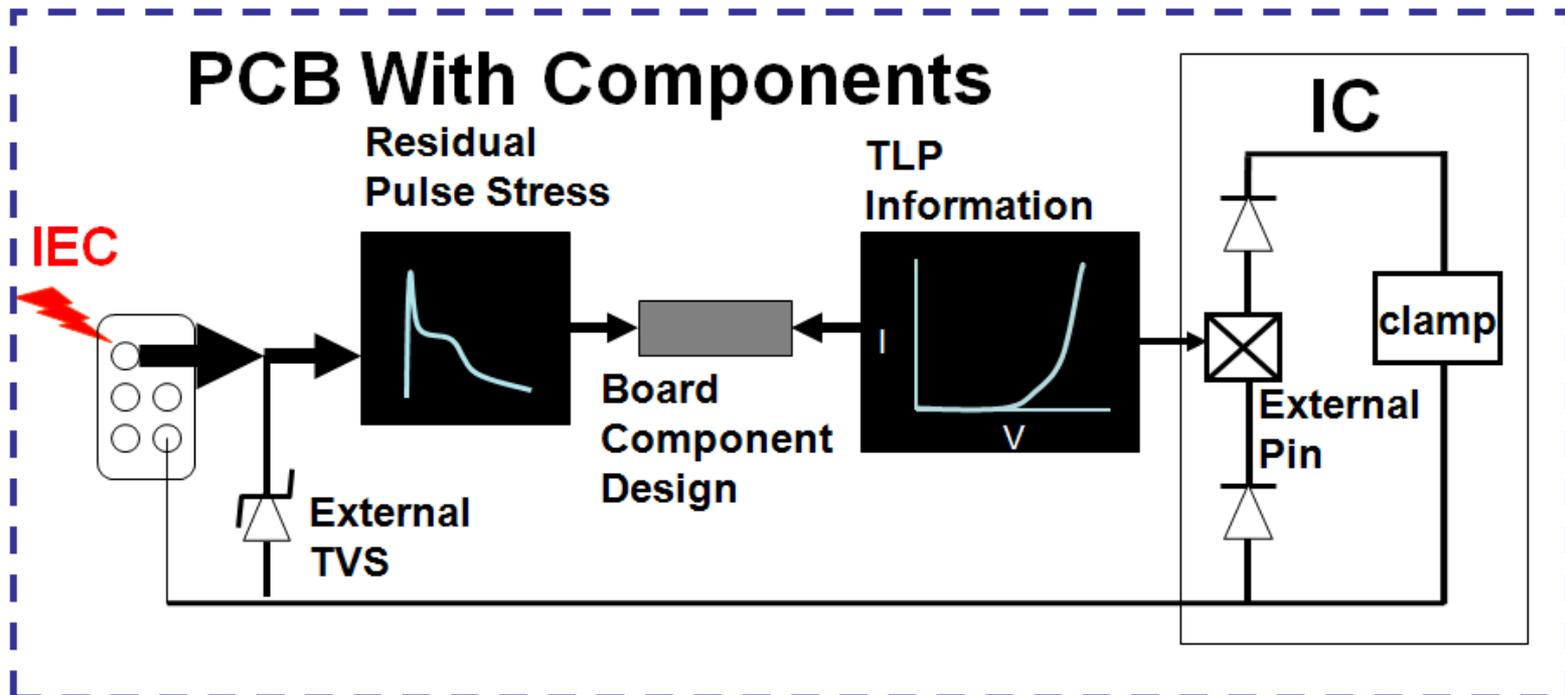
- Utilizes existing component level ESD protection as a starting point for design
- For an efficient system protection design, the IC pin's breakdown characteristics play a critical role
- Effective IEC protection design can be achieved for any IC pin that interfaces with the external world

Does SEED reproduce real, physical behavior of a board and IC?

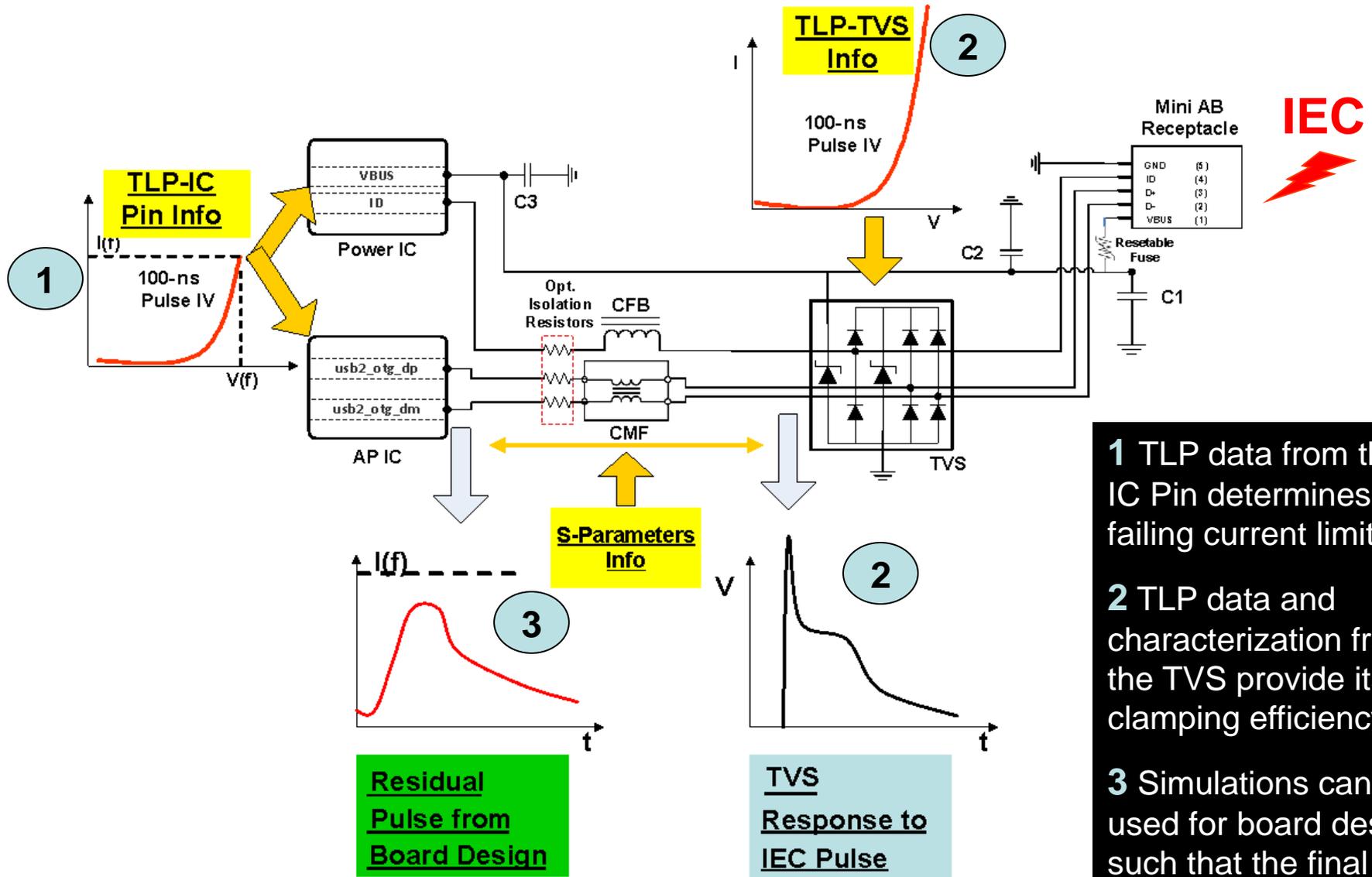
- **SEED is a design concept whose goal is to attenuate damaging current pulses before reaching the internal IC pin.**
- **So in this sense, it must first model what the physical effect would be on an IC pin resulting from an IEC stress at the external port of the PCB.**
- **What it represents for the board depends on how well the scenario is represented during the SEED analysis.**

SEED Concept: General Approach

1. IC Supplier provides Transmission Line Pulse (TLP) data on IC pin
2. Board Designer characterizes the Transient Voltage Pulse (TVP) at the bare component board interface.
3. Board protection components are adjusted to balance the RPS data to the TLP data.
4. This approach can be refined by repeating TLP on the board with the component installed. Board protection components are then readjusted.



SEED Concept: Application Example



Highlights of WP3 Part I

Summary

- ESD test specification requirements of system providers must be clearly understood
- Using component level ESD specifications as a basis to address robust system designs must be discouraged
- Understanding of system ESD failures and upset mechanisms is important
- ➔ Shared responsibility between system designers and component providers is critical

Part I Published as JEP161

- HBM and CDM specifications do not correlate to System Level ESD robustness
- Components/devices just passing a certain level of any stress type (such as IEC) does not always ensure complete system robustness
- *External vs. Internal* IC pins must be identified and understood for good system design
- Large area on-chip protection is not a good strategy for robust system ESD design
- ➔ The System-Efficient ESD Design (SEED) strategy will reduce the overall R&D effort.

Part II Approach

- System ESD can impact an entire system and can create both “hard” and “soft” failures.
- So called soft failures may involve complex EMC/EMI effects and also some Transient Latchup (TLU) phenomenon.
- Part II will establish recommendations for component and system level manufacturers regarding proper protection / controls and best practice ESD design for EMC/EMI

Part II Objectives

- **Recommendations for IC and system level manufacturers regarding proper protection, and best practice ESD system design and tests.**
- **Tests which can properly assess ESD robustness in system level tests.**
- **Recommendations that the IC manufacturer should provide to the system designer**
- **Guidance of best practices for shared responsibility between IC designer and system designer.**

Additional Q&A

Why wouldn't you expect to see correlation between device level and system level testing?

- **Since the tests are done in different environments (unpowered versus powered or stand-alone versus on board) along with the different stress current wave shapes for the two tests, it is not surprising that they would lack correlation.**
- **However when external pins are involved, a higher component level ESD on these pins could mean less load for the on-board clamp to handle. But this type of approach, while being impractical and unpredictable, also detracts from the need for an efficient system ESD design compatible with the on-board clamp.**

Is 2kV "HBM" testing the same as IEC Zap Gun testing?

- Unfortunately, there is sometimes confusion in the comparison of the two methods.
- Actual human contact to an IC component is simulated / tested with the Human Body Model Tester, which results in ESD stress between two or more component pins.
- This is completely different from the IEC Test method where the Zap Gun is used to test an IC system case, board or board connector.

Will there be a need for a device ESD target level, to confirm system level performance?

- **No. System level performance is a combination of on-chip ESD protection, on-board protection components and system mechanics design.**
- **The detailed properties of the IC's ESD protection (such as turn on voltage, resistance, and maximum withstand current) are much more important than the IC's HBM and CDM withstand level measured in voltage.**

If system level ESD testing does not guarantee system level (including component) ESD performance, aren't higher component level HBM ESD targets better than nothing?

- **This would only give a false sense of security and could result in extensive cost of analysis, customer delays and a circuit performance impact. (Remember, higher HBM ICs may be harder to protect!)**
- **System ESD protection depends on the pin application and therefore requires a different strategy.**
- **System level ESD is clearly important, but targeting and relying on excessive component level requirements could pull resources away from addressing and designing better system level ESD.**

It is often heard that the IEC 61000-4-2 pulse is a superposition of a CDM and a HBM pulse. Can IEC 61000-4-2 ESD testing replace CDM and HBM testing?

- **Looking at the two peaks in an IEC 61000-4-2 pulse, the time duration is indeed comparable to a CDM and HBM pulse.**
- **However the required levels and discharge nature are completely different.**
- **This is because CDM is intended for component level testing while IEC61000-4-2 is intended for system level testing.**

Since ICs are now designed for lower component ESD levels, why would this not be reflected by a sudden change in the overall health of a system for its ESD capability?

- **The overall health of a system is dependent on a comprehensive approach to the protection methodology that includes a number of factors including on board protection components, optimized board signal routing, component packaging and, as a last line of defense, the component level protection.**

If a component with the new lower ESD levels starts showing high levels of system failures how will the industry address this?

- **First, an investigation comparing ICs from provider A and provider B should look at the details of the component level ESD designs, not just the component failure levels in volts.**
- **Second, the OEM should share the system level ESD test results with the IC providers. For example, if IC provider A fails and IC provider B (2nd source) passes. IC provider A needs to investigate why their IC fails.**
- **Next, the OEM should review their ESD protection design for further improvement for both IC suppliers. This type of dialogue is important in the future.**

Is there a correlation between device failure thresholds and real world system level failures?

- There is rarely correlation between device (IC level) failure thresholds and real world system level failure in the field.
- Device failure thresholds are based on a simulated ESD voltage and current directly injected into (or extracted from) the device (IC) with the device in a powered down condition.
- Real world system level failures in the field occur in many different conditions, most of which are powered.