TEXAS INSTRUMENTS

Open Defects in Release

ID	Summary	State	Reported In Release	Target Release	Workaround	Release Notes
SDSCM00052843	Using .cdecls directive causes compiler to get header files from temporary directory	Open	ARM_5.2.6		Remove the files from the TEMP directory.	
SDSCM00052754	Compiler fails to attach #pragma INTERRUPT to template template function	Open	ARM_5.2.6			
SDSCM00052592	On MSP432, #pragma vector= cannot be applied to static member function although it could be on MSP430	Open	ARM_5.2.5			
SDSCM00051742	CCS Help Contents does not show the ARM and C2000 Compiler Users Guides	Open	ARM_5.2.0			

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SDSCM00051292	__rev should accept and return an unsigned int instead of a signed int.	Accepted	ARM_5.2.1			
SDSCM00050861	Should accept 2-operand add in ARM mode	Accepted	ARM_5.2.0B1			
SDSCM00050499	The .label assembler directive should not be accepted when assembling for ELF.	Accepted	ARM_5.2.0B1			
SDSCM00050131	Local struct with non-constant initializer treated as static scope variable	Accepted	ARM_5.2.0B1			
SDSCM00049911	__aeabi_dcmpun returns 1 for Inf and -Inf	Accepted	ARM_5.2.0B1			
SDSCM00049284	Compiler misreports Misra warning 10.1	Accepted	ARM_5.2.0B1			
SDSCM00049280	Ill advised enum scalar usage gets MISRA diagnostic, but similar usage of enum array does not	Open	ARM_5.2.0B1			

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SDSCM00049278	Array that is correctly initialized erroneously gets a MISRA diagnostic about size not being specified	Open	ARM_5.2.0B1			
SDSCM00048267	Warning generated when using __curpc intrinsic on Thumb 2	Accepted	ARM_5.2.0B1			
SDSCM00047902	Predefined macro __TI_FPv4SPD16_SUPPORT__ should be __TI_FPV4SPD16_SUPPORT__	Accepted	ARM_5.2.0B1			
SDSCM00047077	Incorrectly reduced double constant to float when ultimate destination is short	Accepted	ARM_5.2.0B1			
SDSCM00046352	Disassembler does not emit certain instructions in UAL form by default	Accepted	ARM_5.2.0B1			
SDSCM00046102	MISRA 12.8 and MISRA 10.5 false positives	Accepted	ARM_5.2.0B1			

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SDSCM00046074	Cortex-M0 library lacks uread4, etc.	Open	ARM_5.2.0B1		If using the TI compiler, the TI compiler doesn't call any of these functions, so no workaround should be necessary. If using any other vendor's compiler and linking with the TI toolchain, link with the other vendor's toolchain.	
SDSCM00044038	float library functions misbehave with --abi=eabi -mv5e -me --float_support=fpalib	Accepted	ARM_5.2.0B1			
SDSCM00044035	float library functions misbehave with -me --float_support=fpalib	Accepted	ARM_5.2.0B1		Use --float_support=vfplib instead.	

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SDSCM00042945	-pdse=195 causes an error under EABI if any standard header file is included	Accepted	ARM_5.2.0B1			
SDSCM00042418	Internal error when compiling code with WEAK functions; linker crash	Accepted	ARM_5.2.0B1		None	
SDSCM00040934	Structure is not initialized correctly when using -o2 or -o3 optimization	Accepted	ARM_5.2.0B1		The initialization will have to be done at run-time, through a __sti initialization routine. You can see this routine when compiling without optimization. To workaround the compiler removing this initialization routine, initialize the object at the beginning of main: Info2.mSize = ((unsigned)_end_isr_stack - (unsigned)_start_isr_stack);	

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SDSCM00040523	The _ssat16 intrinsic allows literals in the range of 0-31, but the SSAT16 instruction only accepts values from 1-16	Accepted	ARM_5.2.0B1			
SDSCM00040522	_ssatl intrinsic allows 3rd argument to be 0 resulting in an assembler error.	Accepted	ARM_5.2.0B1			
SDSCM00039636	When creating a partial linked ELF object file, the linker uses virtual addresses instead of relative addresses.	Accepted	ARM_5.2.0B1			
SDSCM00039626	ARM assembler does not issue a warning for PC-relative loads when --embedded_constants=off	Accepted	ARM_5.2.0B1			
SDSCM00039220	Assembler does not accept the SP operand of the SRSDB instruction	Accepted	ARM_5.2.0B1		Omit the SP! operand and the instruction should assemble correctly.	

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SDSCM00038278	ARM floating point conversion routines do not support NaN	Accepted	ARM_5.2.0B1			
SDSCM00037227	ARM disassembler error for VMRS instruction	Accepted	ARM_5.2.0B1			
SDSCM00037086	ARM assembler allows incorrect VFP registers for some instructions on D16 VFP architectures	Accepted	ARM_5.2.0B1			
SDSCM00037008	Linker outputting wrong build attribute name for EABI TAG_VFP_arch on ARM targets	Accepted	ARM_5.2.0B1			
SDSCM00036874	Section relative ELF symbol values in partially linking object files should hold the section offset for the symbol	Accepted	ARM_5.2.0B1			

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SDSCM00036773	LDM/STM - DA/FA/IB/ED viariant instructions erroneously accepted by assembler for Cortex-M3	Accepted	ARM_5.2.0B1			
SDSCM00036770	LDREXD and STREXD instructions erroneously generate errors on Cortex A8 and R4	Accepted	ARM_5.2.0B1			
SDSCM00018691	Linker gives misleading warning when dot expressions used in SECTION directive for .stack section	Accepted	ARM_5.2.0B1			
SDSCM00014430	calloc doesn't check arguments to make sure the requested size is reasonable	Accepted	ARM_5.2.0B1			

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SDSCM00008928	Extern inline functions are not supported in the C/C++ Compiler with COFF ABI	Accepted	ARM_5.2.0B1			This bug only affects COFF ABI. If a function is declared as inline and there are no references to it in the same file, the function is eliminated and can't be called from another file.
SDSCM00008685	DWARF does not correctly represent variables stored in register pairs	Accepted	ARM_5.2.0B1		Although 'var1' and 'var2' are shown to be in single registers, a debugger could determine that they are actually stored in register pairs by looking at the type of the variables: [00000113] DW_TAG_base_type DW_AT_name long long DW_AT_encoding 0x5 DW_AT_byte_size 0x8 The base type indicates that the	

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					size of the variables is 0x8 bytes. Since a single register can only store 0x4 bytes of information, it would take two registers to hold this values. On TI architectures, values stored in multiple registers are always stored in consecutive registers. Thus, the debugger would know that if the entire value could not fit in A4, the rest of the value must be in A5. A5 would contain the upper 32 bits of the value.	
SDSCM00008543	Forward reference in .space generates an internal error	Accepted	ARM_5.2.0B1		none	

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SDSCM00008465	Language Conformance: crash because of void pointer dereference	Accepted	ARM_5.2.0B1		Please describe the workaround for this problem.	
SDSCM00008248	Compilers on PC will not work without TMP set	Accepted	ARM_5.2.0B1		Set the TMP environment variable, even if just set to . (current directory)	
CODEGEN-24	Compiler mistakenly issues MISRA 17.6: The address of an object with automatic storage shall not be assigned to another obje	Open	ARM_5.2.7			

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