AM64x/AM243x EVM BOARD
PROC101C

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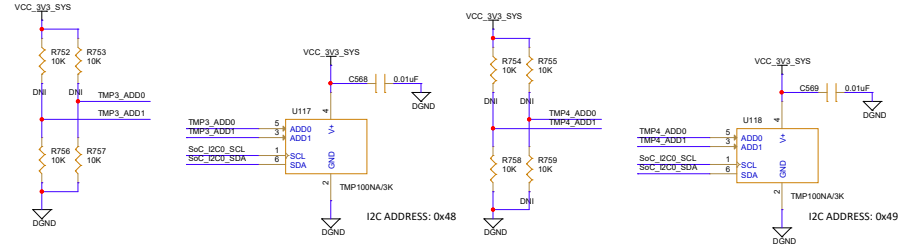
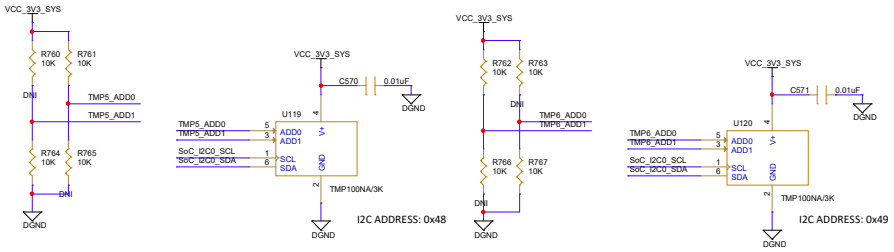
SoC_I2C0_SCL
SoC_I2C0_SDA
SoC_I2C0_SCL
SoC_I2C0_SDA

TEMPERATURE SENSOR



SoC_I2C1_SCL
SoC_I2C1_SDA
SoC_I2C1_SCL
SoC_I2C1_SDA

TEMPERATURE SENSOR



NOTE: PLACE TEMP SENSOR CORNERS OF THE BOARD

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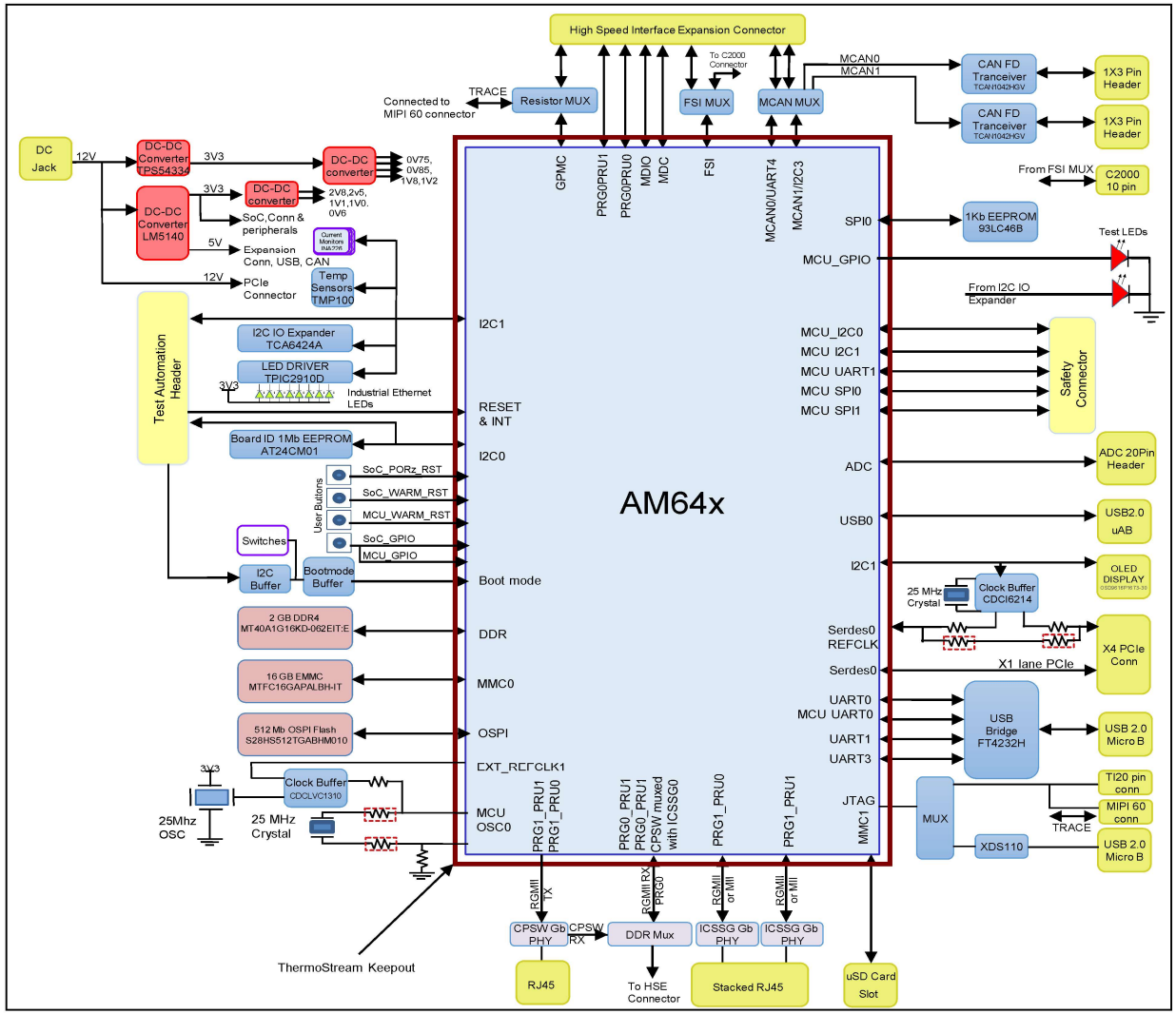
REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.1	11th MARCH 2022	Drafted from "PROC101B_SCH" document.	Mistral Design Team	AJIT MB	AJIT MB
0.2	11th MARCH 2022	Removed Voltage Monitor circuit & added RC Delay Circuit for power down sequence requirement Fixed Power down sequence issue seen on AM243x REV B	Mistral Design Team	AJIT MB	AJIT MB
0.3	11th MARCH 2022	Updated schematics to support PG2 Silicon	Mistral Design Team	AJIT MB	AJIT MB
1.0	30th MARCH 2022	Baselined and Released	Mistral Design Team	AJIT MB	AJIT MB
1.1	5th AUG 2022	Updated SoC Part Number and OPN Details Updated SoC Symbol for Reserved pins	Mistral Design Team	AJIT MB	AJIT MB

BLOCK DIAGRAM_AM64x_EVM



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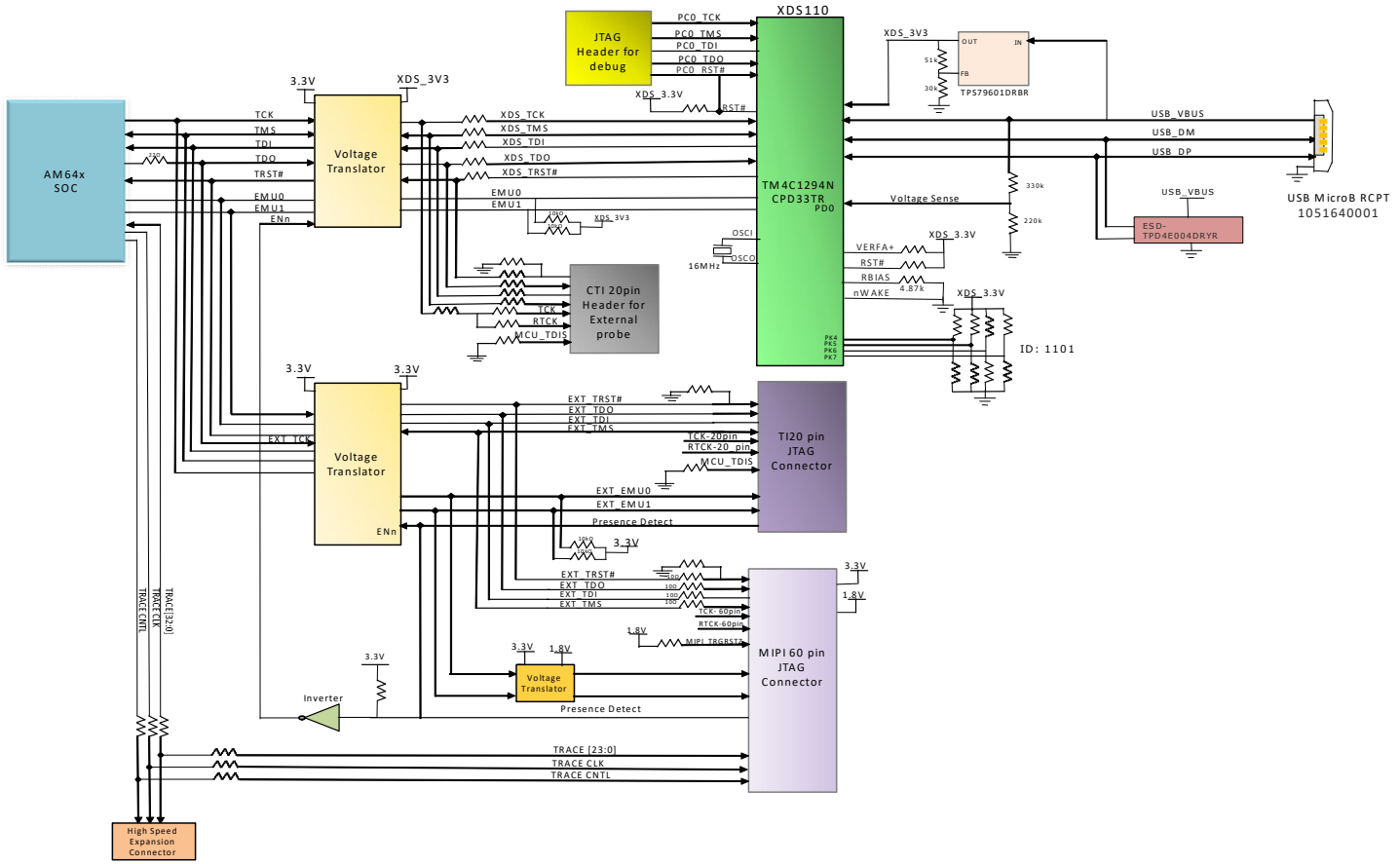
BLOCK DIAGRAM_XDS110



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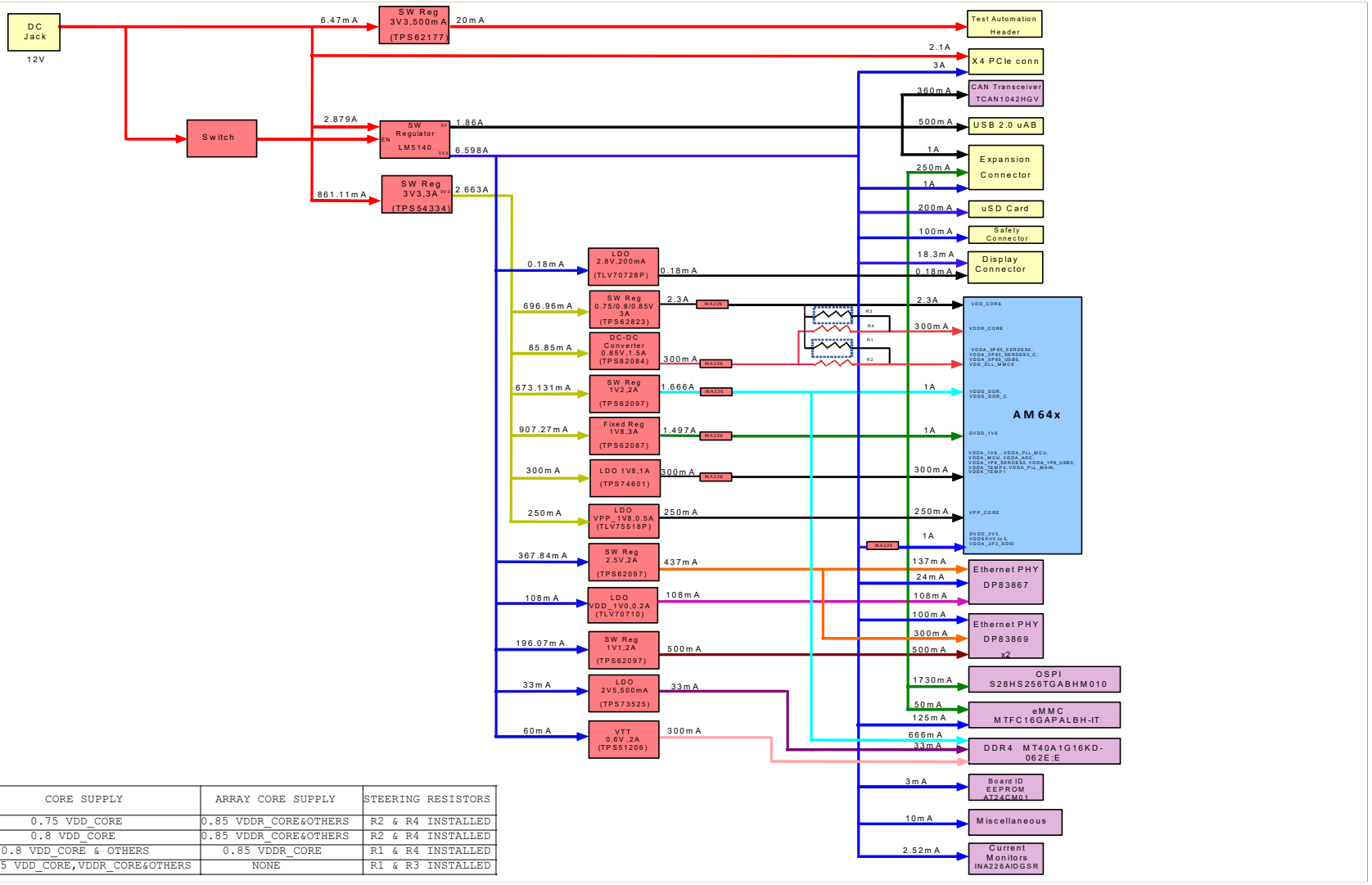
POWER FLOW DIAGRAM



CORE SUPPLY	ARRAY CORE SUPPLY	STEERING RESISTORS
0.75 VDD_CORE	0.85 VDDR_CORE&OTHERS	R2 & R4 INSTALLED
0.8 VDD_CORE	0.85 VDDR_CORE&OTHERS	R2 & R4 INSTALLED
0.8 VDD_CORE & OTHERS	0.85 VDDR_CORE	R1 & R4 INSTALLED
0.85 VDD_CORE,VDDR_CORE&OTHERS	NONE	R1 & R3 INSTALLED

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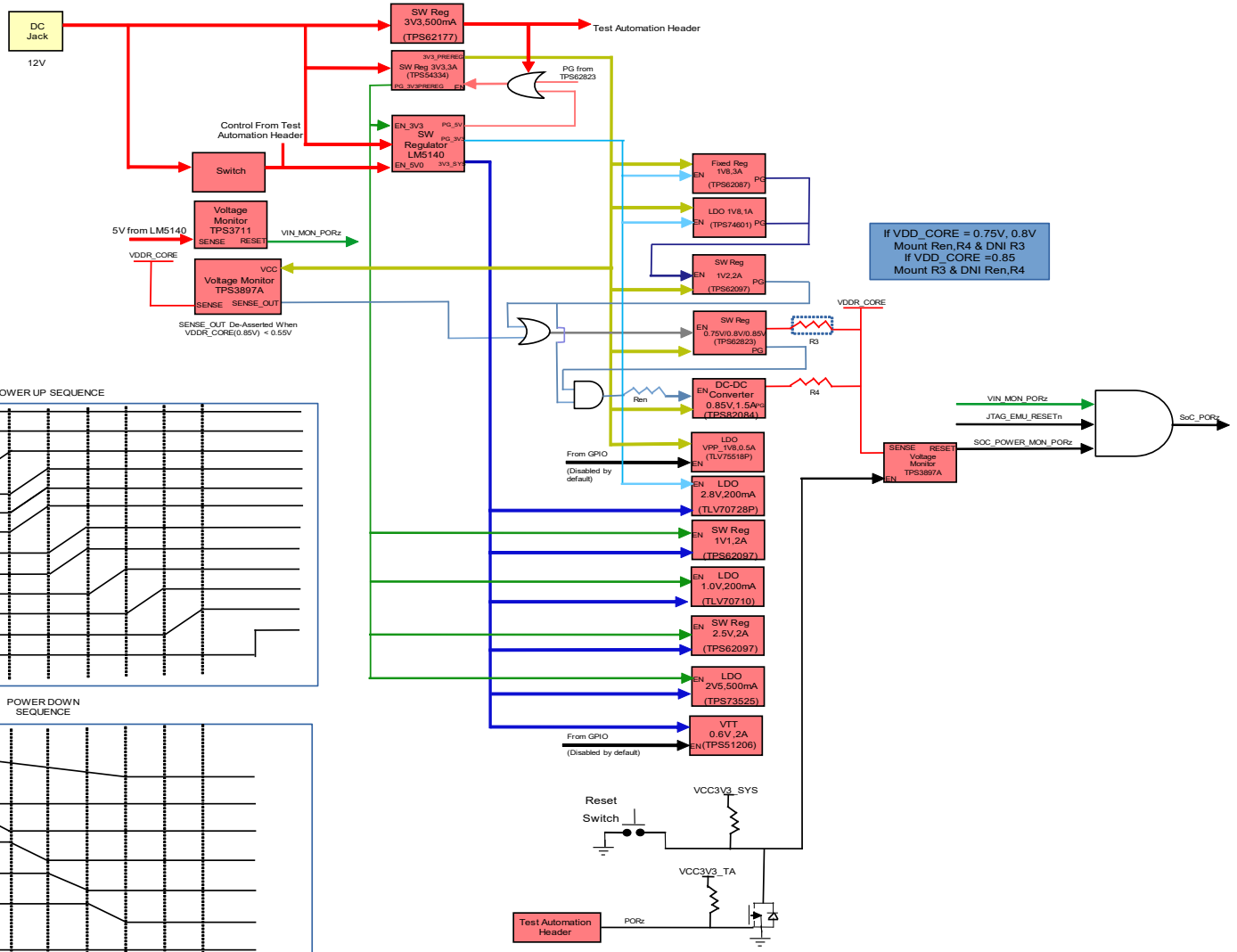
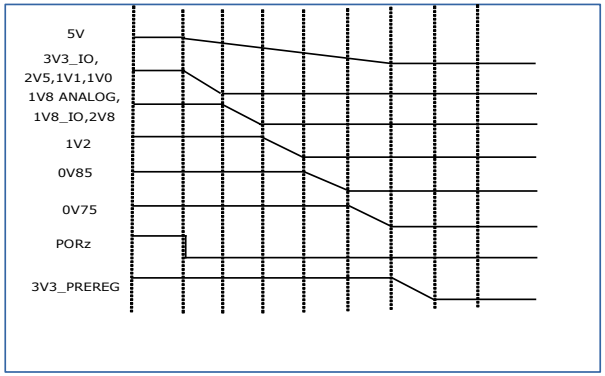
POWER SEQUENCE



POWER UP SEQUENCE

POWER DOWN SEQUENCE



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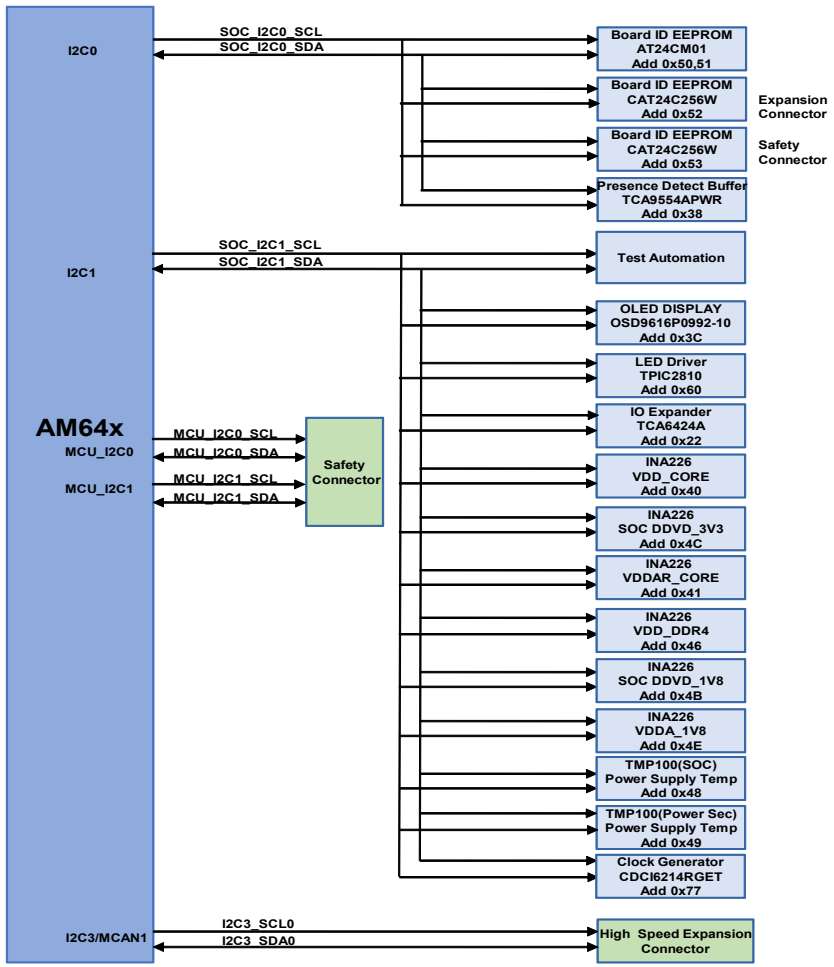
GPIO MAPPING TABLE

S.NO	GPIO DESCRIPTION	GPIO NETNAME	REQUIRED ON	FUNCTIONALITY	GPIO USED	SoC Muxed Signal Name	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE
1	EMMC RESET Control GPIO	GPIO_eMMC_RSTn	GP EVM	Reset	IO EXPANDER- P00		OUTPUT	HIGH	LOW
2	OSPI RESET Control GPIO	GPIO_OSPI_RSTn	GP EVM	Reset	GPIO013	OSPI0_CS2	OUTPUT	HIGH	LOW
3	CPSW RGMII1 RESET Control GPIO	GPIO_CPSW1_RST	GP EVM	Reset	IO EXPANDER- P02		OUTPUT	HIGH	LOW
4	PRG1 RGMII1 Ethernet PHY RESET Control GPIO	GPIO_RGMII1_RST	GP EVM	Reset	IO EXPANDER- P03		OUTPUT	HIGH	LOW
5	PRG1 RGMII2 Ethernet PHY RESET Control GPIO	GPIO_RGMII2_RST	GP EVM	Reset	IO EXPANDER- P04		OUTPUT	HIGH	LOW
6	PRG1 RGMII1 Ethernet PHY Link Detection GPIO	PRG1_ETH1_LED_LINK	GP EVM	Link Detection	PRG1_PRU0_GPO8		INPUT	LOW	HIGH
7	PRG1 RGMII2 Ethernet PHY Link Detection GPIO	PRG1_ETH2_LED_LINK	GP EVM	Link Detection	PRG1_PRU1_GPO8		INPUT	LOW	HIGH
8	CPSW Ethernet PHY Interrupt	CPSW_RGMII_INTn	GP EVM	Interrupt	Connected to PRG1_RGMII_INT via 0E res		INPUT	HIGH	LOW
9	PRG1 Ethernet PHY 1Interrupt	PRG1_RGMII_INT	GP EVM	Interrupt	GPIO1_70	EXTINTn	INPUT	HIGH	LOW
10	PRG1 Ethernet PHY 2Interrupt			Interrupt			INPUT	HIGH	LOW
11	PCIe RESET Control GPIO	GPIO_PCIe_RST_OUT	GP EVM	Reset	IO EXPANDER- P05		OUTPUT	LOW	HIGH
12	SD card load switch enable control	MMC1_SD_EN	GP EVM	Load SW Enable	IO EXPANDER- P06		OUTPUT	HIGH	LOW
13	One GPIO is required to control the Mux select between HSE and FSI Connector	FSI_FET_SEL	GP EVM	Mux Seleection	IO EXPANDER- P07		OUTPUT	PREFERABLE	PREFERABLE
14	One GPIO is required to enable Standby mode in CAN tranceiver	MCAN0_STB_3V3	GP EVM	Standby mode selection	IO EXPANDER- P10		OUTPUT	LOW	HIGH
15	One GPIO is required to enable Standby mode in CAN tranceiver	MCAN1_STB_3V3	GP EVM	Standby mode selection	IO EXPANDER- P11		OUTPUT	LOW	HIGH
16	One GPIO is required to control the Mux select between HSE and Ethernet PHY	CPSW_FET_SEL	GP EVM	Mux Seleection	IO EXPANDER- P12		OUTPUT	PREFERABLE	PREFERABLE
17	MDC/MDIO FET Switch Select for Mux	PRG1_RGMII2_FET_SEL	GP EVM	Mux Selection	IO EXPANDER- P14		OUTPUT	PREFERABLE	PREFERABLE
18	VTT 0.6V regulator Enable	VTT_EN	GP EVM	VTT 0.6V regulator Enable	GPIO0_12	OSPI0_CSn1	OUTPUT	LOW	HIGH
19	TEST GPIO1 from Test Automation Connector/ GPIO for GP board push button	TEST GPIO1/GPIO1_43	GP EVM	GPIO for communications with AM64x	GPIO1_43	SPI0_CS1	INPUT	HIGH	LOW
20	TEST GPIO2 from Test Automation Connector	TEST GPIO2	GP EVM	GPIO for communications with AM64x	IO EXPANDER- P15		INPUT	HIGH	LOW
21	OLED Display RESET GPIO	GPIO_OLED_RESETn	GP EVM	Reset	IO EXPANDER- P16		OUTPUT	LOW	HIGH
22	IO Expander Interrupt	IO_EXP_INTn	GP EVM	Interrupt	GPIO1_78	MMC1_SDWP	INPUT	HIGH	LOW
23	VPP 1.8V regulator Enable	VPP_LDO_EN	GP EVM	VPP 01.8V regulator Enable	IO EXPANDER- P17		OUTPUT	LOW	HIGH
24	One GPIO is required to control the Mux select between HSE and CAN Interface	CAN_MUX_SEL	GP EVM	Mux Seleection	IO EXPANDER- P01		OUTPUT	LOW	HIGH
25	User LED	TEST_LED1	GP EVM	Test	IO EXPANDER- P20		OUTPUT	LOW	HIGH
26	User LED	TEST_LED2	GP EVM	Test	MCU_SPI1_CS0	MCU_GPIO0_5	OUTPUT	LOW	HIGH
27	One GPIO to enable the PCIe Clock generator outputs	CDC_OE1/E4	GP EVM	Clock output enable	IO EXPANDER- P21		OUTPUT	HIGH	HIGH

I2C TREE



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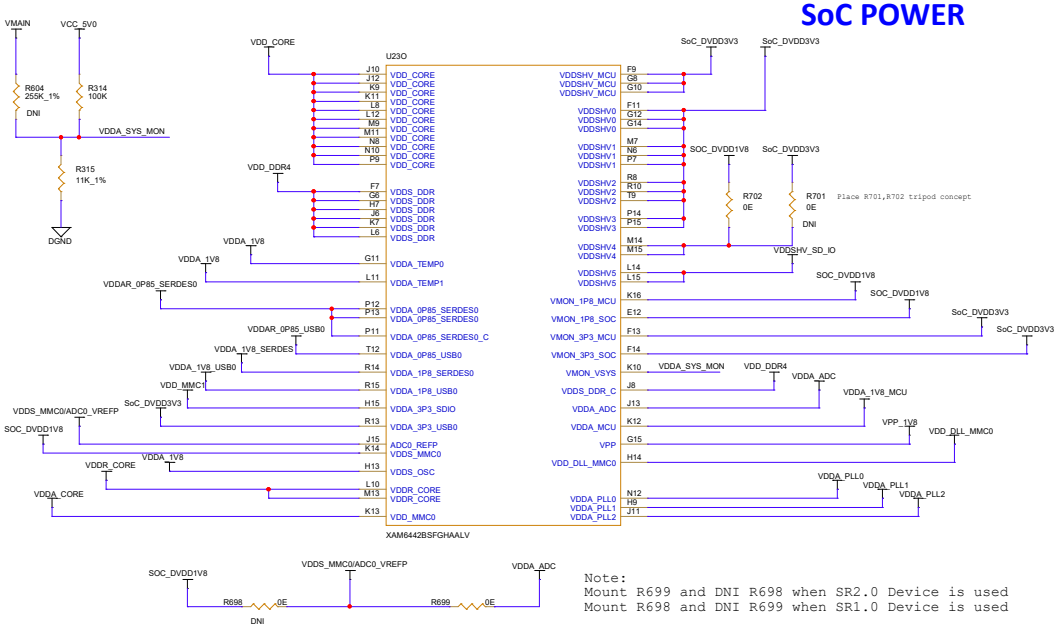
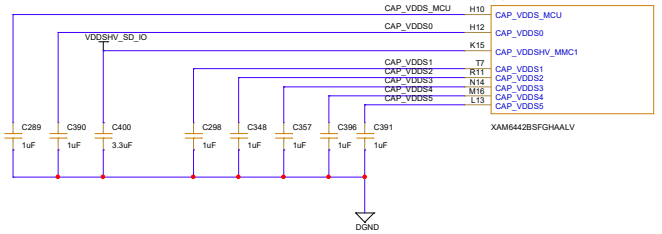
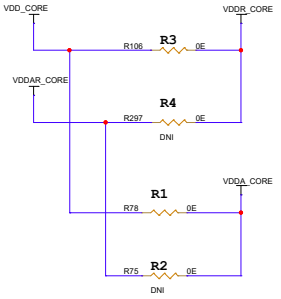
SoC POWER

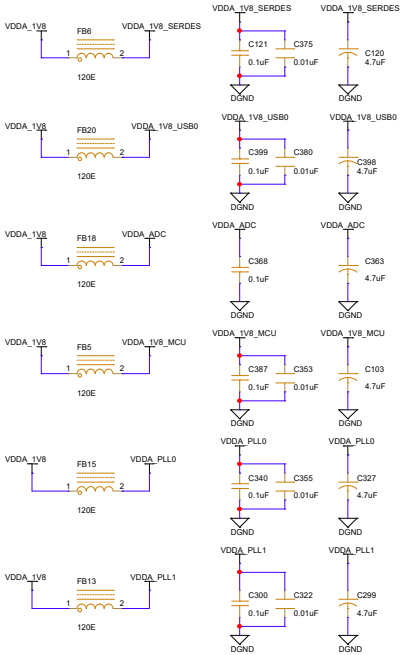


Note:
Mount R699 and DNI R698 when SR2.0 Device is used
Mount R698 and DNI R699 when SR1.0 Device is used

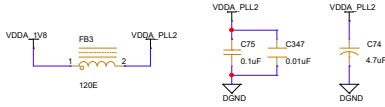




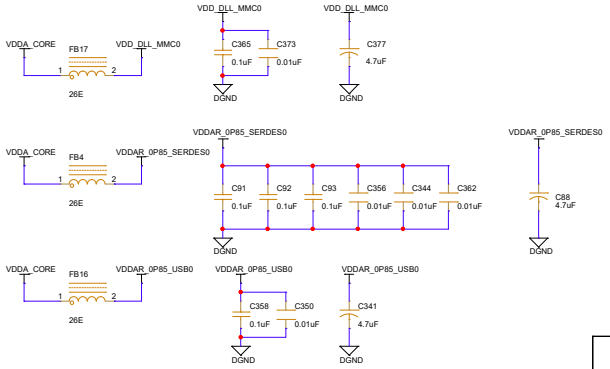
1.8V Analog SUPPLY



1.8V Analog SUPPLY



CORE SUPPLY



CORE SUPPLY	ARRAY CORE SUPPLY	STEERING RESISTORS
0.75 VDD_CORE	0.85 VDDR_CORE&OTHERS	R2 & R4 INSTALLED
0.8 VDD_CORE	0.85 VDDR_CORE&OTHERS	R2 & R4 INSTALLED
0.8 VDD_CORE & OTHERS	0.85 VDDR_CORE	R1 & R4 INSTALLED
0.85 VDD_CORE,VDDR_CORE&OTHERS	NONE	R1 & R3 INSTALLED

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TEXAS INSTRUMENTS MISTRAL

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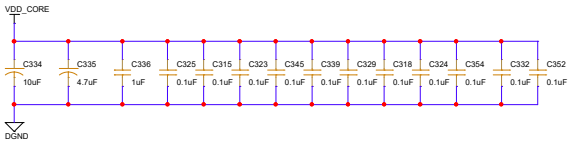
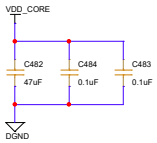
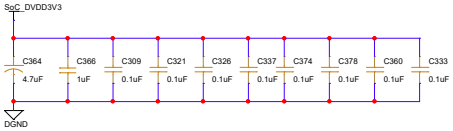
SoC POWER Decaps



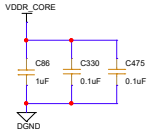
Place one 0.1uF cap near each Pin

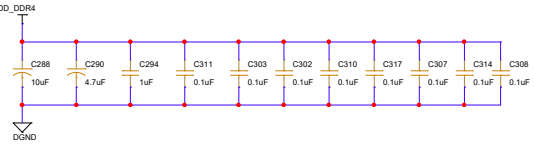


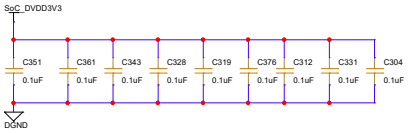
To place after current sense resitor on VDD_CORE plane

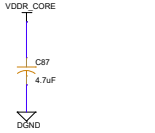


Place one 0.1uF cap near each Pin

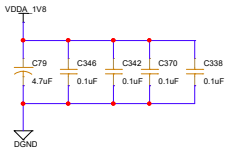




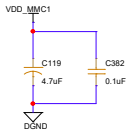




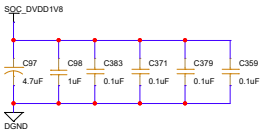
VDD ARRAY CORE

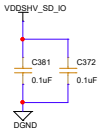


VDDA_3P3_SDIO



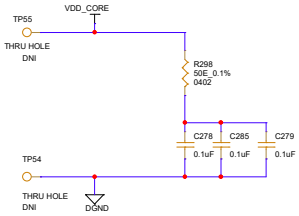
Place one 0.1uF cap near each Pin

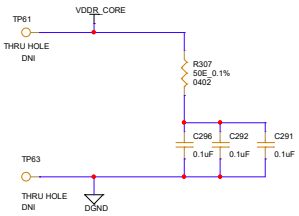




Place one 0.1uF cap near each Pin

Core & Array Core Supply Kelvin Sensing





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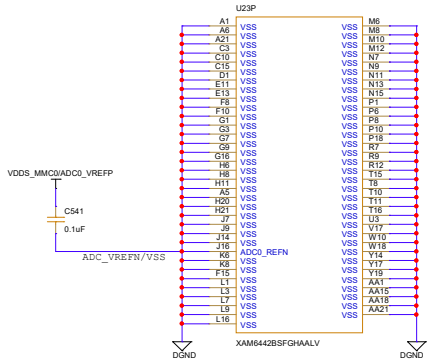
SoC POWER - VSS



CAD Note:
Place CAP C541
between pins
J15 and J16

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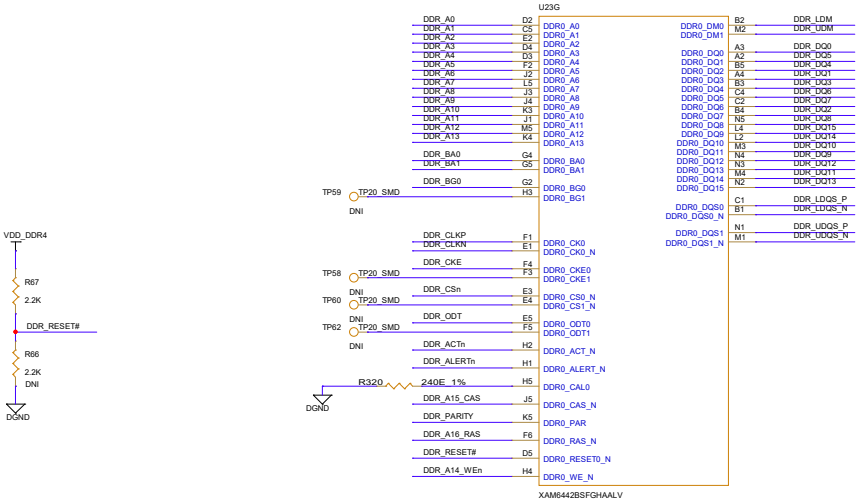
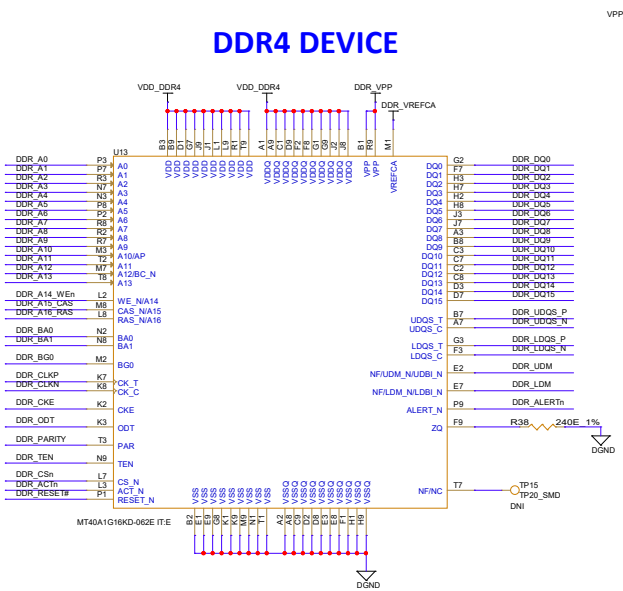
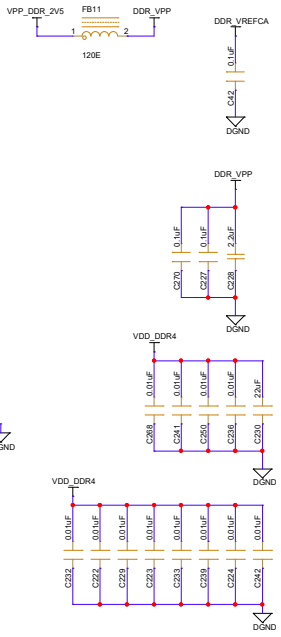
SoC DDR INTERFACE



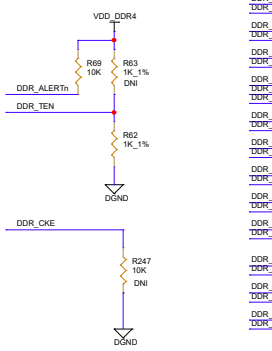
DDR DQ Lines Swapped
With Data Byte

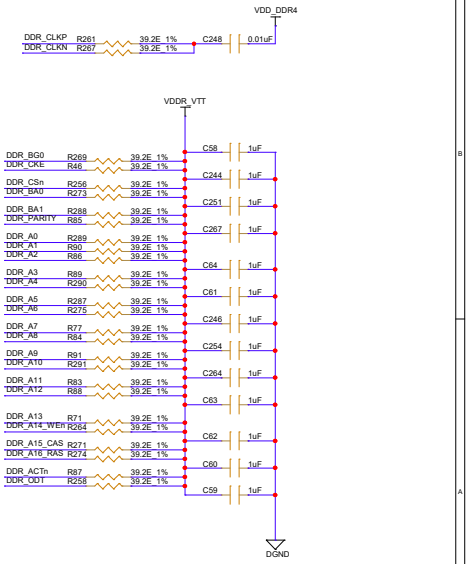
DDR4 DEVICE





DDR TERMINATION





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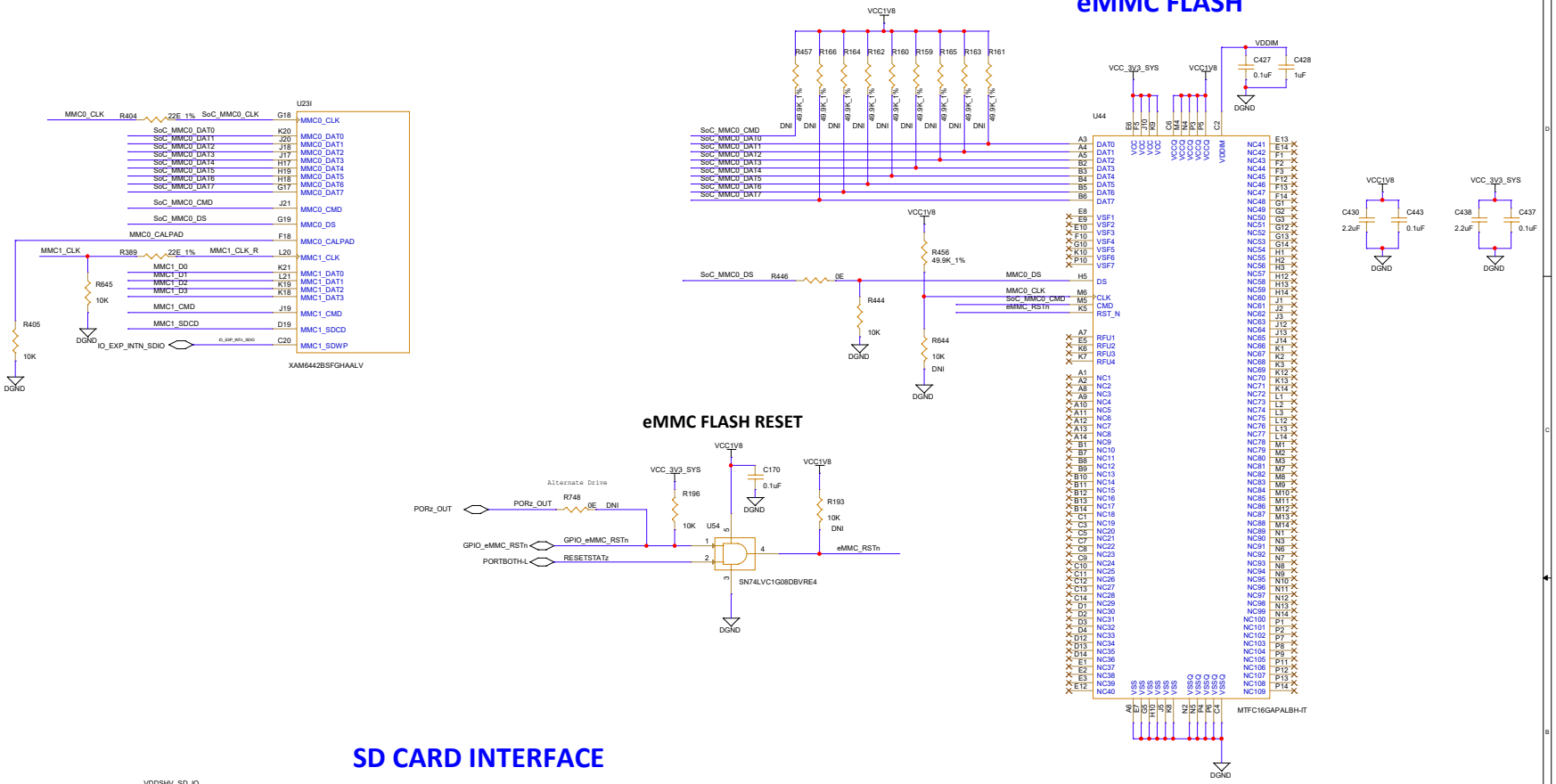
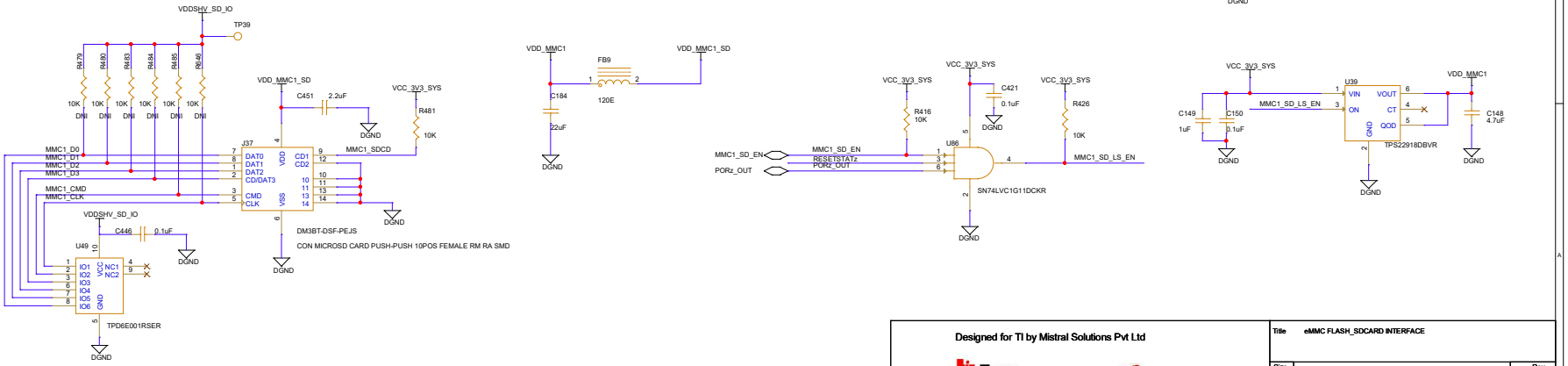
eMMC FLASH



eMMC FLASH RESET

SD CARD INTERFACE



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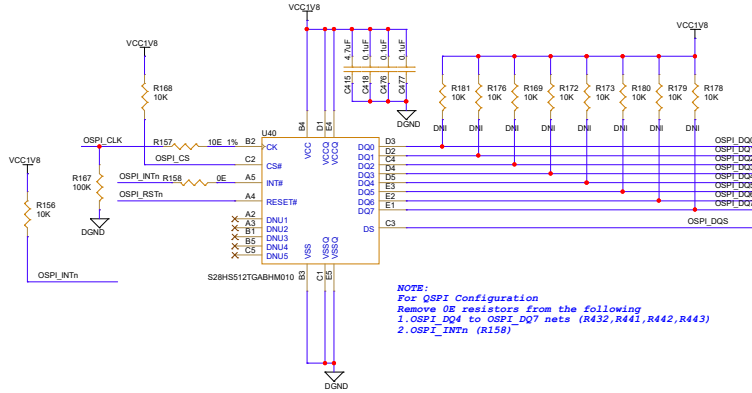
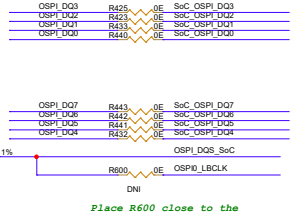
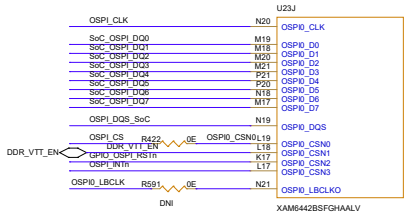
OSPI FLASH



NOTE:
For QSPI Configuration
Remove 0E resistors from the following
1.OSPI_DQ4 to OSPI_DQ7 nets (R432,R441,R442,R443)
2.OSPI_INTn (R158)



Place R600 close to the memory to avoid stub

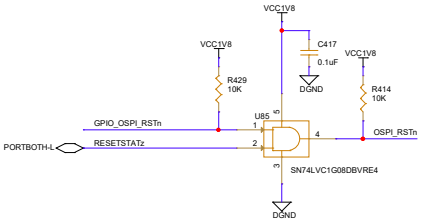


Place R591 close to the ball with as little trace as possible

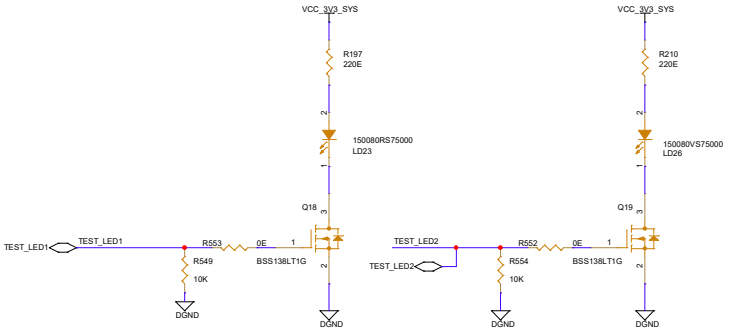
To Route DQS to LBCLK0	To Route DQS to SOC's DQS
Mount R591 & R600	Mount R601 & R592
DNI R601 & R592	DNI R591 & R600

SOC OSPI INTERFACE

OSPI FLASH RESET



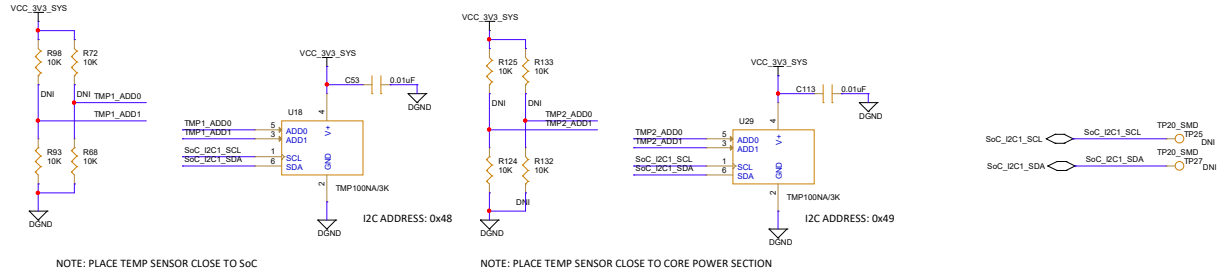
USER TEST LED



Designed for TI by Mistral Solutions Pvt Ltd

Title	OSPI	
Size: C	Variant Name = <Core Design>	Rev: E2
Date: Wednesday, July 30, 2025	Sheet 14 of 40	

TEMPERATURE SENSOR

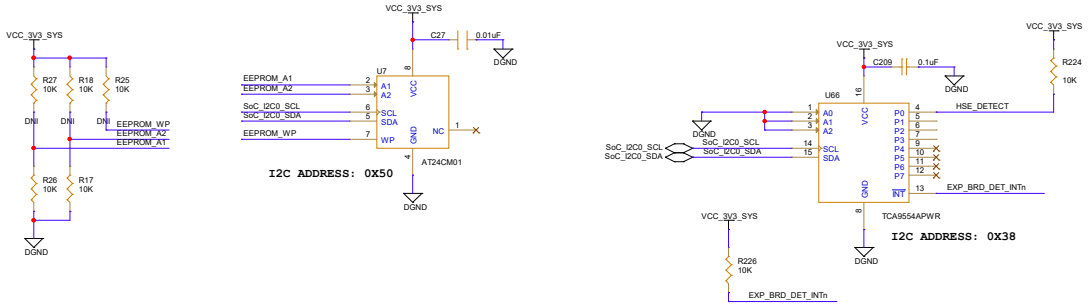


NOTE: PLACE TEMP SENSOR CLOSE TO SoC

NOTE: PLACE TEMP SENSOR CLOSE TO CORE POWER SECTION

BOARD ID EEPROM

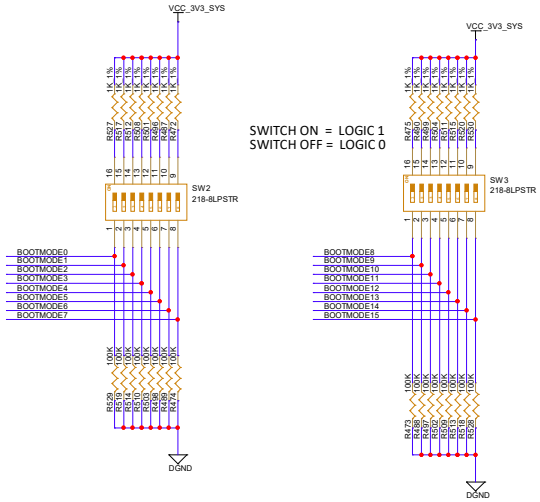
BOARD PRESENCE DETECT CIRCUIT



Designed for TI by Mistral Solutions Pvt Ltd

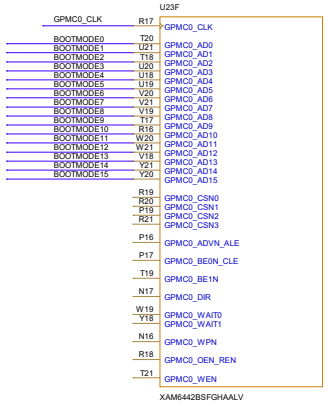
Title	EEPROM,PRESENCE DETECTION & TEMP SENSOR	
Size: C	Variant Name = <Core Design>	Rev: E2
Date: Wednesday, July 30, 2025	Sheet 15 of 40	

In next revesion we can have boot strap Resistors to configure the boot method.



SWITCH ON = LOGIC 1
SWITCH OFF = LOGIC 0

GPMC



BOOT MODES SUPPORTED

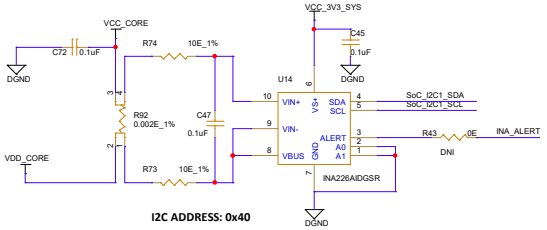
1. OSPI
2. MMC1 - SD CARD
3. MMC0 - eMMC
4. CPSW Ethernet Slave
5. USB Host
6. USB Device
7. UART
8. Ethernet

Designed for TI by Mistral Solutions Pvt Ltd

Title	BOOT MODE BUFFER & SWITCHES	
Size: C	Variant Name = <Core Design>	Rev: E2
Date: Tuesday, July 08, 2025	Sheet 20 of 40	

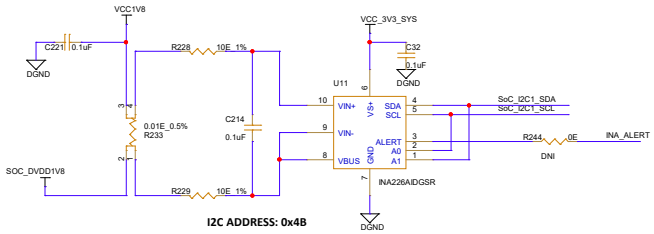
CURRENT MONITORING DEVICES

VDD_CORE



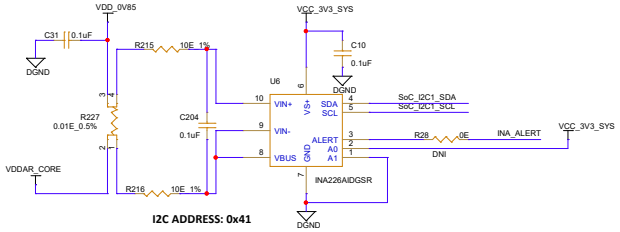
I2C ADDRESS: 0x40

SoC_DVDD1V8



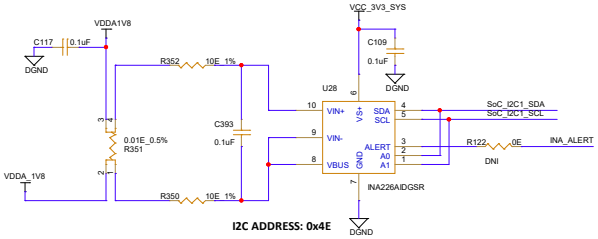
I2C ADDRESS: 0x4B

VDDAR_CORE



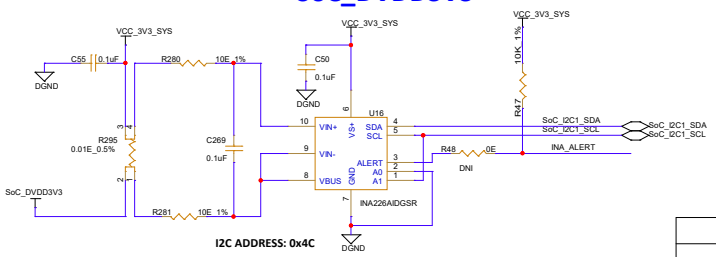
I2C ADDRESS: 0x41

VDDA_1V8

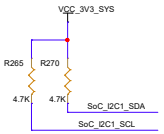


I2C ADDRESS: 0x4E

SoC_DVDD3V3

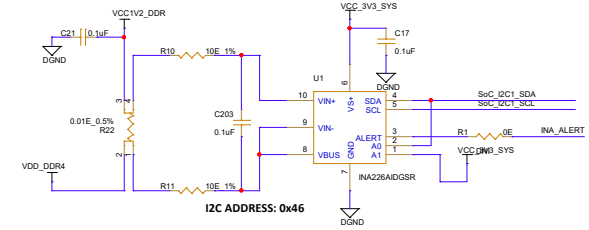


I2C ADDRESS: 0x4C



INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VDD_0V85	VDDAR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC1V8	SoC_DVDD1V8	4B
VDDA1V8	VDDA_1V8	4E
VCC1V2_DDR	VDD_DDR4	46

VDD_DDR4



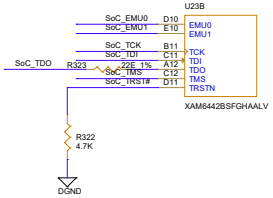
I2C ADDRESS: 0x46

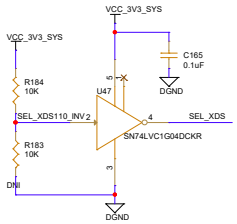
Designed for TI by Mistral Solutions Pvt Ltd

Title	CURRENT MONITORING DEVICES	
Size: C	Variant Name = <Core Design>	Rev: E2
Date: Wednesday, July 30, 2025	Sheet 21 of 40	

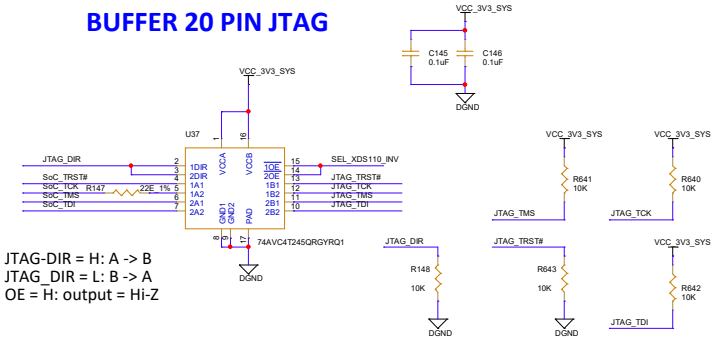
JTAG BUFFER

JTAG SoC SECTION

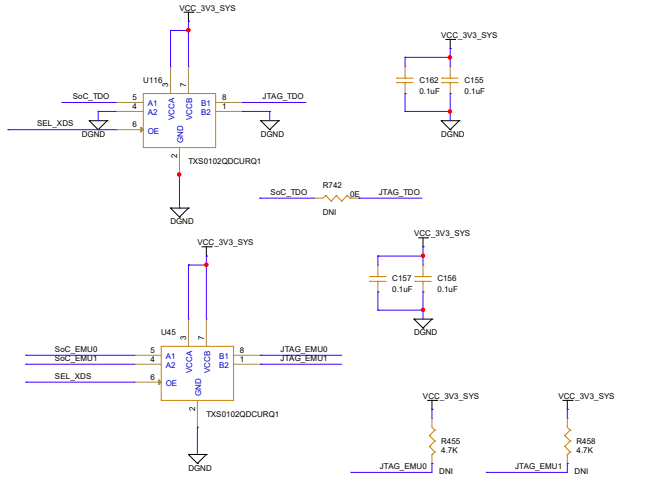




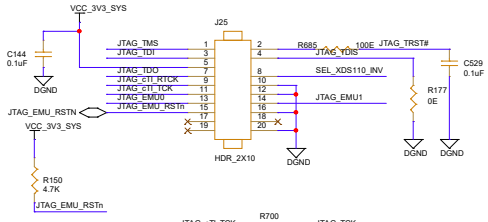
BUFFER 20 PIN JTAG

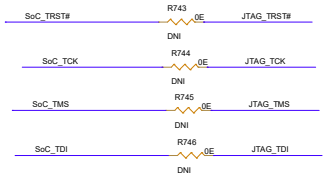


JTAG-DIR = H: A -> B
JTAG_DIR = L: B -> A
OE = H: output = Hi-Z



JTAG 20 PIN cTI CONNECTOR





Off Page Connections

From XDS1100 Debugger

24	SEL_XDS110_INV	SEL_XDS110_INV	
24	JTAG_EMU0	JTAG_EMU0	
24	JTAG_EMU1	JTAG_EMU1	
22	XDS110_TDI	XDS110_TDI	
22	XDS110_TCK	XDS110_TCK	
22	XDS110_TMS	XDS110_TMS	
22	XDS110_TRST#	XDS110_TRST#	
24	JTAG_TDI	JTAG_TDI	
24	JTAG_TCK	JTAG_TCK	
24	JTAG_TMS	JTAG_TMS	
24	JTAG_TRST#	JTAG_TRST#	
24	JTAG_TDO	JTAG_TDO	
22	XDS110_EMU0	XDS110_EMU0	
22	XDS110_EMU1	XDS110_EMU1	

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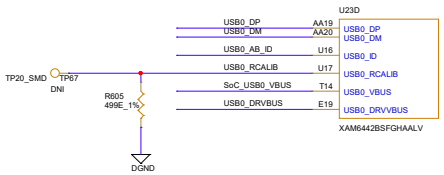
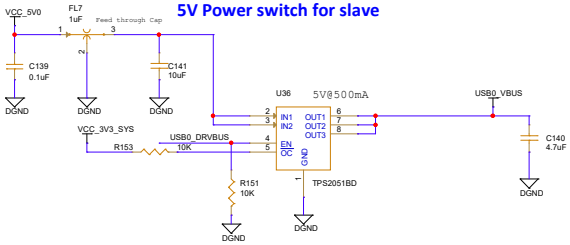
TEXAS INSTRUMENTS MISTRAL

Title	JTAG BUFFER		
Size	C	Variant Name = <Core Design>	Rev E2
Date:	Wednesday, July 30, 2025	Sheet 23 of 40	

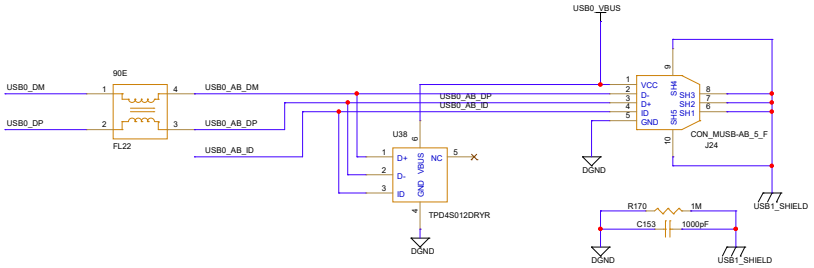
USB 2.0 INTERFACE

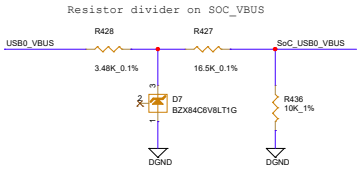


5V Power switch for slave



Micro USB 2.0 AB Connector





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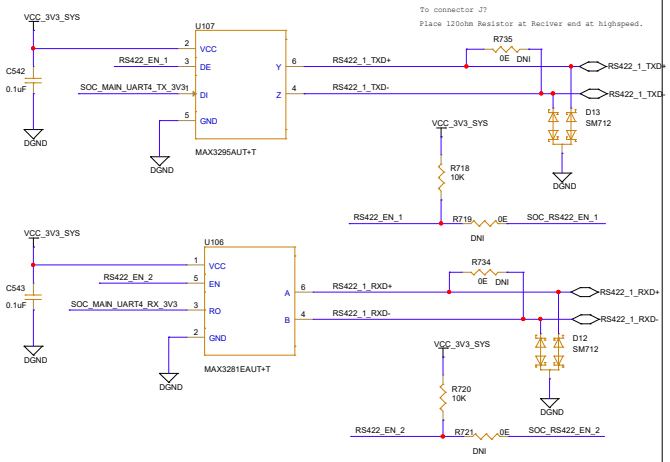
Title	USB 2.0 INTERFACE		
Size			Rev
C	Variant Name = <Core Design>		E2
Date:	Wednesday, July 30, 2025	Sheet 25 of 40	

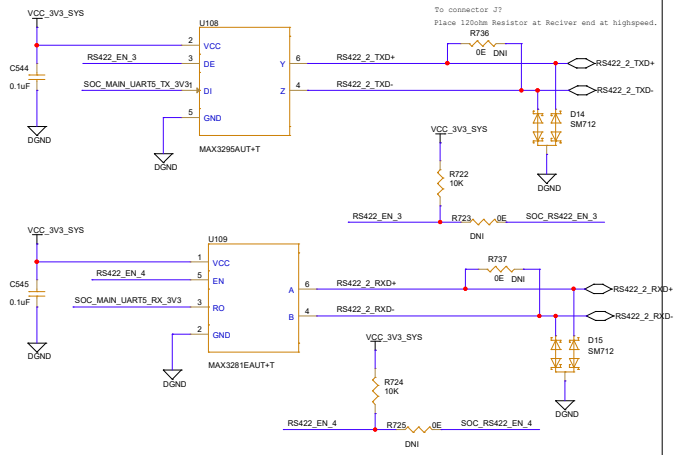
UART to RS422

IOCARD 1_UART to RS422

MAIN_UART - RS422 -1 TX/RX

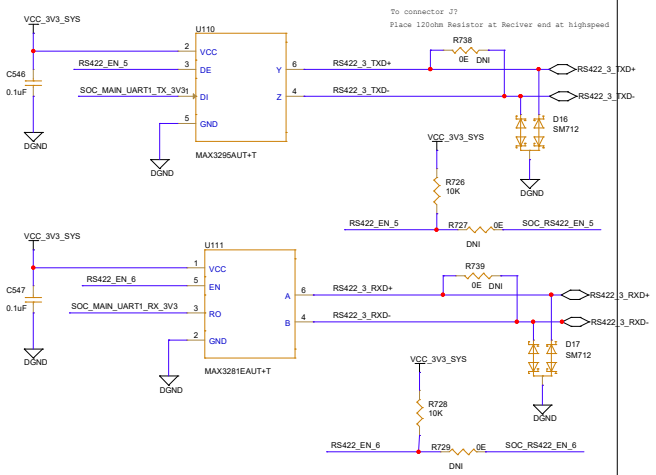


STANDBY_UART - RS422 -2 TX/RX

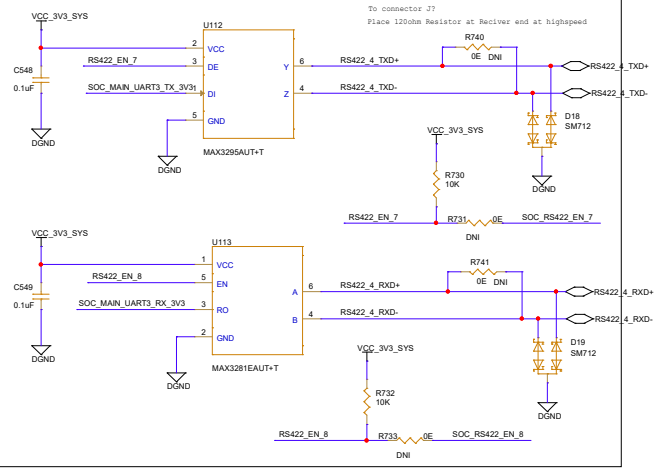


IOCARD 2_UART to RS422

MAIN_UART - RS422 -3 TX/RX



STANDBY_UART - RS422 -4 TX/RX



SOC_MAIN_UART4_TX_3V3
SOC_MAIN_UART4_RX_3V3
SOC_MAIN_UART5_TX_3V3
SOC_MAIN_UART5_RX_3V3
SOC_MAIN_UART3_TX_3V3
SOC_MAIN_UART3_RX_3V3
SOC_MAIN_UART1_TX_3V3
SOC_MAIN_UART1_RX_3V3

SOC_RS422_EN_1
SOC_RS422_EN_2
SOC_RS422_EN_3
SOC_RS422_EN_4
SOC_RS422_EN_5
SOC_RS422_EN_6
SOC_RS422_EN_7
SOC_RS422_EN_8

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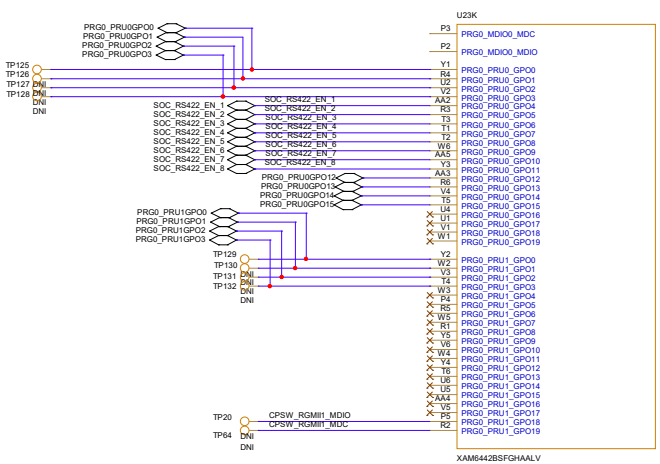
TEXAS INSTRUMENTS

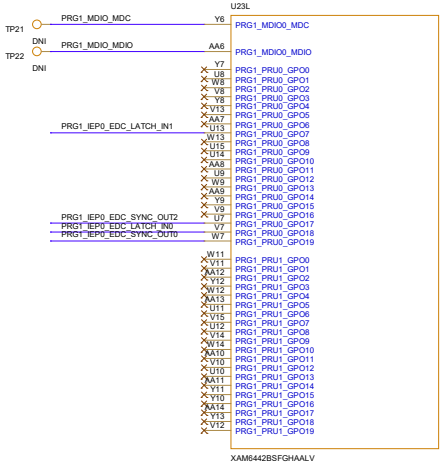
MISTRAL

Title	FT4232 UART TO USB BRIDGE	
Size: C	Variant Name = <Core Design>	Rev: E2
Date: Wednesday, July 30, 2025	Sheet 26 of 40	

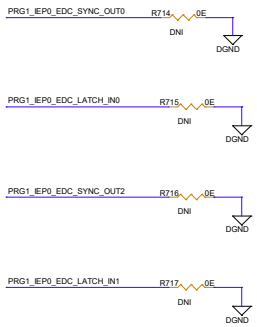
NC BLOCKS

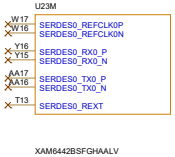
PRG0 & PRG1

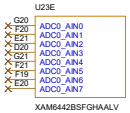




SYNC TP

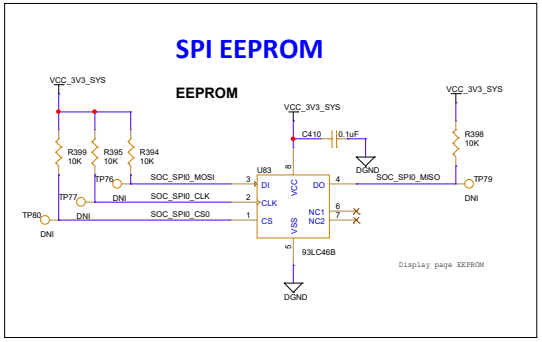


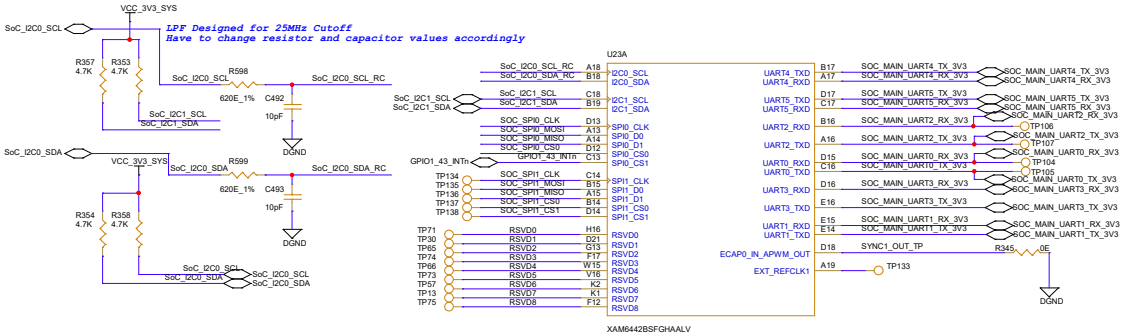




Designed for TI by Mistral Solutions Pvt Ltd

Title	HSE CONNECTOR		
Size	Variant Name = <Core Design>		Rev
C			E2
Date:	Tuesday, July 08, 2025	Sheet 27 of	40

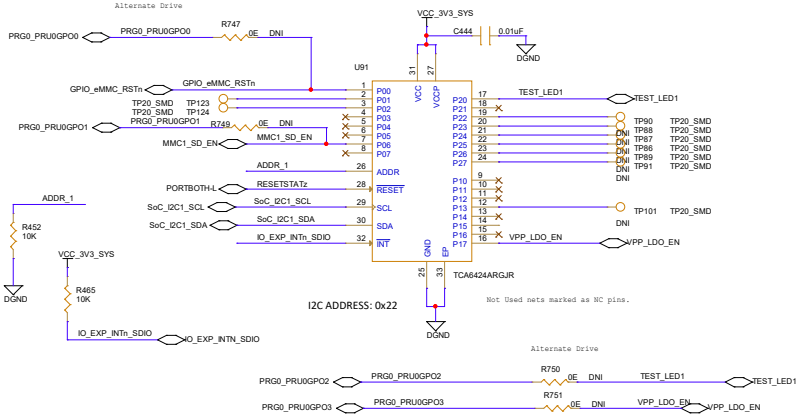




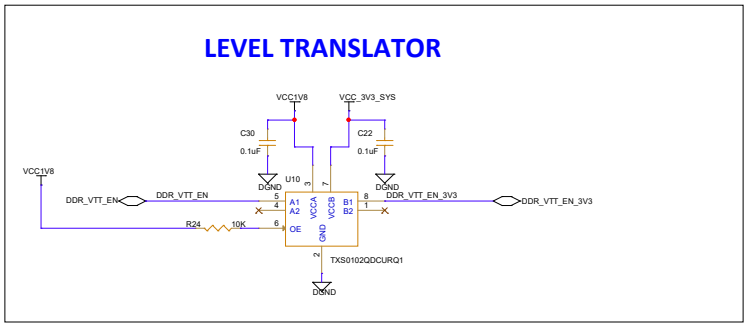
<Core Design>

Project : <Project Name>	Designed for TI by Mistral Solutions Pvt Ltd	Title: CAN & DISPLAY INTERFACE
		Size: C | Document Number: MS_TI_MAXIE_APPLICATION_CARD_SCH_REVA | Rev: E2
		Date: Wednesday, July 30, 2025 | Sheet 29 of 40

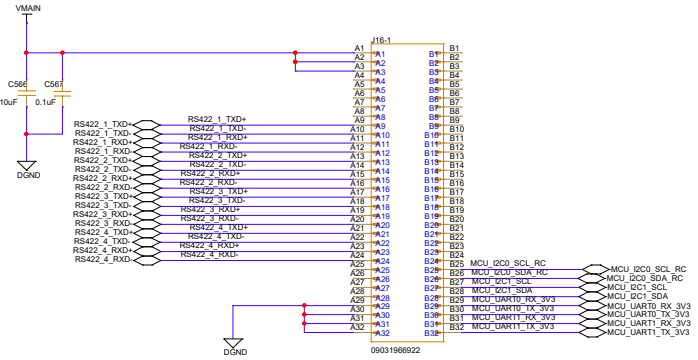
IO EXPANDER

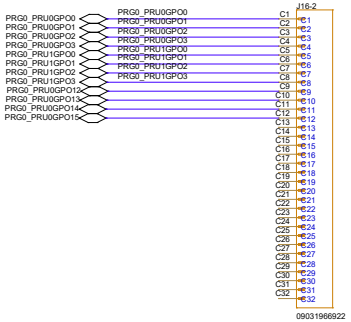


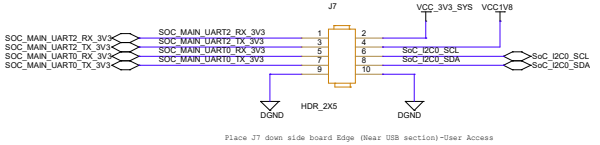
LEVEL TRANSLATOR



INPUT CONNECTOR



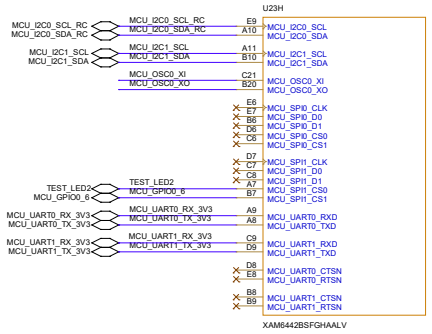


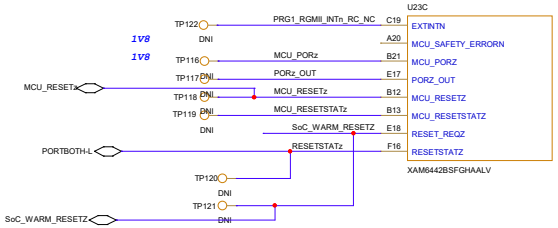


Designed for TI by Mistral Solutions Pvt Ltd

Title	IO EXPANDER		—
Size	Variant Name = <Core Design>		Rev
C			E2
Date:	Wednesday, July 30, 2025	Sheet 33 of 40	

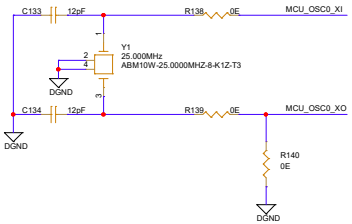
MCU_GENERAL

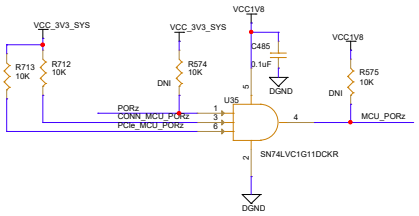




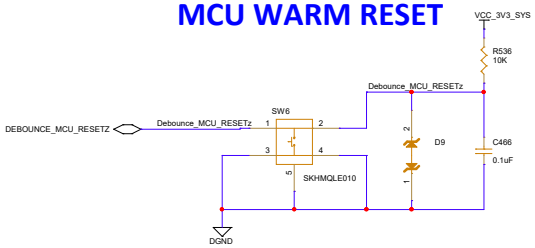
MCU_CLOCK

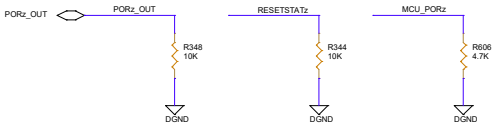
LPF Designed for 25MHz Cutoff
Have to change resistor and capacitor values accordingly





MCU WARM RESET



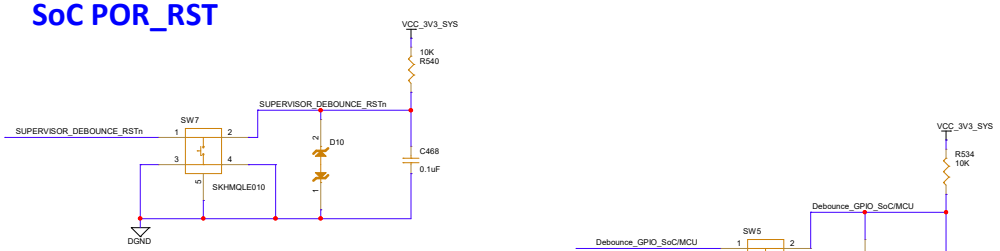


pull-down resistor on PORz_OUT is provided to keep the signal low until the processor is released from reset during the power-up seqence

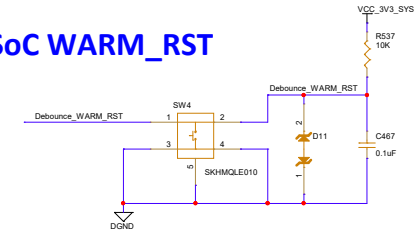
Designed for TI by Mistral Solutions Pvt Ltd

Title	MCU GENERAL & SAFETY CONNECTOR	
Size: C	Variant Name = <Core Design>	Rev: E2
Date: Friday, January 02, 2026	Sheet 34 of 40	

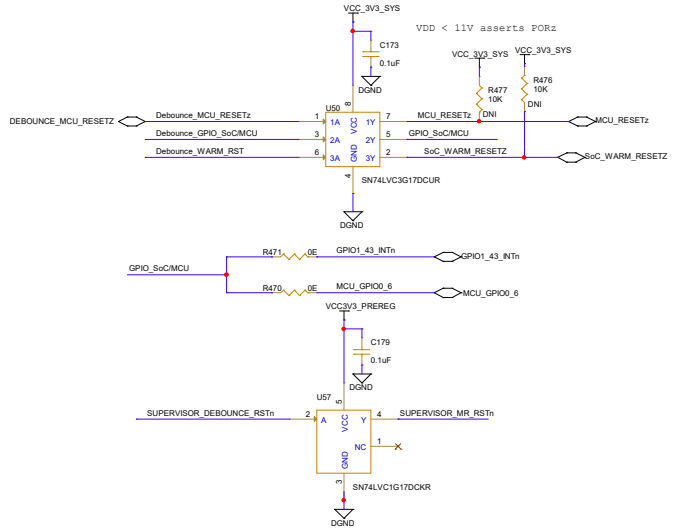
SoC POR_RST



SoC WARM_RST

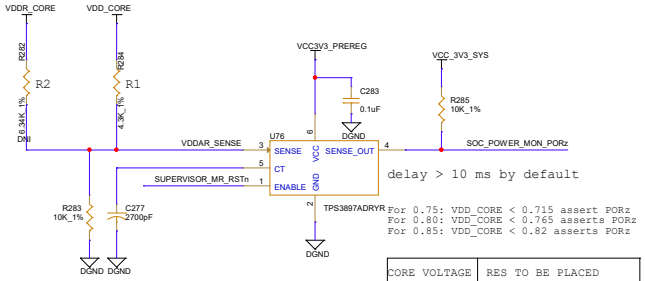


DEBOUNCE CIRCUIT



VOLTAGE SUPERVISOR

Core Voltage Monitor (VDDAR_CORE/VDD_CORE)



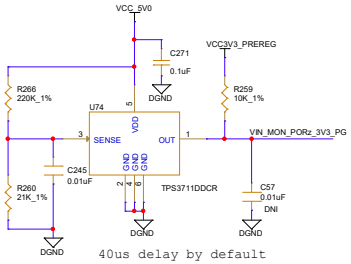
delay > 10 ms by default

For 0.75: VDD_CORE < 0.715 assert PORz
For 0.80: VDD_CORE < 0.765 asserts PORz
For 0.85: VDD_CORE < 0.82 asserts PORz

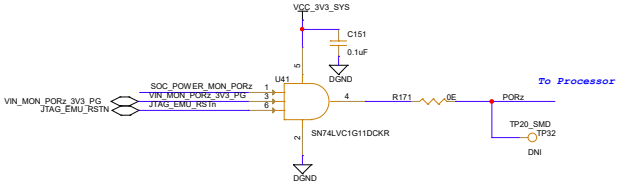
CORE VOLTAGE	RES TO BE PLACED
0.75V	R1 = 4.3K
0.80V	R2 = 5.23K

0.85V R2 = 6.34K

5V OUTPUT MONITOR (VCC_5V0)



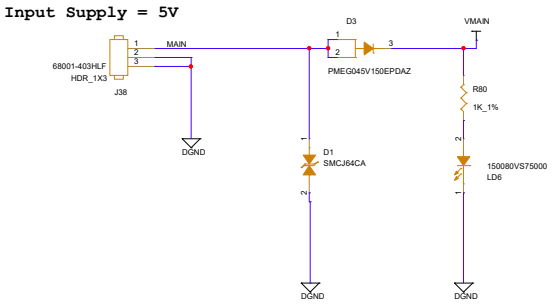
40us delay by default
VDD < 4.6 asserts PORz



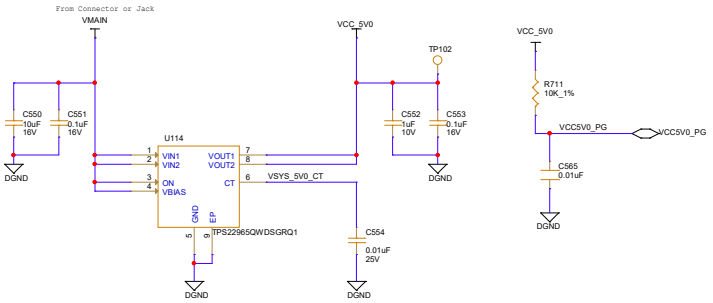
Designed for TI by Mistral Solutions Pvt Ltd

Title	DEBOUNCE CIRCUIT & VOLTAGE SUPERVISOR		
Size			Rev
C	Variant Name = <Core Design>		E2
Date:	Wednesday, July 30, 2025	Sheet 35 of 40	

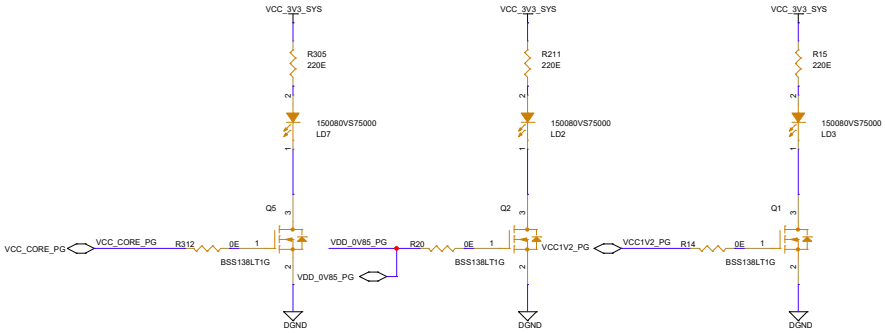
MAIN INPUT 5V DC

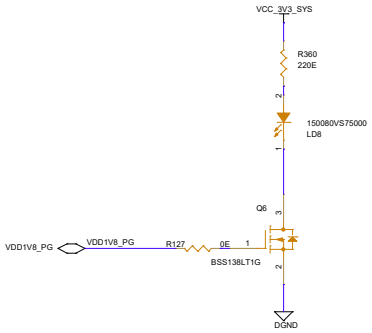


SYS MAIN INPUT 5V DC Load Switch

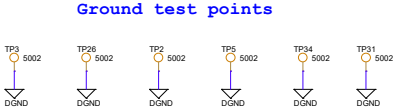


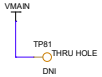
POWER INDICATION LED's





Ground test points





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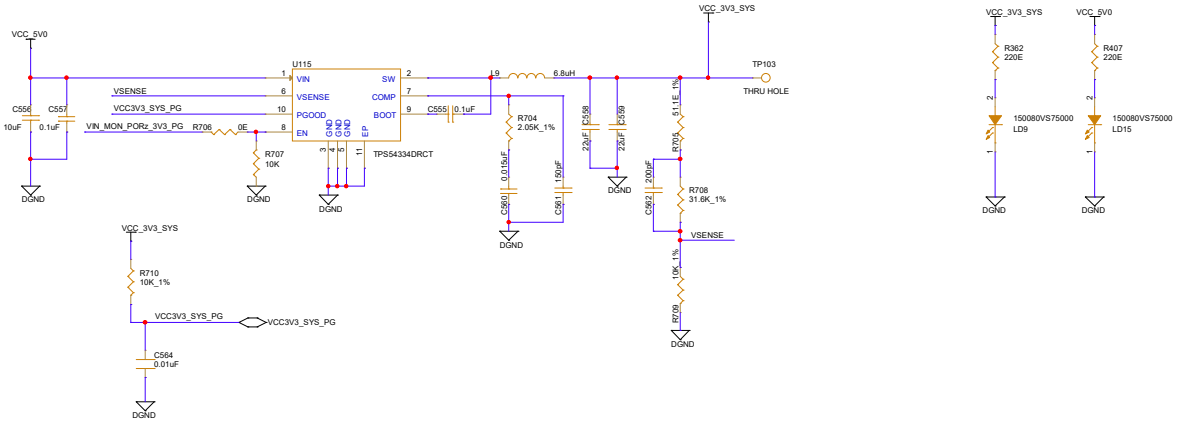
Title	MAIN 12V POWERSUPPLY	
Size: C	Variant Name = <Core Design>	Rev: E2
Date: Wednesday, July 30, 2025	Sheet 36 of 40	

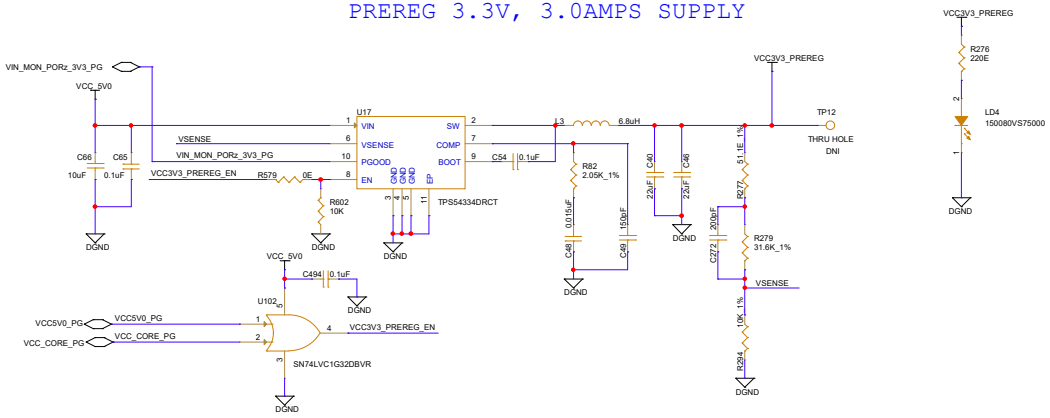
VCC3V3_SYS POWER SUPPLY

3.3V,3A SUPPLY

VCC_3V3_SYS, 3.0AMPS SUPPLY



PREREG 3.3V, 3.0AMPS SUPPLY



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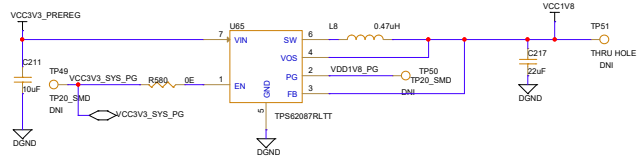
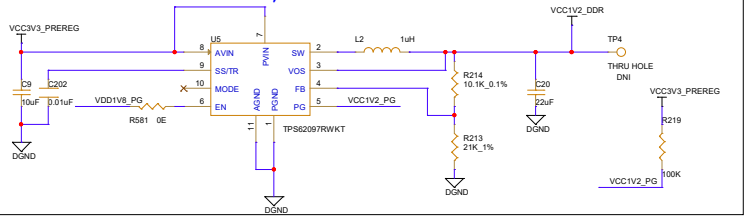
Title	DUAL & PREREG REGULATOR	
Size	Variant Name = <Core Design>	Rev
C		E2
Date:	Friday, January 02, 2026	Sheet 37 of 40

SoC POWER SUPPLY

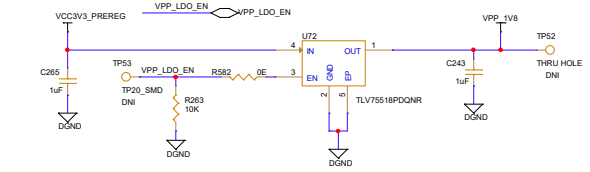
1.8V IO, 3.0AMPS SUPPLY



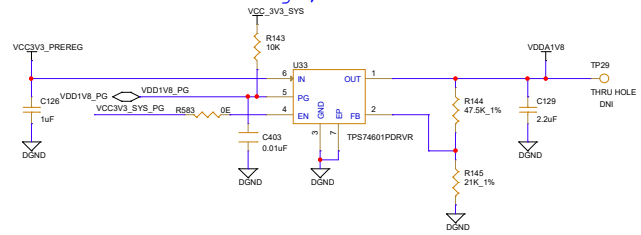
1.2V, 2.0AMPS SUPPLY



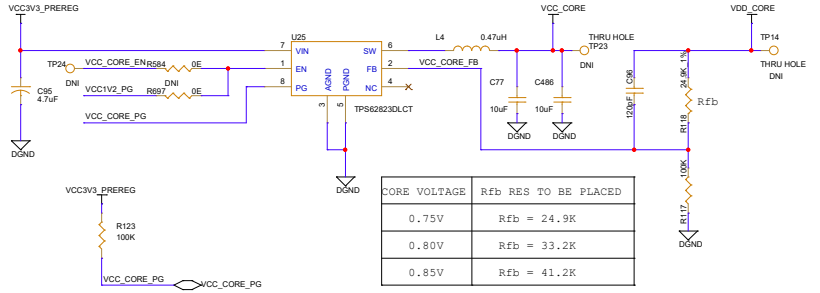
1.8V VPP, 0.15AMPS SUPPLY



1.8V Analog , 1AMPS SUPPLY

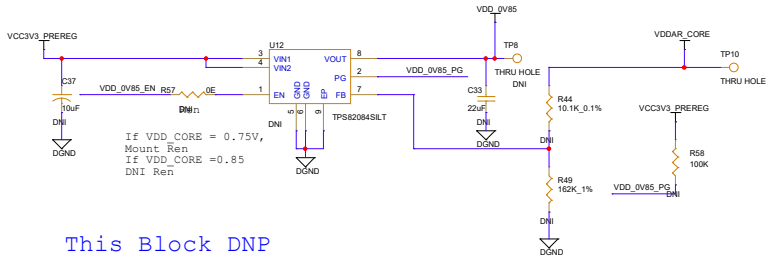


0.75 / 0.8 /0.85V, 3.0AMPS SUPPLY

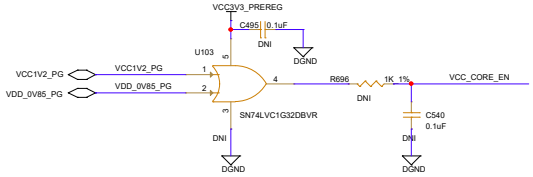


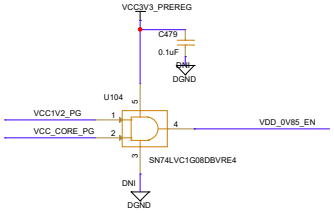
CORE VOLTAGE	Rfb RES TO BE PLACED
0.75V	Rfb = 24.9K
0.80V	Rfb = 33.2K
0.85V	Rfb = 41.2K

0.85 V, 1.5AMPS SUPPLY



This Block DNP





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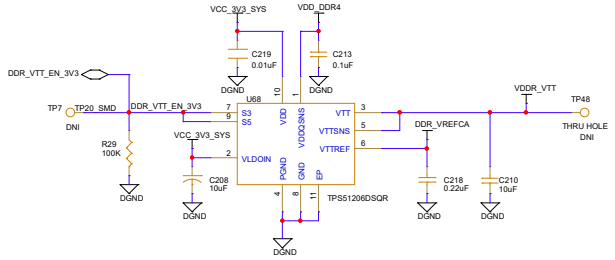
Title	SoC POWER SUPPLY	
Size: C	Variant Name = <Core Design>	Rev: E2
Date: Friday, January 02, 2026	Sheet 38 of 40	

PERIPHERAL POWER SUPPLY

TEST AUTOMATION BOARD POWER

Test Connector Power Supply Removed

VTT SUPPLY FOR DDR4



1.1V ETHERNET PHY POWER SUPPLY

Ethernet Power section removed

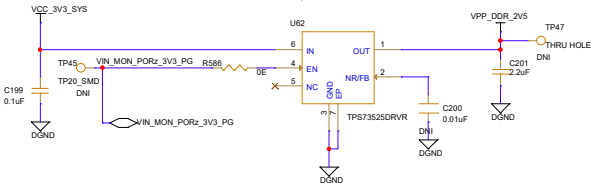
2.5V, 2.0AMPS SUPPLY

Ethernet Power section removed

1.0V ETHERNET PHY POWER SUPPLY

Ethernet Power section removed

2.5V, .5 AMPS SUPPLY



2.8V , 0.15AMPS SUPPLY

DISPLAY SECTION POWER REMOVED

VCC3V3_SYS_PG

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Title	PERIPHERAL POWER SUPPLY	
Size: C	Variant Name = <Core Design>	Rev: E2
Date: Friday, January 02, 2026	Sheet 39 of 40	

HARDWARE SCHEMATICS

ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.

2. PCB should be baked at 120 degree for 8 hours.

3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.

4. These assemblies are ESD sensitive, ESD precautions shall be observed.

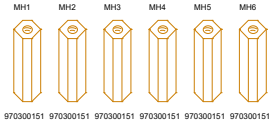
5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

6. Provide serial numbers to the assembled boards for identification.

7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

FIDUCIALS

STANDOFFs



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TEXAS INSTRUMENTS MISTRAL

Title	HARDWARE SCHEMATICS	
Size: C	Variant Name = <Core Design>	Rev: E2
Date: Wednesday, July 30, 2025	Sheet 40 of 40	