PRU-I2S Support Details

AM64 I2S:

- ICSSG details:
  - PRU0 supports 2 instances of bidirectional I2S, 16 bit, 2 channel, 48KHz
    - Both of the instances share BCLK and FS
  - PRU1 supports 2 instances of Rx only I2S, 16 bit, 48KHz
    - Both of the instances share BCLK and FS
  - BCLK sourced from outside, 1.536MHz
  - FS sourced from outside, 48KHz. Slot size is 16 bit, 1 clock advanced
  - SDI Latch after detecting rising edge of BCLK
  - SDO write after detecting falling edge of BCLK

AM263: I2S

- ICSSM details:
  - PRU0 supports 3 instances of Tx only I2S, 32 bit, 2 channel, 48KHz
    - All I2S instances share BCLK and FS
  - PRU1 supports 2 instances of Rx only I2S, 32 bit, 48KHz
    - Both of the instances share BCLK and FS
  - BCLK sourced from outside, 3.072MHz
  - FS sourced from outside, 48KHz. Slot size is 32 bit, 1 clock advanced
  - SDI Latch after detecting rising edge of BCLK
  - SDO write after detecting falling edge of BCLK

AM263x: TDM4 using PRU I2S

- ICSSM details:
  - PRU0 supports 1 Tx slave with 4 channels, 32 bit per channel
  - FSYNC (Fs) is 48kHz
  - MCLK and SCLK are the same and are 128Fs or 6.144MHz
  - SDIN must be 32bits wide to meet the minimum MCLK/SCLK (128Fs) allowed (The channels are in this order 1,2,3,4 or can be 3,4,1,2 depending the settings in register 0x03).
  - Data transmitted at every falling edge of BCLK.

AM263x: TDM6 using PRU I2S

- ICSSM details:

- PRU0 supports 1 Tx slave with 6 channels, 16 bit per channel
- FSYNC (Fs) is 16kHz
- MCLK and SCLK are the same and are 2.3MHz