TI MCU TM4C1290NCZAD：I2C Master Data Read rev2

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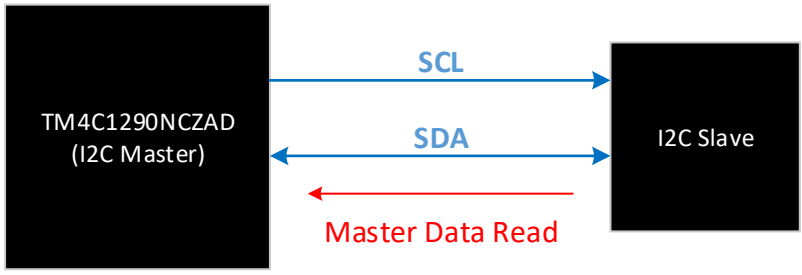
1. In the case of I2C Master Data Read with TM4C1290NCZAD

The following figure is a scheme of I2C master with TM4C1290NCZAD.

I have some questions in a case of master data read.

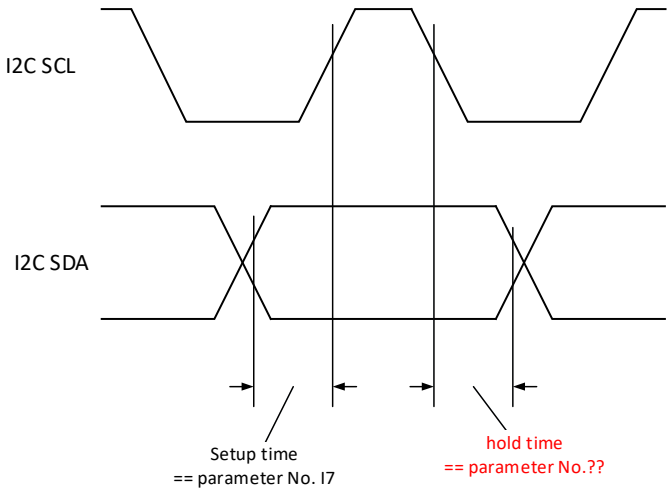


In the case of master data read on a common I2C specification (AppendixⅡ), we should get setup time & hold time met by input of master.

According to I2C timing specification of TM4C1290NCZAD (AppendixⅠ), the setup time corresponds to Parameter No.17 (18 system clock min) but I cannot figure out which Parameter No. correspond to hold time on that chart.

【 Question 3 】

Please tell me which Parameter No. correspond to hold time on I2C timing chart of TM4C1290NCZAD (AppendixⅠ).



● Appendix Ⅰ ：TM4C1290NCZAD I2C Timing Specification

Inter-Integrated Circuit (I^2C) Interface

Table 26-48. I^2C Characteristics

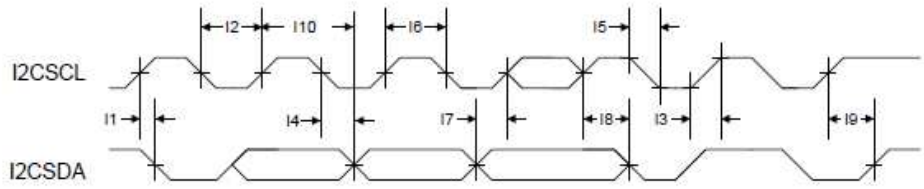
Parameter No.	Parameter	Parameter Name	Min	Nom	Max	Unit
I1[a]	T_{SCH}	Start condition hold time	36	-	-	system clocks
I2[a]	T_{LP}	Clock Low period	36	-	-	system clocks
I3[b]	T_{SRT}	I2CSCL/I2CSDA rise time (V_{IL} =0.5 V to V_{IH} =2.4 V)	-	-	(see note b)	ns
I4	T_{DH}	Data hold time (slave)	-	2	-	system clocks
		Data hold time (master)	-	7	-	system clocks
I5[c]	T_{SFT}	I2CSCL/I2CSDA fall time (V_{IH} =2.4 V to V_{IL} =0.5 V)	-	9	10	ns
I6[a]	T_{HT}	Clock High time	24	-	-	system clocks
I7	T_{DS}	Data setup time	18	-	-	system clocks
I8[a]	T_{SCSR}	Start condition setup time (for repeated start condition only)	36	-	-	system clocks
I9[a]	T_{SCS}	Stop condition setup time	24	-	-	system clocks
I10	T_{DV}	Data Valid (slave)	-	2	-	system clocks
		Data Valid (master)	-	(6 * (1 + TPR)) + 1	-	system clocks

a. Values depend on the value programmed into the TPR bit in the **I^2C Master Timer Period (I2CMTPR)** register; a TPR programmed for the maximum I2CSCL frequency (TPR=0x2) results in a minimum output timing as shown in the table above. The I^2C interface is designed to scale the actual data transition time to move it to the middle of the I2CSCL Low period. The actual position is affected by the value programmed into the TPR; however, the numbers given in the above values are minimum values.

b. Because I2CSCL and I2CSDA operate as open-drain-type signals, which the controller can only actively drive low, the time I2CSCL or I2CSDA takes to reach a high level depends on external signal capacitance and pull-up resistor values.

c. Specified at a nominal 50 pF load.

Figure 26-33. I^2C Timing



● Appendix Ⅱ ： Example of Common I2C Timing Specification

*Unless otherwise specified, GND = 0 V , V_{DD}= 1.6 V ~ 5.5 V , Ta = -40°C ~ +85°C

Item	Symbol	Standard-Mode (f_{SCL}=100kHz)		Fast-Mode (f_{SCL}=400kHz)		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}		100		400	kHz
Start condition setup time	$t_{SU;STA}$	4.7		0.6		µs
Start condition hold time	$t_{HD;STA}$	4.0		0.6		µs
Data setup time	$t_{SU;DAT}$	250		100		ns
Data hold time	$t_{HD;DAT}$	0		0		ns
Stop condition setup time	$t_{SU;STO}$	4.0		0.6		µs
Bus idle time between start condition and stop condition	t_{BUF}	4.7		1.3		µs
Time when SCL = "L"	t_{LOW}	4.7		1.3		µs
Time when SCL = "H"	t_{HIGH}	4.0		0.6		µs
Rise time for SCL and SDA	t_r		1.0		0.3	µs
Fall time for SCL and SDA	t_f		0.3		0.3	µs
Allowable spike time on bus	t_{SP}		50		50	ns

• Timing chart