

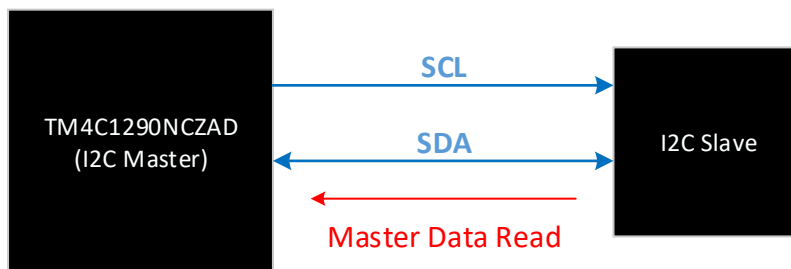
# TI MCU TM4C1290NCZAD : I2C Master Data Read rev3

EIZO Co. 2019.12.23

## 1. In the case of I2C Master Data Read with TM4C1290NCZAD

The following figure is a scheme of I2C master with TM4C1290NCZAD.

I have some questions in a case of master data read.

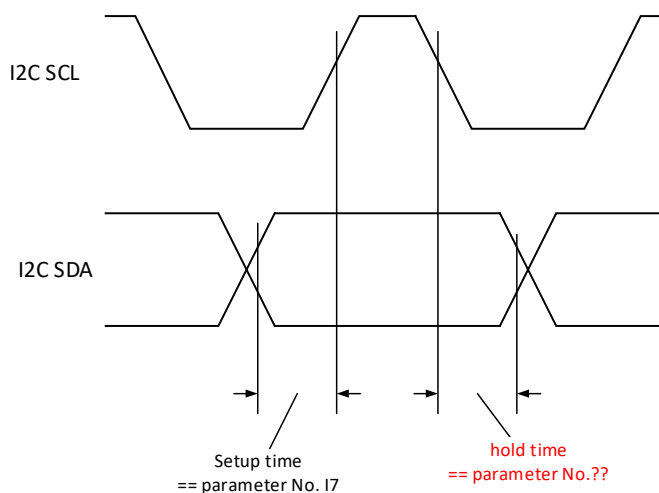


In the case of master data read on a common I2C specification (Appendix II), we should get setup time & hold time met by input of master.

According to I2C timing specification of TM4C1290NCZAD (Appendix I), the setup time corresponds to Parameter No.17 (18 system clock min) but I cannot figure out which Parameter No. correspond to hold time on that chart.

### 【 Question 3 】

Please tell me which Parameter No. correspond to hold time on I2C timing chart of TM4C1290NCZAD (Appendix I).



【 Answer 3 】

The standard data hold time of SDA is from spec I4. To get a more specific answer you need to use a specific example. What frequency is the system clock and what is the targeted I2C speed?

Best Regards, Bob Crosby

【 Question 4 】

For our example below.

*I2C Standard Mode*

$$SCL\_PERIOD = 2 \times (1 + TIMER\_PRD) \times (SCL\_LP + SCL\_HP) \times CLK\_PRD$$

$$CLK\_PRD = 8.33 \text{ ns} \quad \text{※system clock} = 120 \text{ MHz}$$

$$TIMER\_PRD = 66 \text{ (DEC)}$$

$$SCL\_LP = 6 \quad \text{※fixed}$$

$$SCL\_HP = 4 \quad \text{※fixed}$$

*yields a SCL Frequency of*

$$1/SCL\_PERIOD = 89.55 \text{ kHz}$$

In this case, How many system clocks needed for minimum hold time ?

Please tell me a method to derive the minimum hold time.

● Appendix I : TM4C1290NCZAD I2C Timing Specification

## Inter-Integrated Circuit (I<sup>2</sup>C) Interface

Table 26-48. I<sup>2</sup>C Characteristics

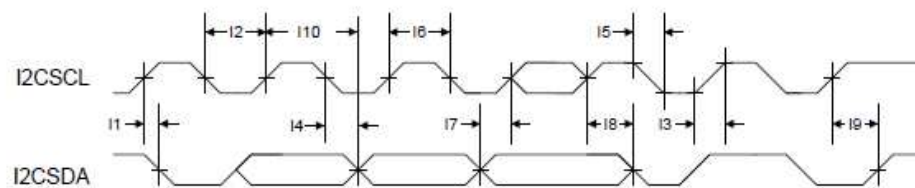
Parameter No.	Parameter	Parameter Name	Min	Nom	Max	Unit
11 <sup>a</sup>	T <sub>SCH</sub>	Start condition hold time	36	-	-	system clocks
12 <sup>a</sup>	T <sub>LP</sub>	Clock Low period	36	-	-	system clocks
13 <sup>b</sup>	T <sub>SRT</sub>	I2CSCL/I2CSDA rise time (V <sub>IL</sub> =0.5 V to V <sub>IH</sub> =2.4 V)	-	-	(see note b)	ns
14	T <sub>DH</sub>	Data hold time (slave)	-	2	-	system clocks
		Data hold time (master)	-	7	-	system clocks
15 <sup>c</sup>	T <sub>SFT</sub>	I2CSCL/I2CSDA fall time (V <sub>IH</sub> =2.4 V to V <sub>IL</sub> =0.5 V)	-	9	10	ns
16 <sup>a</sup>	T <sub>HT</sub>	Clock High time	24	-	-	system clocks
17	T <sub>DS</sub>	Data setup time	18	-	-	system clocks
18 <sup>a</sup>	T <sub>SCSR</sub>	Start condition setup time (for repeated start condition only)	36	-	-	system clocks
19 <sup>a</sup>	T <sub>SCS</sub>	Stop condition setup time	24	-	-	system clocks
110	T <sub>DV</sub>	Data Valid (slave)	-	2	-	system clocks
		Data Valid (master)	-	(6 * (1 + TPR)) + 1	-	system clocks

a. Values depend on the value programmed into the TPR bit in the I<sup>2</sup>C Master Timer Period (I2CMTPR) register; a TPR programmed for the maximum I2CSCL frequency (TPR=0x2) results in a minimum output timing as shown in the table above. The I<sup>2</sup>C interface is designed to scale the actual data transition time to move it to the middle of the I2CSCL Low period. The actual position is affected by the value programmed into the TPR; however, the numbers given in the above values are minimum values.

b. Because I2CSCL and I2CSDA operate as open-drain-type signals, which the controller can only actively drive low, the time I2CSCL or I2CSDA takes to reach a high level depends on external signal capacitance and pull-up resistor values.

c. Specified at a nominal 50 pF load.

Figure 26-33. I<sup>2</sup>C Timing



● Appendix II : Example of Common I2C Timing Specification

\*Unless otherwise specified, GND = 0 V, VDD = 1.6 V ~ 5.5 V, Ta = -40°C ~ +85°C

Item	Symbol	Standard-Mode (fSCL=100kHz)		Fast-Mode (fSCL=400kHz)		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	fSCL		100		400	kHz
Start condition setup time	tSU;STA	4.7		0.6		μs
Start condition hold time	tHD;STA	4.0		0.6		μs
Data setup time	tSU;DAT	250		100		ns
Data hold time	tHD;DAT	0		0		ns
Stop condition setup time	tSU;STO	4.0		0.6		μs
Bus idle time between start condition and stop condition	tBUF	4.7		1.3		μs
Time when SCL = "L"	tLOW	4.7		1.3		μs
Time when SCL = "H"	tHIGH	4.0		0.6		μs
Rise time for SCL and SDA	tr		1.0		0.3	μs
Fall time for SCL and SDA	tf		0.3		0.3	μs
Allowable spike time on bus	tSP		50		50	ns

• Timing chart

