TI MCU TM4C1290NCZAD：I2C Master Data Read rev4

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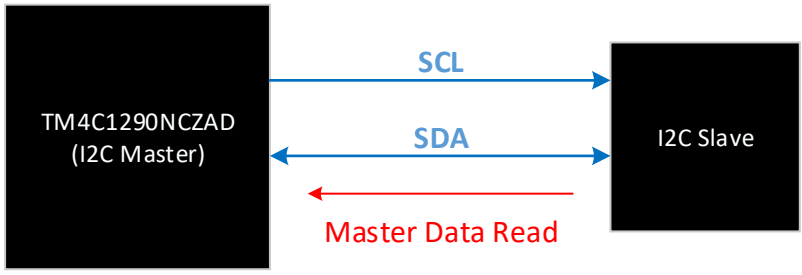
1. In the case of I2C Master Data Read with TM4C1290NCZAD

The following figure is a scheme of I2C master with TM4C1290NCZAD.

I have some questions in a case of master data read.

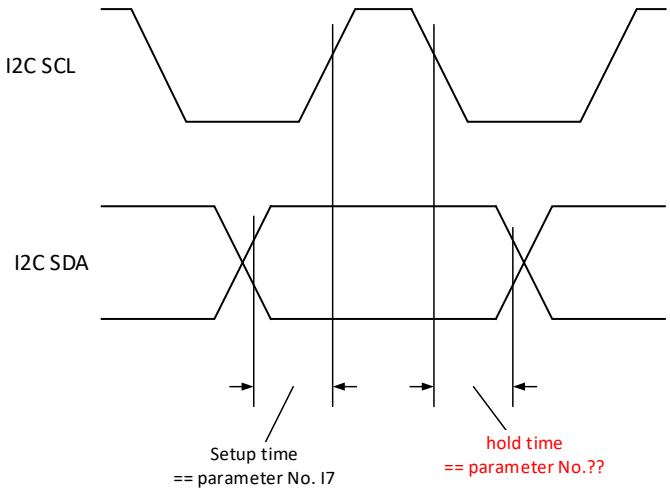


In the case of master data read on a common I2C specification (AppendixⅡ), we should get setup time & hold time met by input of master.

According to I2C timing specification of TM4C1290NCZAD (AppendixⅠ), the setup time corresponds to Parameter No.17 (18 system clock min) but I cannot figure out which Parameter No. correspond to hold time on that chart.

【 Question 3 】

Please tell me which Parameter No. correspond to hold time on I2C timing chart of TM4C1290NCZAD (AppendixⅠ).



【 Answer 3 】

The standard data hold time of SDA is from spec I4. To get a more specific answer you need to use a specific example. What frequency is the system clock and what is the targeted I2C speed?

Best Regards, Bob Crosby

【 Question 4 】

For our example below.

I2C Standard Mode

SCL_PERIOD = 2×(1 + TIMER_PRD)×(SCL_LP + SCL_HP)×CLK_PRD

CLK_PRD = 8.33 ns ※system clock = 120 MHz

TIMER_PRD = 66 (DEC)

SCL_LP = 6 ※fixed

SCL_HP = 4 ※fixed

yields a SCL Frequency of

1/SCL_PERIOD = 89.55 kHz

In this case, How many system clocks needed for minimum hold time ?

Please tell me a method to derive the minimum hold time.

【 Answer 4 】

When acting as a master, the I2C provides a 7 system clock hold time or 7 * 8.33nS = 58.3nS. As a slave it provides a 2 system clock hold time or 16.66nS. **When acting as a master reading data from a slave, 0ns hold time is required as the data is sampled in the middle of the high period of SCL.**

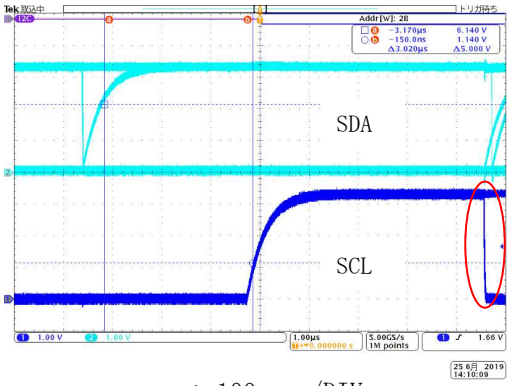
Best Regards, Bob Crosby

【 Question 5 】

One more Question we have.

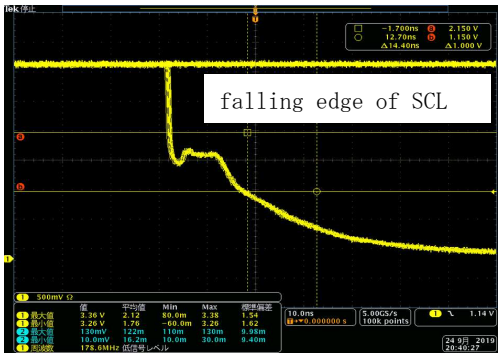
The following figure is a waveform of our application when acting as a master reading data from a slave.

This application meets the timing specification of 0ns hold time, but the falling edge has some glitch in input threshold range of TM4C1290NCZAD as below.



x-axes : 100 μs/DIV

y-axes : 1.0 V/DIV



x-axes : 10.0 ns/DIV

y-axes : 500 mV/DIV

I wonder if a monotonicity of the falling edge of SCL should be needed when a master reading data from a slave ? or “don’t care”, and no problem?

Please tell me if TM4C1290NCZAD has an allowable spike time on bus?

【 Answer 5 】

The reflection on SCL is not likely a problem for the TM4C129 as it is the master and it is driving the clock. If bad enough it could be a problem for the slave. Treat SCL as a transmission line. If you have not already done so, put the pullup resistor at the slave end of the SCL line to help terminate it. You might even add an AC coupled termination at the slave end. How long are your SDA and SCL lines? Are they PCB traces or wires? What value of pullup are you using and where is it placed?

Best Regards, Bob Crosby

【 Question 6 】

Is there an objective criterion of allowable spike time of TM4C129?

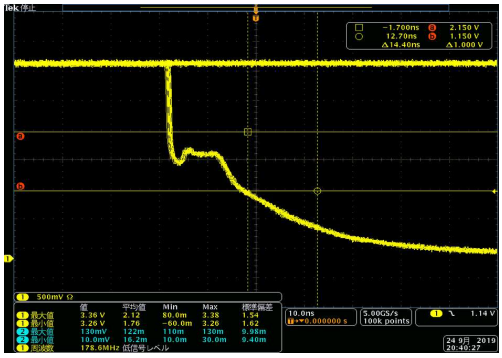
I will close this issue if you could answer this question in yes or no.

If your answer is 'YES', let me know the criterion. Then I will try to meet it you answered.

If your answer is 'NO', I will try to modify the falling edge of SCL to get monotonicity in a range of input threshold of TM4C129 as followings.

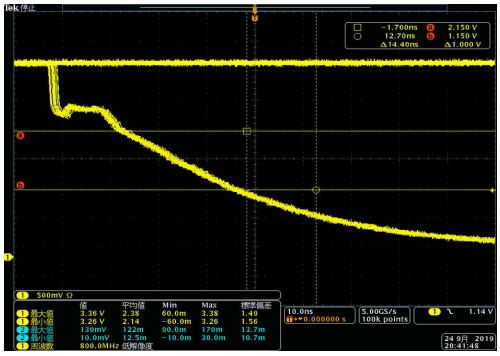
● Method1 : adjustment of drive current on TM4C129 port

Example



Drive Current 4.0 mA

Monotonicity Bad!

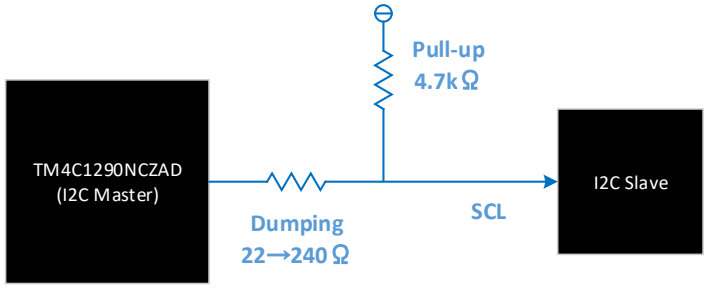


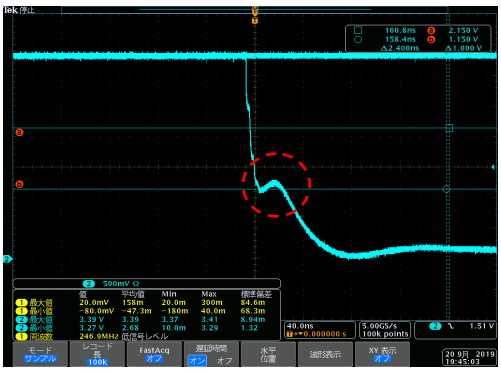
Drive Current 2.0 mA

Monotonicity OK

● Method2 : adjustment of dumping resister placed on SCL output of TM4C129

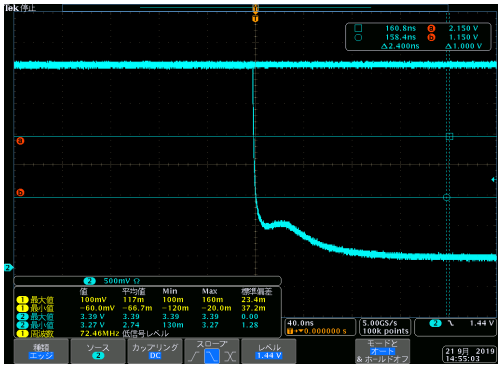
Example





Dumping resister 22Ω

Monotonicity Bad!



Dumping resister 240Ω

Monotonicity OK

● Appendix Ⅰ ：TM4C1290NCZAD I2C Timing Specification

Inter-Integrated Circuit (I^2C) Interface

Table 26-48. I^2C Characteristics

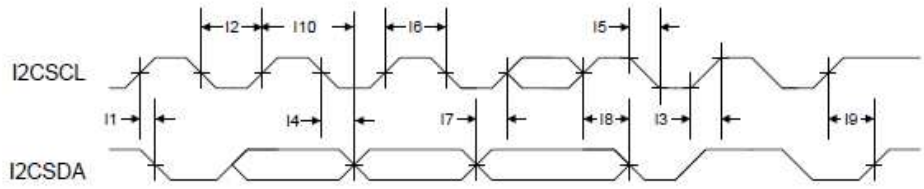
Parameter No.	Parameter	Parameter Name	Min	Nom	Max	Unit
I1[a]	T_{SCH}	Start condition hold time	36	-	-	system clocks
I2[a]	T_{LP}	Clock Low period	36	-	-	system clocks
I3[b]	T_{SRT}	I2CSCL/I2CSDA rise time (V_{IL} =0.5 V to V_{IH} =2.4 V)	-	-	(see note b)	ns
I4	T_{DH}	Data hold time (slave)	-	2	-	system clocks
		Data hold time (master)	-	7	-	system clocks
I5[c]	T_{SFT}	I2CSCL/I2CSDA fall time (V_{IH} =2.4 V to V_{IL} =0.5 V)	-	9	10	ns
I6[a]	T_{HT}	Clock High time	24	-	-	system clocks
I7	T_{DS}	Data setup time	18	-	-	system clocks
I8[a]	T_{SCSR}	Start condition setup time (for repeated start condition only)	36	-	-	system clocks
I9[a]	T_{SCS}	Stop condition setup time	24	-	-	system clocks
I10	T_{DV}	Data Valid (slave)	-	2	-	system clocks
		Data Valid (master)	-	(6 * (1 + TPR)) + 1	-	system clocks

a. Values depend on the value programmed into the TPR bit in the **I^2C Master Timer Period (I2CMTPR)** register; a TPR programmed for the maximum I2CSCL frequency (TPR=0x2) results in a minimum output timing as shown in the table above. The I^2C interface is designed to scale the actual data transition time to move it to the middle of the I2CSCL Low period. The actual position is affected by the value programmed into the TPR; however, the numbers given in the above values are minimum values.

b. Because I2CSCL and I2CSDA operate as open-drain-type signals, which the controller can only actively drive low, the time I2CSCL or I2CSDA takes to reach a high level depends on external signal capacitance and pull-up resistor values.

c. Specified at a nominal 50 pF load.

Figure 26-33. I^2C Timing



● Appendix Ⅱ ： Example of Common I2C Timing Specification

*Unless otherwise specified, GND = 0 V , V_{DD}= 1.6 V ~ 5.5 V , Ta = -40°C ~ +85°C

Item	Symbol	Standard-Mode (f_{SCL}=100kHz)		Fast-Mode (f_{SCL}=400kHz)		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}		100		400	kHz
Start condition setup time	$t_{SU;STA}$	4.7		0.6		µs
Start condition hold time	$t_{HD;STA}$	4.0		0.6		µs
Data setup time	$t_{SU;DAT}$	250		100		ns
Data hold time	$t_{HD;DAT}$	0		0		ns
Stop condition setup time	$t_{SU;STO}$	4.0		0.6		µs
Bus idle time between start condition and stop condition	t_{BUF}	4.7		1.3		µs
Time when SCL = "L"	t_{LOW}	4.7		1.3		µs
Time when SCL = "H"	t_{HIGH}	4.0		0.6		µs
Rise time for SCL and SDA	t_r		1.0		0.3	µs
Fall time for SCL and SDA	t_f		0.3		0.3	µs
Allowable spike time on bus	t_{SP}		50		50	ns

• Timing chart