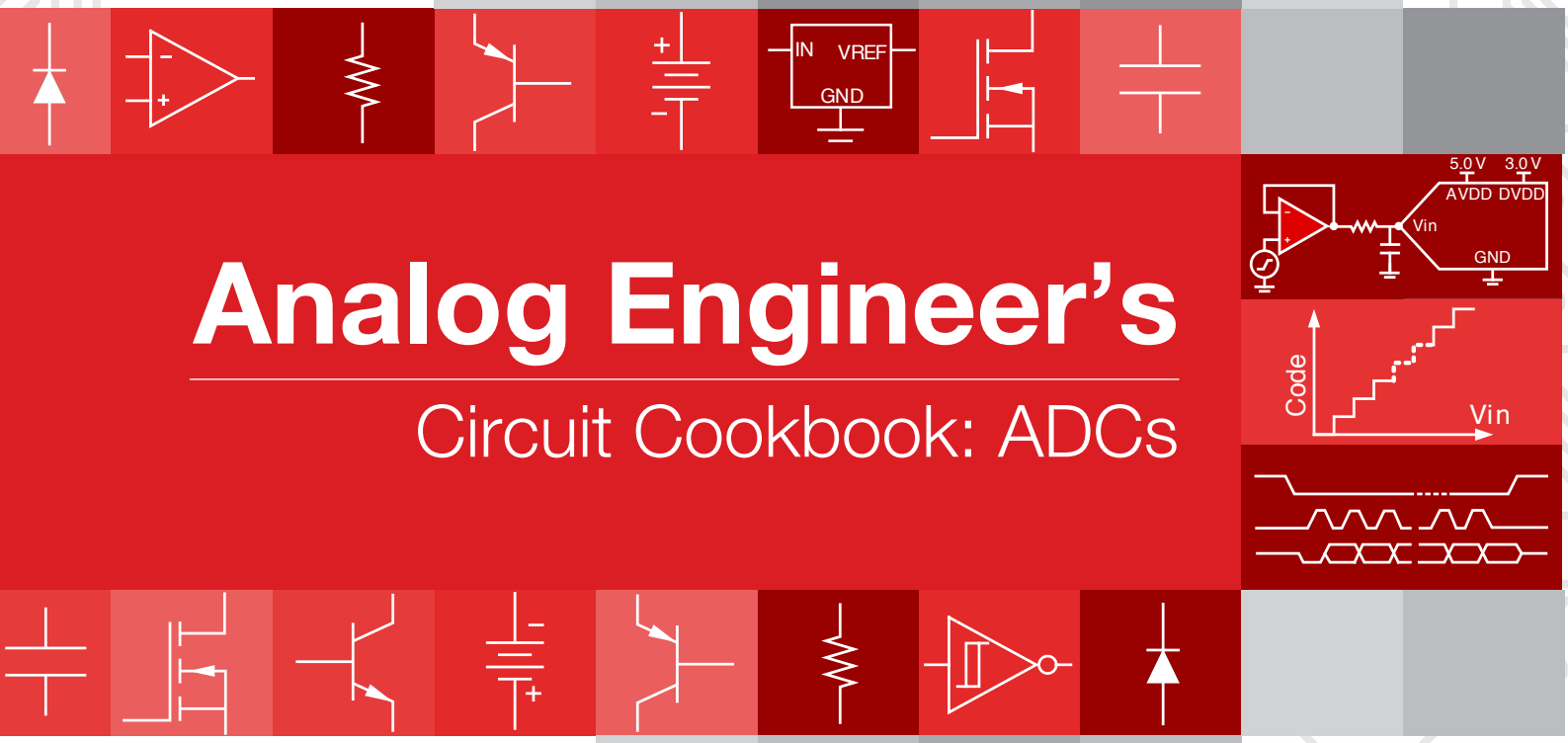

Analog Engineer's

Circuit Cookbook: ADCs

TEXAS INSTRUMENTS

Analog Engineer's Circuit Cookbook: ADCs

First Edition
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Edited by:

Art Kay, Luis Chioye and Dale Li

Special thanks for technical contribution:

Peggy Liska

Cynthia Sosa

Reed Kaczmarek

Bryan McKay

Manuel Chavez

Analog Engineer's Circuit Cookbook: ADCs

(First Edition)

Message from the editors:

The *Analog Engineer's Circuit Cookbook*: *ADCs* provides analog-to-digital converter (ADC) sub-circuit ideas that can be quickly adapted to meet your specific system needs. Each circuit is presented as a "definition-by-example." They include step-by-step instructions, like a recipe, with formulas enabling you to adapt the circuit to meet your design goals. Additionally, all circuits are verified with SPICE simulations and include links to the corresponding TINA-TI™ SPICE circuits.

We've provided at least one recommended ADC for each circuit, but you can swap it with another device if you've found one that's a better fit for your design. You can search our large portfolio of ADCs at www.ti.com/ADCs.

Our circuits require a basic understanding of amplifier and data converter concepts. If you're new to data converter design, we highly recommend completing our TI Precision Labs (TIPL) training series. TIPL includes courses on introductory topics, such as device architecture, as well as advanced, application-specific problem-solving, using both theory and practical knowledge. Check out our curriculum for op amps, ADCs and more at: www.ti.com/precisionlabs.

We plan to update this e-book with new ADC circuit building blocks and encourage you to see if your version is the latest at www.ti.com/circuitcookbooks. If you have feedback on any of our existing circuits or would like to request additional ADC circuits for the next edition of this e-book, please contact us at adccookbook@list.ti.com.

We hope you find our collection of ADC circuits helpful in developing your designs!

Additional resources to explore

TI Precision Labs
ti.com/precisionlabs
- On-demand courses and tutorials ranging from introductory to advanced concepts that focus on application-specific problem solving
- Hands-on labs and evaluation modules (EVM) available
  - TIPL Op Amps experimentation platform, ti.com/TIPL-amp-evm
  - TIPL SAR ADC experimentation platform, ti.com/TIPL-adc-evm

Analog Engineer's Pocket Reference
ti.com/analogrefguide
- PCB, analog and mixed-signal design formulae; includes conversions, tables and equations
- e-book, iTunes app and hardcopy available

***The Signal* e-book**
ti.com/signalbook
- Short, bite-sized lessons on on op-amp design topics, such as offset voltage, input bias current, stability, noise and more

Analog Wire Blog
ti.com/analogwire
- Technical blogs written by analog experts that include tips, tricks and design techniques

TI Designs
ti.com/tidesigns
- Ready-to-use reference designs with theory, calculations, simulations schematics, PCB files and bench test results

ADC Parametric Quick Search
ti.com/ADC-search
- Find your next precision or high-speed ADC

DIY Amplifier Circuit Evaluation Module (DIYAMP-EVM)
ti.com/DIYAMP-EVM
- Single-channel circuit evaluation module providing SC70, SOT23 and SOIC package options in 12 popular amplifier configurations

Dual-Channel DIY Amplifier Circuit Evaluation Module (DUAL-DIYAMP-EVM)
ti.com/dual-diyamp-evm
- Dual-channel circuit evaluation module in an SOIC-8 package with 10 popular amplifier configurations

TINA-TI simulation software
ti.com/tool/tina-ti
- Complete SPICE simulator for DC, AC, transient and noise analysis
- Includes schematic entry and post-processor for waveform math

Analog Engineer's Calculator
ti.com/analogcalc
- ADC and amplifier design tools, noise and stability analysis, PCB and sensor tools

TI E2E™ Community
ti.com/e2e
- Support forums for all TI products

Table of Contents

Driving a SAR ADC Directly Without a Front-End Buffer Circuit (Low-Power, Low-Sampling-Speed DAQ)

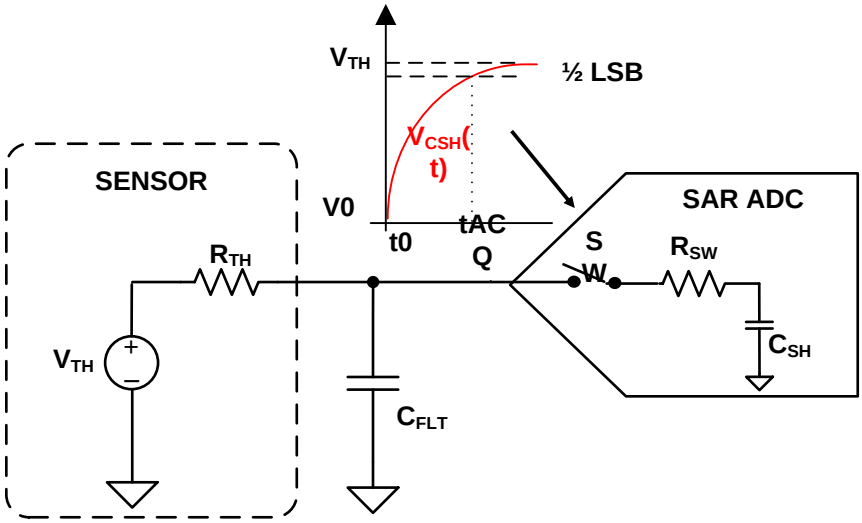
Abhijeet Godbole

Design Description

This design explains how sensor outputs can be directly interfaced with a SAR ADC input. In applications such as *Environmental Sensors*, *Gas Detectors*, and *Smoke or Fire Detectors*, the input is very slow-moving and the sensor output voltage is sampled at fairly slower speeds (10ksps or so). In such or similar systems, the sensor output can be directly interfaced with the SAR ADC input without the need for a driver amplifier to achieve a small form-factor, low-cost design.

Interfacing Sensor Output Directly to a SAR ADC

The following figure shows a typical application diagram for interfacing a sensor directly to a SAR ADC input without the use of a driver amplifier. The sensor block highlights the Thevenin equivalent of a sensor output. Voltage source, V_{TH}, is the Thevenin-equivalent voltage and source resistance R_{TH} is the Thevenin-equivalent impedance. Most sensor data sheets provide the Thevenin model of the sensor from which the value of the series impedance can be easily calculated.



Specifications

Parameter	Calculated	Simulated	Measured
Transient ADC Input Settling Error	< 0.5LSB < 100.5µV	36.24µV	N/A
Step Input Full Scale Range	3.15V	3.15V	3.14978
Input Source Impedance (R_{TH})	10kΩ	10kΩ	10.01kΩ
Filter Capacitor Value (C_{FLT})	680pF	680pF	N/A
ADC Sampling Speed	10ksps	10ksps	10ksps

Design Note

1. Determine source impedance of input signal. Calculate the RC time constant of the input source impedance and filter capacitor (known value).
2. Determine the minimum acquisition time required for the input signal to settle for a given source impedance and the filter capacitor combination.
3. Select COG capacitors to minimize distortion.
4. Use 0.1% 20ppm/°C film resistors or better for good gain drift and to minimize distortion.

Component Selection for ADC Input Settling

SAR ADCs can be directly interfaced with sensors when the analog input source is capable of driving the switched capacitor load of a SAR ADC and settling the analog input signal to within ½ of an LSB within the acquisition time of the SAR ADC. To achieve this, the external RC filter (R_{TH} and C_{FLT}) must settle within the acquisition time (t_{ACQ}) of the ADC. The relationship between the ADC acquisition time and RC time constant of the external filter is:

$$t_{ACQ} \geq k \cdot \tau_{FLT}$$

where

- $\tau_{FLT} = R_{TH} \cdot C_{FLT}$
- k is the single pole time constant for N bit ADC

The following design example values are given in the table on page 1:

R_{TH} = 10kΩ

C_{FLT} = 680pF

K = 11 (Single pole time constant multiplier for 14-bit ADC) – More information is found on page 96 and page 97 of the *Analog Engineer's Pocket Reference*.

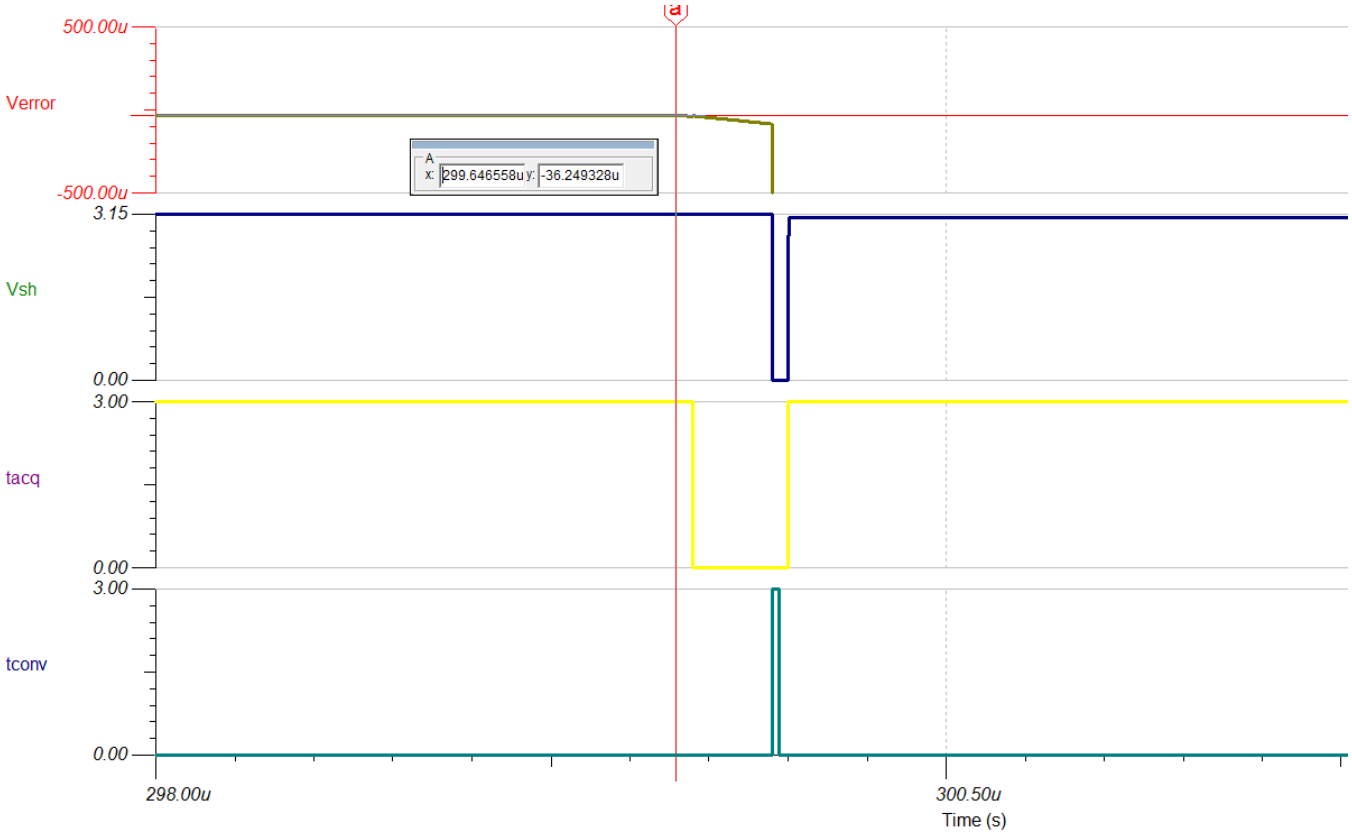
Minimum acquisition time required for proper settling is calculated using this equation:

$$t_{ACQ} \geq 11 \cdot 10k\Omega \cdot 680pF = 74.80\mu s$$

For more information on SAR ADCs and front end design for SAR ADCs, refer to *Introduction to SAR ADC Front-End Component Selection*.

Transient Input Settling Simulation using TI-TINA

The following figure shows the settling of an *ADS7056* ADC given a 3.15-V DC input signal. This type of simulation shows that the sample and hold kickback circuit is properly selected. Refer to *Refine the Rfilt and Cfilt Values* in the *TI Precision Labs - ADCs* training video series for detailed theory on this subject.



Increasing Acquisition Time of SAR ADC for Input Signal Settling

The acquisition time of a SAR ADC can be increased by reducing the throughput in the following ways:

1. Reducing the SCLK frequency to reduce the throughput.
2. Keeping the SCLK fixed at the highest permissible value and increasing the CS high time.

The following table lists the acquisition time for the previous two cases for the *ADS7056* SAR ADC operating at 10ksps throughput (tcycle = 100µs). Case 2 provides a longer acquisition time for the input signal to settle because of the increased frequency of the SCLK given a fixed conversion and cycle time.

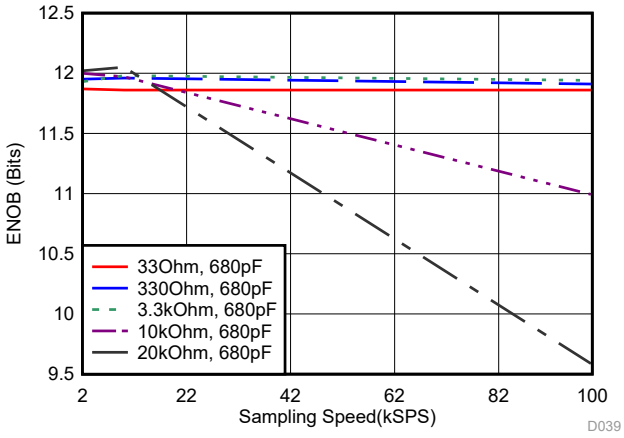
Case	SCLK	t_{cycle}	Conversion Time ($18 \cdot t_{SCLK}$)	Acquisition Time ($t_{cycle} - t_{conv}$)
1	0.24MHz	100µs	74.988µs	25.01µs
2	60MHz	100µs	0.3µs	99.70µs

The following table shows a performance comparison between an 8-, 10-, 12-, and 14-bit ADC with respect to sampling speed and effective number of bits (ENOB) when a sensor output with an output impedance of 10kΩ is directly interfaced with the ADC input. As expected, the ENOB degrades with higher sampling rates because the acquisition time decreases.

Sampling Speed (ksps)	ADS7040 (8-bit ADC) ENOB (R_{TH} = 10kΩ, C_{FLT} = 1.5nF)	ADS7041 (10-bit ADC) ENOB (R_{TH} = 10kΩ, C_{FLT} = 1.5nF)	ADS7042 (12-bit ADC) ENOB (R_{TH} = 10kΩ, C_{FLT} = 1.5nF)	ADS7056 (14-bit ADC) ENOB (R_{TH} = 10kΩ, C_{FLT} = 680pF)
10	7.93	9.87	10	12.05
100	7.92	9.85	9.97	10.99
500	7.88	9.68	9.95	8.00

Performance Achieved at Different Throughput Rates with Different Source impedance

The following figure provides the ENOB achieved from the ADS7056 at different throughout with different input impedances. Note that all the results for were taken without an ADC driver amplifier.



Design Featured Devices:

Device	Key Features	Link	Other Possible Devices
ADS7040	8-bit resolution, SPI, 1-Msps sample rate, single-ended input, AVDD/Vref input range 1.6V to 3.6V.	http://www.ti.com/product/ADS7040	Similar Devices
ADS7041	10-bit resolution, SPI, 1Msps sample rate, single-ended input, AVDD/Vref input range 1.6V to 3.6V.	http://www.ti.com/product/ADS7041	Similar Devices
ADS7042	12-bit resolution, SPI, 1-Msps sample rate, single-ended input, AVDD/Vref input range 1.6V to 3.6V.	http://www.ti.com/product/ADS7042	Similar Devices
ADS7056	14-bit resolution, SPI, 2.5-Msps sample rate, single-ended input, AVDD/Vref input range 1.6V to 3.6V.	http://www.ti.com/product/ADS7056	Similar Devices

NOTE: The ADS7042 and ADS7056 use the AVDD as the reference input. A high-PSRR LDO, such as the TPS7A47, should be used as the power supply.

Link to Key files

Source Files for Interfacing Sensor Output Directly with SAR ADCs (http://www.ti.com/lit/zip/sbac178)

For direct support from TI Engineers use the E2E community:

e2e.ti.com

Other Links

www.ti.com/adcs

www.ti.com/opamp

Low-Power Sensor Measurements: 3.3-V, 1-ksps, 12-bit, Single-Ended, Dual-Supply Circuit

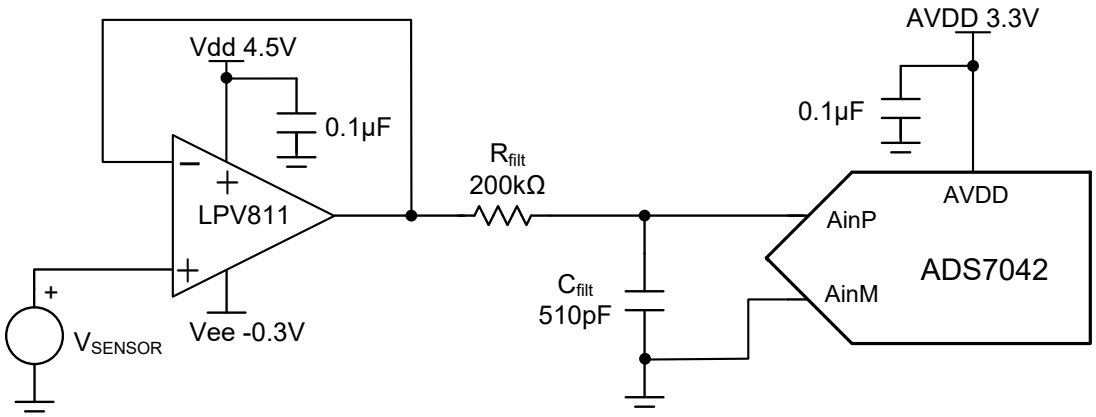
Reed Kaczmarek

Input	ADC Input	Digital Output ADS7042
V_{inMin} = 0V	AIN_P = 0V, AIN_M = 0V	000_H or 0_{10}
V_{inMax} = 3.3V	AIN_P = 3.3V, AIN_M = 0V	FFF_H or 4096_{10}

Power Supplies		
AVDD	**V_{ee}**	**V_{dd}**
3.3V	–0.3V	4.5V

Design Description

This design shows an low-power amplifier being used to drive a SAR ADC that consumes only nW of power during operation. This design is intended for systems collecting sensor data and require a low-power signal chain which only burns single-digit µW of power. *PIR sensors*, *gas sensors*, and *glucose monitors* are a few examples of power-sensitive systems that benefit from this SAR ADC design. The values in the component selection section can be adjusted to allow for different data throughput rates and different bandwidth amplifiers. *Low-Power Sensor Measurements: 3.3 V, 1 ksps, 12-bit Single-Ended, Single Supply* shows a simplified version of this circuit where the negative supply is grounded. The –0.3-V negative supply in this example is used to achieve the best possible linear input signal range. See *SAR ADC Power Scaling* for a detailed description of trade-offs in low-power SAR design.



Specifications

Specification	Calculated	Simulated	Measured
Transient ADC Input Settling (1ksps)	< 0.5 × LSB = 402µV	41.6µV	N/A
AVDD Supply Current (1ksps)	230nA	N/A	214.8nA
AVDD Supply Power (1ksps)	759nW	N/A	709nW
VDD OPAMP Supply Current	450nA	N/A	431.6nA
VDD OPAMP Supply Power	2.025µW	N/A	1.942µW
AVDD + VDD System Power (1ksps)	2.784µW	N/A	2.651µW

Design Notes

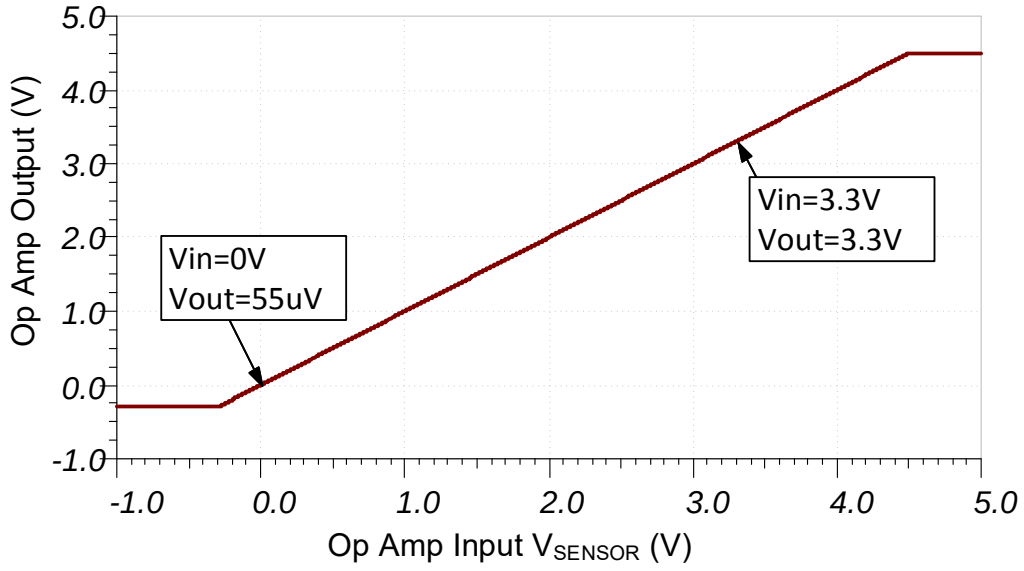
1. Determine the linear range of the op amp based on common mode, output swing, and linear open loop gain specification. This is covered in the component selection section.
2. Select a COG (NPO) capacitor for Cfilt to minimize distortion.
3. The *TI Precision Labs – ADCs* training video series covers methods for selecting the charge bucket circuit Rfilt and Cfilt (see *Introduction to SAR ADC Front-End Component Selection*). These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here will give good settling and AC performance for the amplifier and data converter in this example. If you modify the design you will need to select a different RC filter.

Component Selection

1. Select a low-power op amp:
   - Supply current < 0.5µA
   - Gain bandwidth product > 5kHz (5 times the sampling rate)
   - Unity gain stable
   - LPV811 – 450-nA supply current, 8-kHz gain bandwidth product, unity gain stable
2. Find op amp maximum and minimum output for linear operation:
   $V_{ee} + 0V < V_{out} < V_{dd} - 0.9V$ from LPV811 V_{cm} specification
   $V_{ee} + 10mV < V_{out} < V_{dd} - 10mV$ from LPV811 Vout swing specification
   $V_{ee} + 0.3V < V_{out} < V_{dd} - 0.3V$ from LPV811 Aol linear region specification
3. Typical power calculations (at 1ksps) with expected values. See *SAR ADC Power Scaling* for a detailed description of trade-offs in low-power SAR design:
   $P_{AVDD} = I_{AVDD\_AVG} \times AVDD = 230nA \times 3.3V = 759nW$
   $P_{LPV811} = I_{LPV811} \times (V_{dd} - V_{ee}) = 450nA \times (4.5V - (-0.3V)) = 2.16\mu W$
   $P_{total} = P_{AVDD} + P_{LPV811} = 759nW + 2.16\mu W = 2.919\mu W$
4. Typical power calculations (at 1ksps) with measured values:
   $P_{AVDD} = I_{AVDD\_AVG} \times AVDD = 214.8nA \times 3.3V = 708.8nW$
   $P_{LPV811} = I_{LPV811} \times (V_{dd} - V_{ee}) = 431.6nA \times (4.5V - (-0.3V)) = 2.071\mu W$
   $P_{total} = P_{AVDD} + P_{LPV811} = 708.8nW + 2.071\mu W = 2.780\mu W$
5. Find Rfilt and Cfilt to allow for settling at 1ksps. Refer to *Refine the Rfilt and Cfilt Values* (a *Precision Labs* video) for the algorithm to select Rfilt and Cfilt. The final value of 200kΩ and 510pF proved to settle to well below ½ of a least significant bit (LSB).

DC Transfer Characteristics

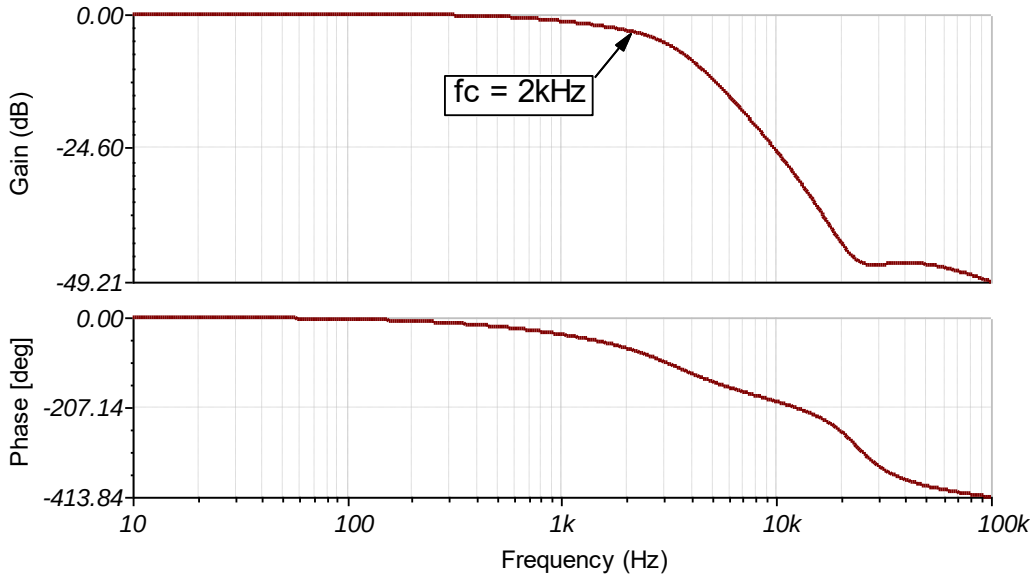
The following graph shows a linear output response for inputs from 0 to 3.3V. The full-scale range (FSR) of the ADC falls within the linear range of the op amp. Refer to *Determining a SAR ADC's Linear Range when using Operational Amplifiers* for detailed theory on this subject.



AC Transfer Characteristics

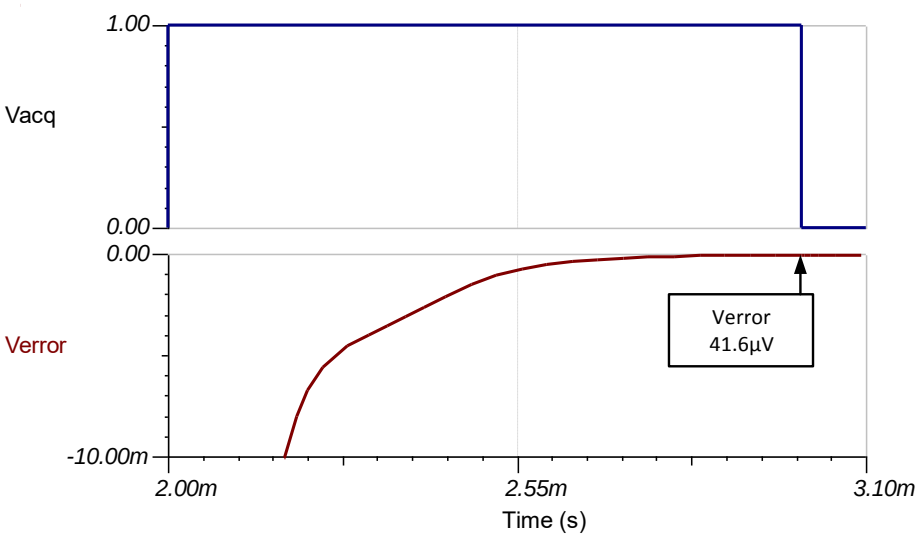
The bandwidth simulation includes the effects of the amplifier output impedance and the RC charge bucket circuit (R_{filt} and C_{filt}).The bandwidth of the RC circuit is shown in the following equation to be 1.56kHz. The simulated bandwidth of 2kHz includes effects from the output impedance interacting with the impedance of the load. See *TI Precision Labs - Op Amps: Bandwidth 1* for more details on this subject.

$$f_C = \frac{1}{2\times\pi\times R_{filt}\times C_{filt}} = \frac{1}{2\times\pi\times(200k\Omega)\times(510pF)} = 1.56kHz$$



Transient ADC Input Settling Simulation

The following simulation shows settling to a 3-V DC input signal. This type of simulation shows that the sample and hold kickback circuit is properly selected to within ½ of an LSB (402µV). Refer to *Introduction to SAR ADC Front-End Component Selection* for detailed theory on this subject.



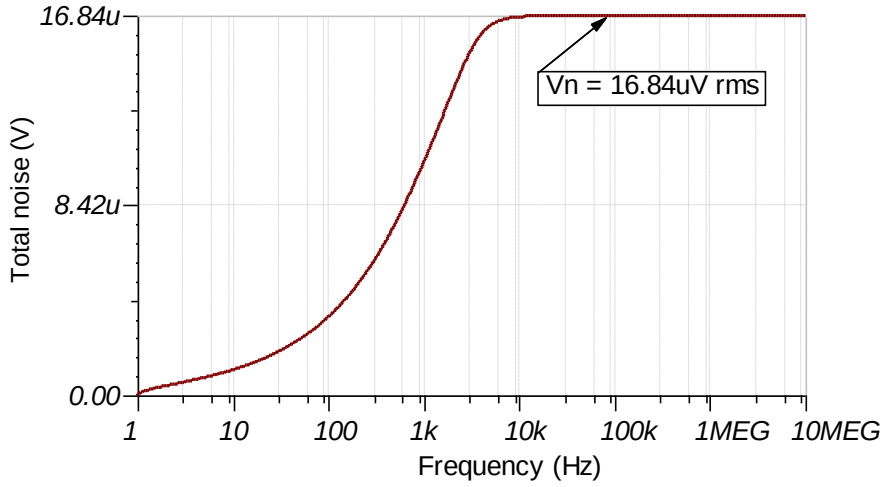
Noise Simulation

This section walks through a simplified noise calculation for a rough estimate. We neglect resistor noise in this calculation as it is attenuated for frequencies greater than 10kHz.

$$f_c = \frac{1}{2\times\pi\times R_{filt}\times C_{filt}} = \frac{1}{2\times\pi\times 200k\Omega\times 510pF} = 1560Hz$$

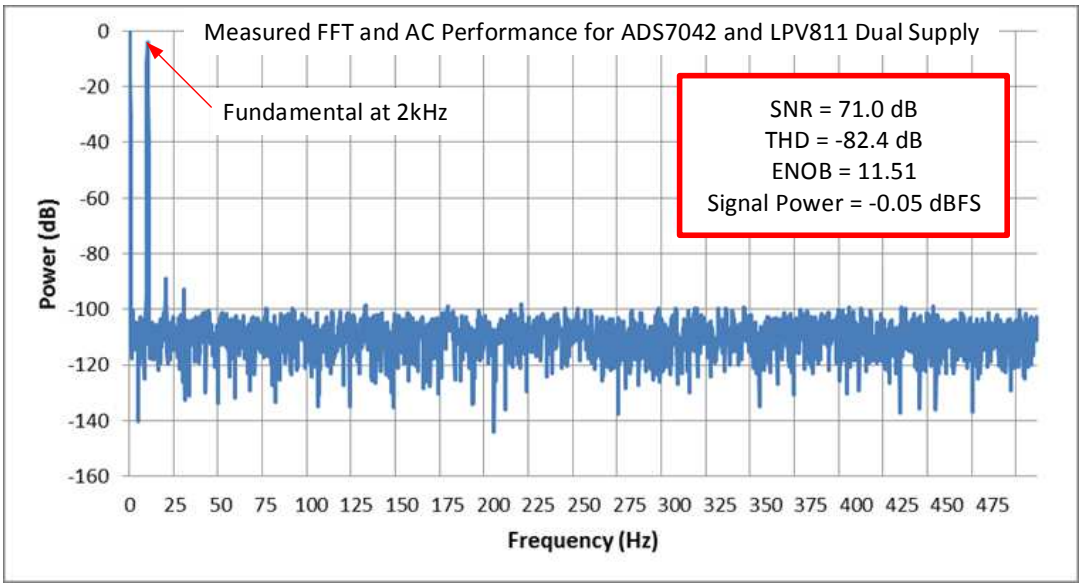
$$E_n = e_{n811}\times\sqrt{K_n\times f_c} = \frac{340nV}{\sqrt{Hz}}\times\sqrt{1.57\times 1560Hz} = 16.8\mu V$$

Note that the calculated and simulated values match well. Refer to *Calculating the Total Noise for ADC Systems* for detailed theory on this subject.



Measure FFT

This performance was measured on a modified version of the ADS7042EVM with a 10-Hz input sine wave. The AC performance indicates SNR = 71.0dB, THD = –82.4dB, and ENOB (effective number of bits) = 11.51, which matches well with the specified performance of the ADC, SNR = 70dB and THD = –80dB. This test was performed at room temperature. See *Introduction to Frequency Domain* for more details on this subject.



Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS7042 (1)	12-bit resolution, SPI, 1-Msps sample rate, single-ended input, AVDD reference input range 1.6 V to 3.6 V.	http://www.ti.com/product/ADS7042	Links to similar devices
LPV811 (2)	8-kHz bandwidth, rail-to-rail output, 450-nA supply current, unity gain stable	http://www.ti.com/product/LPV811	Links to similar devices

(1) The ADS7042 uses the AVDD as the reference input. A high-PSRR LDO, such as the TPS7A47, should be used as the power supply.

(2) The LPV811 is also commonly used in low-speed applications for sensors. Furthermore, the rail-to-rail output allows for linear swing across the entire ADC input range.

Link to Key Files (TINA)

Design files for this circuit - http://www.ti.com/lit/zip/sbam342

For direct support from TI Engineers use the E2E community:

http://e2e.ti.com/

TI Precision Labs Training Series community:

TI Precision Labs - https://training.ti.com/ti-precision-labs-overview

Other Links

www.ti.com/adcs

www.ti.com/opamp

Low-Power Sensor Measurements: 3.3V, 1ksps, 12-bit Single-Ended, Single Supply

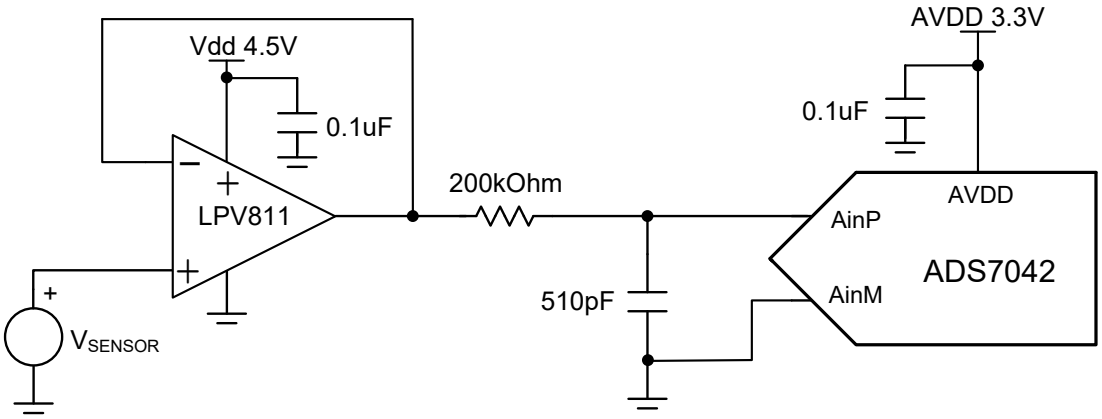
Reed Kaczmarek

Input	ADC Input	Digital Output ADS7042
VinMin = 0 V	AIN_P = 0V, AIN_M = 0V	000_H or 0_{10}
VinMax = 3.3V	AIN_P = 3.3V, AIN_M = 0V	FFF_H or 4096_{10}

Power Supplies		
AVDD	**Vee**	**Vdd**
3.3V	0V	4.5V

Design Description

This design shows an ultra-low power amplifier being used to drive a SAR ADC that consumes only nanoWatts of power during operation. This design is intended for collecting sensor data by providing overall system-level power consumption on the order of single-digit microWatts. *PIR sensors*, *gas sensors*, and *glucose monitors* are a few examples of possible implementations of this SAR ADC design. The values in the *component selection* section can be adjusted to allow for different data throughput rates and different bandwidth amplifiers. *Low-Power Sensor Measurements: 3.3V, 1ksps, 12-bit Single-Ended, Dual Supply* shows a more sophisticated version of this circuit where the negative supply is connected to a small negative voltage (–0.3V). The single-supply version has degraded performance when the amplifier output is near zero volts. However, in most cases the single-supply configuration is preferred for its simplicity.



Specifications

Specification	Calculated	Simulated	Measured
Transient ADC Input Settling (1ksps)	< 0.5·LSB = 402µV	41.6µV	N/A
AVDD Supply Current (1ksps)	230nA	N/A	214.8nA
AVDD Supply Power (1ksps)	759nW	N/A	709nW
VDD OPAMP Supply Current	450nA	N/A	431.6nA
VDD OPAMP Supply Power	2.025µW	N/A	1.942µW
AVDD + VDD System Power (1ksps)	2.784µW	N/A	2.651µW

Design Notes

1. Determine the linear range of the op amp based on common mode, output swing, and linear open loop gain specification. This is covered in the *component selection* section.
2. Select COG capacitors to minimize distortion.
3. Use 0.1% 20ppm/°C film resistors or better to minimize distortion.
4. The *TI Precision Labs – ADCs* training video series covers methods for selecting the charge bucket circuit Rfilt and Cfilt. These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here will give good settling and AC performance for the amplifier and data converter in this example. If you modify this design you will need to select a different RC filter. Refer to the *Introduction to SAR ADC Front-End Component Selection* training video for an explanation of how to select the RC filter for best settling and AC performance.

Component Selection

1. Select a low-power operational amp:
   - Supply current < 0.5µA
   - Gain bandwidth product > 5kHz (5 times the sampling rate)
   - Unity gain stable
   - For this cookbook, the LPV811 was selected. It has a 450-nA supply current, 8-kHz gain bandwidth product, and is unity gain stable.
2. Find op amp maximum and minimum output for linear operation

   $V_{ee} + 0V < V_{out} < V_{dd} - 0.9V$ from LPV811 Vcm specification

   $V_{ee} + 10mV < V_{out} < V_{dd} - 10mV$ from LPV811 Vout swing specification

   $V_{ee} + 0.3V < V_{out} < V_{dd} - 0.3V$ from LPV811 Aol linear region specification

   $0.3V < V_{in} < 3.4V$ Combined worst case

   NOTE: The linear range of the LPV811 is 300mV above ground. This means to design a system to guarantee a full linear range from 0V to 3.3V (full-scale range (FSR) of ADS7042), then a negative supply is required. This design shows that full-measured SNR and THD specifications of the ADS7042 are met without using a negative supply voltage. This testing was only at room temperature and for a more robust system; *Low-Power Sensor Measurements: 3.3V, 1ksps, 12-bit Single-Ended, Dual Supply* shows this design using a negative supply instead of ground.
3. Typical power calculations (at 1ksps) with expected values:

   $P_{AVDD} = I_{AVDD\_Avg} \cdot AVDD = 230nA \cdot 3.3V = 759nW$

   $P_{LPV811} = I_{LPV811} \cdot (V_{dd} - V_{ee}) = 450nA \cdot (4.5V - 0V) = 2.025\mu W$

   $P_{total} = P_{AVDD} + P_{LPV811} = 759nW + 2.025\mu W = 2.794\mu W$
4. Typical power calculations (at 1ksps) with measured values:

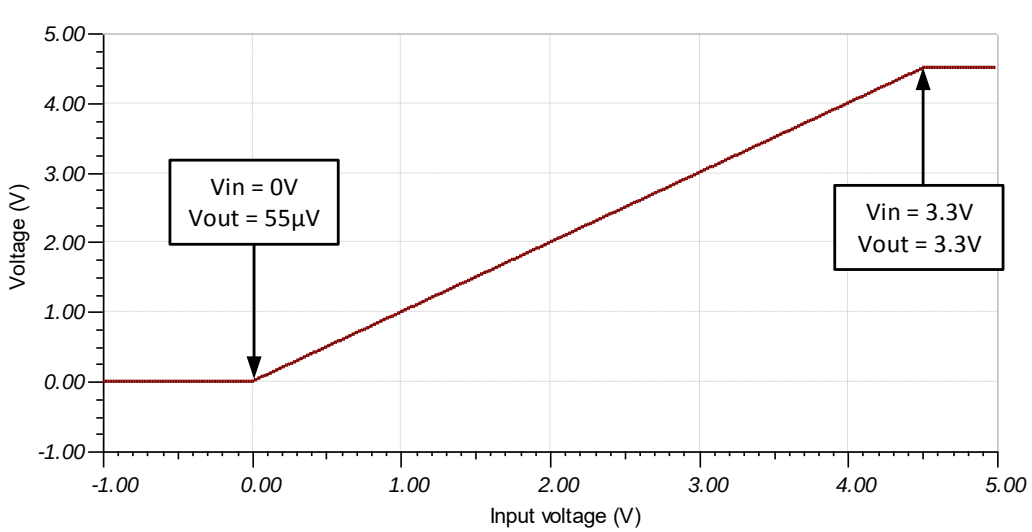
   $P_{AVDD} = I_{AVDD\_Avg} \cdot AVDD = 214nA \cdot 3.3V = 709nW$

   $P_{LPV811} = I_{LPV811} \cdot (V_{dd} - V_{ee}) = 431.6nA \cdot (4.5V - 0V) = 1.942\mu W$

   $P_{total} = P_{AVDD} + P_{LPV811} = 709nW + 1.942\mu W = 2.651\mu W$
5. Find Rfilt and Cfilt to allow for settling at 1ksps. *Refine the Rfilt and Cfilt Values* (a *Precision Labs* video) showing the algorithm for selecting Rfilt and Cfilt. The final value of 200kΩ and 510pF proved to settle to well below ½ of a least significant bit (LSB).

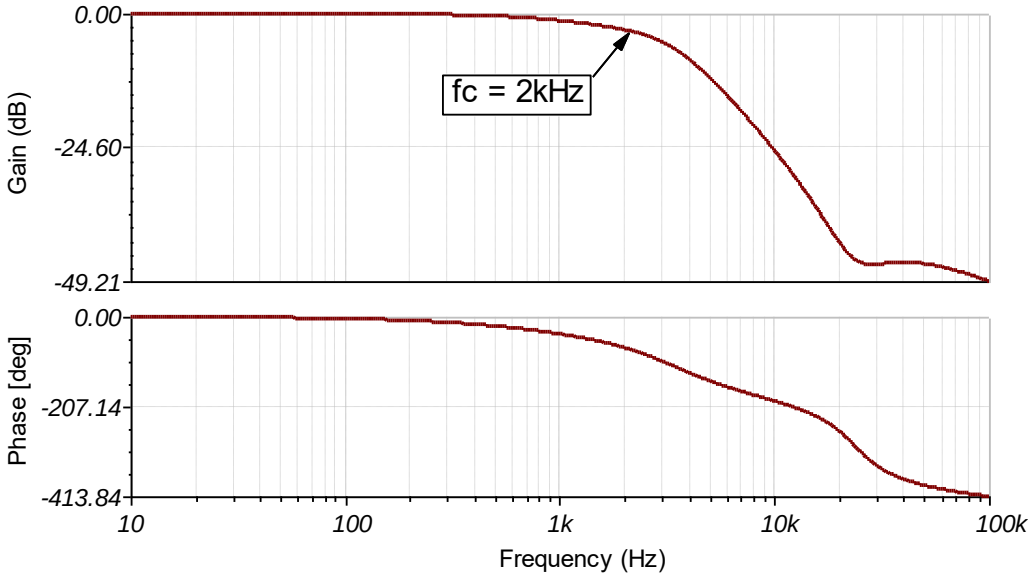
DC Transfer Characteristics

The following graph shows a linear output response for inputs from 0 to 3.3V. The FSR of the ADC falls within the linear range of the op amp.



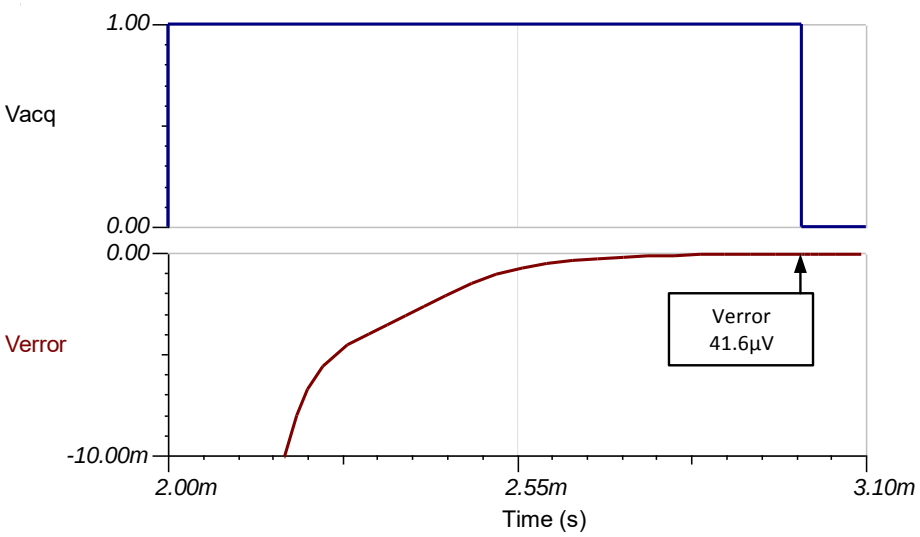
AC Transfer Characteristics

The bandwidth is simulated to be 7.02kHz at the gain of 0dB which is a linear gain of 1. This bandwidth will allow for settling at 1ksps.



Transient ADC Input Settling Simulation

The following simulation shows settling to a 3-V DC input signal. This type of simulation shows that the sample and hold kickback circuit is properly selected to within ½ of a LSB (402µV). Refer to *Introduction to SAR ADC Front-End Component Selection* for detailed theory on this subject.



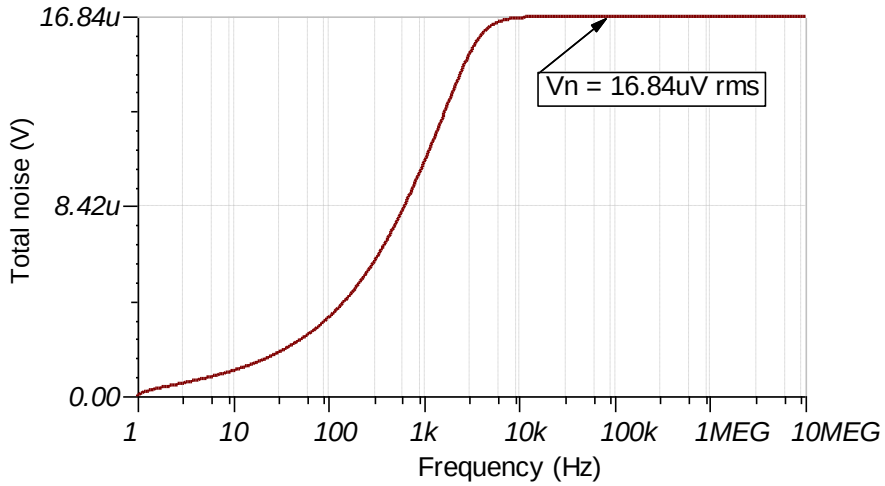
Noise Simulation

This section details a simplified noise calculation for a rough estimate. We neglect resistor noise in this calculation as it is attenuated for frequencies greater than 10kHz.

$$f_c = \frac{1}{2 \cdot \pi \cdot R_{filt} \cdot C_{filt}} = \frac{1}{2 \cdot \pi \cdot (200k\Omega) \cdot (510pF)} = 1560.3Hz$$

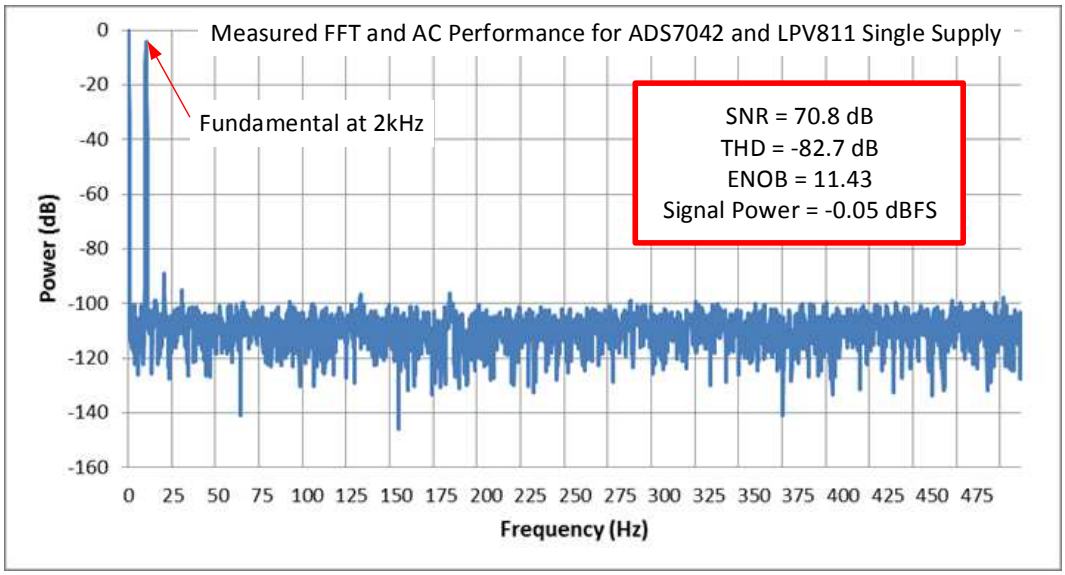
$$E_n = e_{n811} \cdot \sqrt{2 \cdot K_n \cdot f_c} = (340nV / \sqrt{Hz}) \cdot \sqrt{1.57 \cdot (1560Hz)} = 16.8\mu V$$

Note that calculated and simulated match well. Refer to *Calculating the Total Noise for ADC Systems* for detailed theory on this subject.



Measure FFT

This performance was measured on a modified version of the ADS7042EVM-PDK. The AC performance indicates SNR = 70.8dB, THD = –82.7dB, and ENOB (effective number of bits) = 11.43, which matches well with the specified performance of the ADC of SNR = 70dB.



Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS7042[1]	12-bit resolution, SPI, 1-Msps sample rate, single-ended input, AVDD, Vref input range 1.6 V to 3.6 V.	http://www.ti.com/product/ADS7042	Links to similar devices
LPV811[2]	8 kHz bandwidth, Rail-to-Rail output, 450 nA supply current, unity gain stable	http://www.ti.com/product/LPV811	http://www.ti.com/opamps

(1) The ADS7042 uses the AVDD as the reference input. A high-PSRR LDO, such as the TPS7A47, should be used as the power supply.

(2) The LPV811 is also commonly used in low speed applications for sensors. Furthermore, the rail-to-rail output allows for linear swing across all of the ADC input range.

Link to Key Files

Tina Files for Low Power Sensor Measurements - **http://www.ti.com/lit/zip/sbam341**

For direct support from TI Engineers use the E2E community:

e2e.ti.com

Other Links

www.ti.com/adcs

High-Voltage Battery Monitor Circuit: ±20 V, 0-10 kHz, 18-Bit Fully Differential

Bryan McKay, Arthur Kay

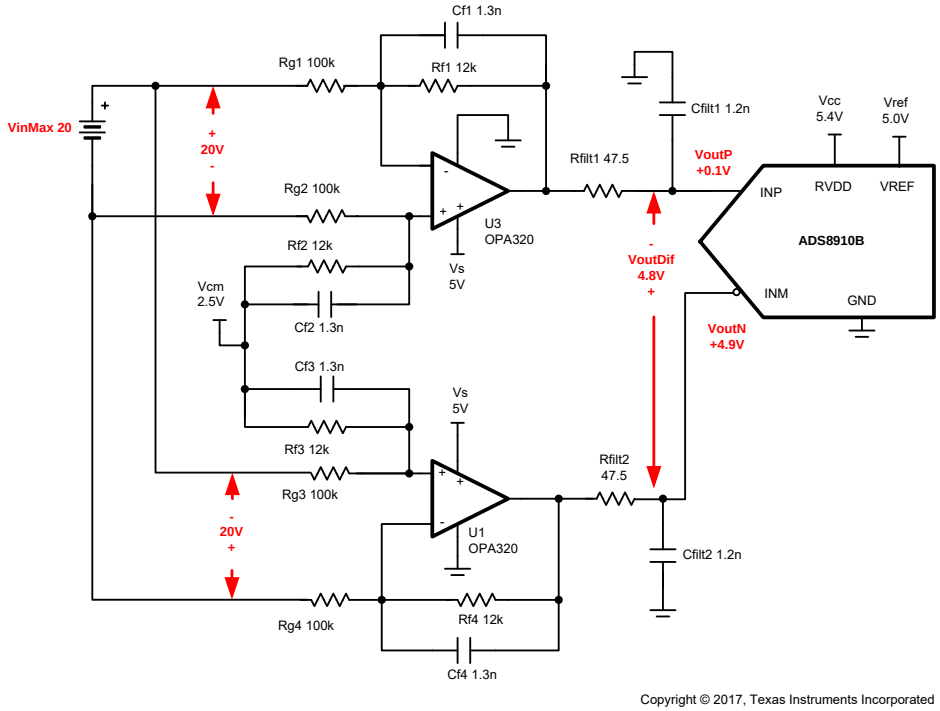
Input	ADC Input	Digital Output ADS8910
VinMin = –20V	VoutDif = 4.8V, VoutP = 4.9V, VoutN = 0.1V	$1EB85_{H}$ or 125829_{10}
VinMax = 20V	VoutDif = –4.8V, VoutP = 0.1V, VoutN = 4.9V	$2147B_{H}$ or $–125829_{10}$

Power Supplies			
Vcc	**Vee**	**Vref**	**Vcm**
5.3 V	0 V	5 V	2.5 V

Design Description

This design translates an input bipolar signal of ±20V into a fully differential ADC differential input scale of ±4.8V, which is within the output linear operation of amplifiers. The values in the *component selection* section can be adjusted to allow for different input voltage levels.

This circuit implementation is applicable in accurate voltage measurement applications such as Battery Maintenance Systems, Battery Analyzers, *Battery Testing Equipment*, *ATE*, and Remote Radio Units (RRU) in wireless base stations.



Specifications

Specification	Calculated	Simulated	Measured
Transient ADC Input Settling	< 0.5LSB or 19µV	6.6µV	N/A
Noise	20.7µV rms	20.65µV rms	30.8µV rms
Bandwidth	10.2kHz	10.4kHz	10.4kHz

Design Notes

1. Determine the linear range of the op amp based on common mode, output swing, and linear open-loop gain specification. This is covered in the *component selection* section.
2. For capacitors in the signal path, select COG type to minimize distortion. In this circuit Cf1, Cf2, Cf3, Cf4, Cfilt1, and Cfilt2 need to be COG type.
3. Use 0.1% 20ppm/°C film resistors or better for good gain drift and to minimize distortion.
4. Precision labs video series covers methods for error analysis. Review the *Statistics Behind Error Analysis* for methods to minimize gain, offset, drift, and noise errors.
5. The *TI Precision Labs – ADCs* training video series covers methods for selecting the charge bucket circuit R_{filt} and C_{filt}. These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here will give good settling and AC performance for the amplifier, gain settings, and data converter in this example. If the design is modified, select a different RC filter. Refer to *Introduction to SAR ADC Front-End Component Selection* for an explanation of how to select the RC filter for best settling and AC performance.

Component Selection

1. The general equation for this circuit.

$$V_{outMinOpa} = \frac{V_{outDifMin}}{2} + V_{cm}$$

$$V_{outMaxOpa} = \frac{V_{outDifMax}}{2} + V_{cm}$$

$$V_{outDif} = V_{inDif} \times Gain_{dif}$$

$$Gain_{dif} = 2 \times \frac{R_f}{R_g}$$

2. Find op amp maximum and minimum output for linear operation.

$-0.1\ V < V_{cm} < 5.1 V$ from OPA320 Vcm specification

$0.035\ V < V_{out} < 4.965\ V$ from OPA320 Vout swing specification

$0.1\ V < V_{out} < 4.9\ V$ from OPA320 Aol specification for linear operation

$0.1\ V < V_{out} < 4.9\ V$ Combined worst case

3. Rearrange the equation from part 1 and solve for VoutDifMin and VoutDifMax. Find maximum and minimum differential output voltage based on combined worst case from step 2.

$$V_{outDifMax} = 2 \cdot V_{outMaxOpa} - 2 \cdot V_{cm} = 2 \cdot (4.9\ V) - 2 \cdot (2.5\ V) = 4.8\ V$$

$$V_{outDifMax} = 2 \cdot V_{outMinOpa} - 2 \cdot V_{cm} = 2 \cdot (0.1\ V) - 2 \cdot (2.5\ V) = -4.8\ V$$

4. Find differential gain based on results from step 3.

$$Gain = \frac{V_{outDifMax} - V_{outDifMin}}{V_{inDifMax} - V_{inDifMin}} = \frac{(4.8\ V) - (-4.8\ V)}{(20\ V) - (-20\ V)} = 0.24$$

5. Find standard resistor values for differential gain. Use *Analog Engineer's Calculator* ("Amplifier and Comparator\Find Amplifier Gain" section) to find standard values for Rf/Rg ratio.

$$\frac{Gain_{dif}}{2} = \frac{R_f}{R_g} = \frac{0.24}{2} = 0.12$$

$$\frac{R_f}{R_g} = 0.12 = \frac{12\ k\Omega}{100\ k\Omega} = 0.12$$

6. Find Cf for cutoff frequency.

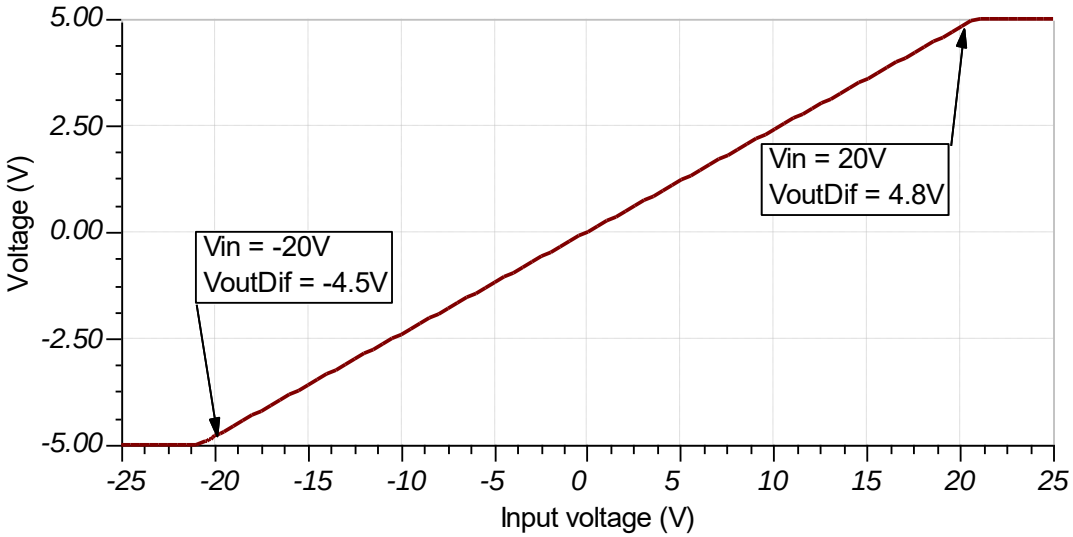
$$f = \frac{1}{2 \cdot \pi \cdot C_f \cdot R_f} = \frac{1}{2 \cdot \pi \cdot (1.3 nF) \cdot (12 k\Omega)} = 10.2\ kHz$$

$$C_f = \frac{1}{2 \cdot \pi \cdot f_c \cdot R_f} = \frac{1}{2 \cdot \pi \cdot (10\ kHz) \cdot (12\ k\Omega)} = 1.326 \quad nF \text{ or } 1.3\ nF \text{ for standard value}$$

$$f = \frac{1}{2 \cdot \pi \cdot C_f \cdot R_f} = \frac{1}{2 \cdot \pi \cdot (1.3 nF) \cdot (12 k\Omega)} = 10.2 kHz$$

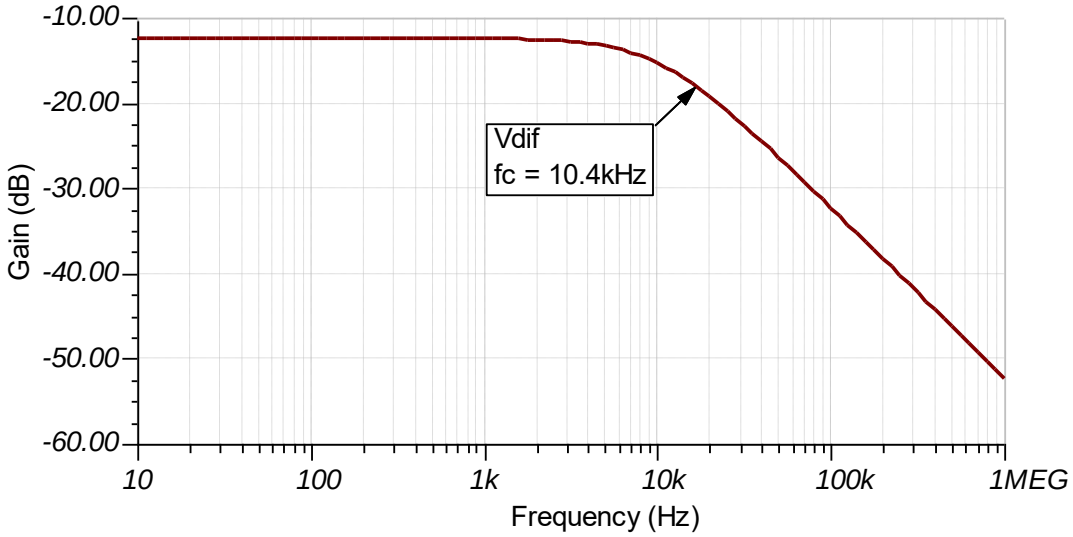
DC Transfer Characteristics

The following graph shows a linear output response for inputs from –20V to +20V. Refer to *Determining a SAR ADC's Linear Range when using Operational Amplifiers* for detailed theory on this subject.



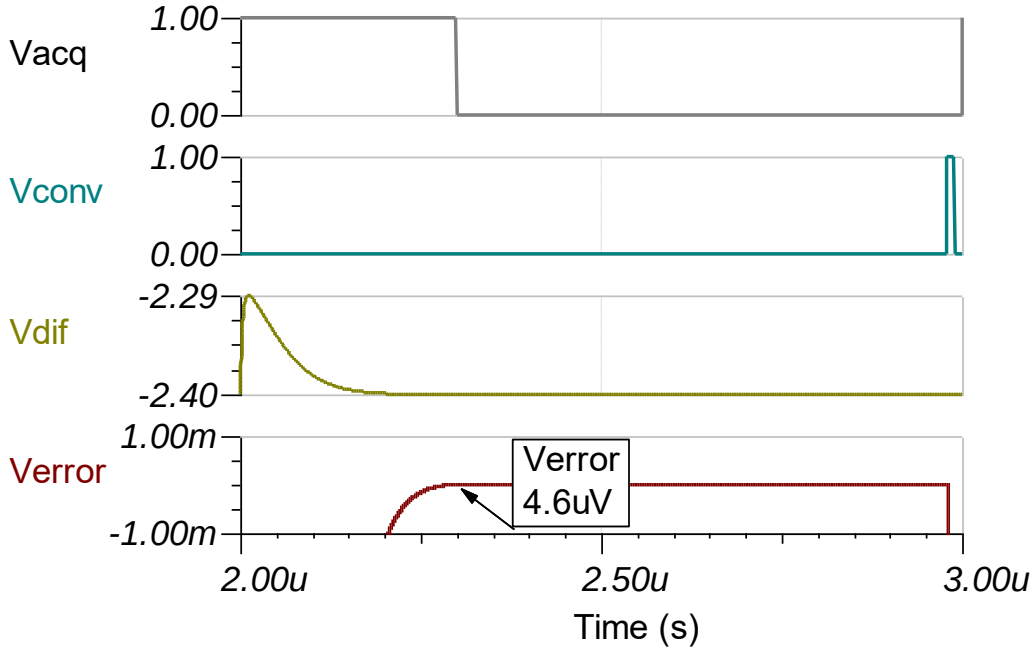
AC Transfer Characteristics

The bandwidth is simulated to be 10.4 kHz, and the gain is –12.4dB which is a linear gain of 0.12. See *Op Amps: Bandwidth 1* for more details on this subject.



Transient ADC Input Settling Simulation

The following simulation shows settling to a –20V dc input signal. This type of simulation shows that the sample and hold kickback circuit is properly selected. Refer to *Introduction to SAR ADC Front-End Component Selection* for detailed theory on this subject.



Noise Simulation

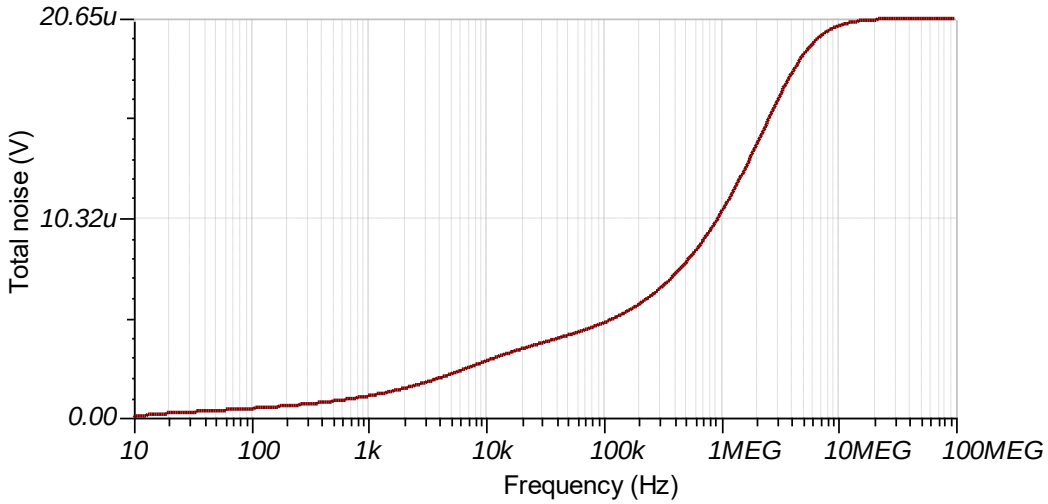
The following simplified noise calculation is provided for a rough estimate. We neglect resistor noise in this calculation as it is attenuated for frequencies greater than 10kHz.

$$f_c = \frac{1}{2\cdot\pi\cdot R_{filt}\cdot C_{filt}} = \frac{1}{2\cdot\pi\cdot(47.5\Omega)\cdot(1.2nF)} = 2.8MHz$$

$$E_{n\_se} = e_{n320}\cdot\sqrt{K_n\cdot f_c} = (7nV/\sqrt{Hz})\cdot\sqrt{(1.57)\cdot(2.8MHz)} = 14.7\mu Vrms \quad \text{for a single ended input}$$

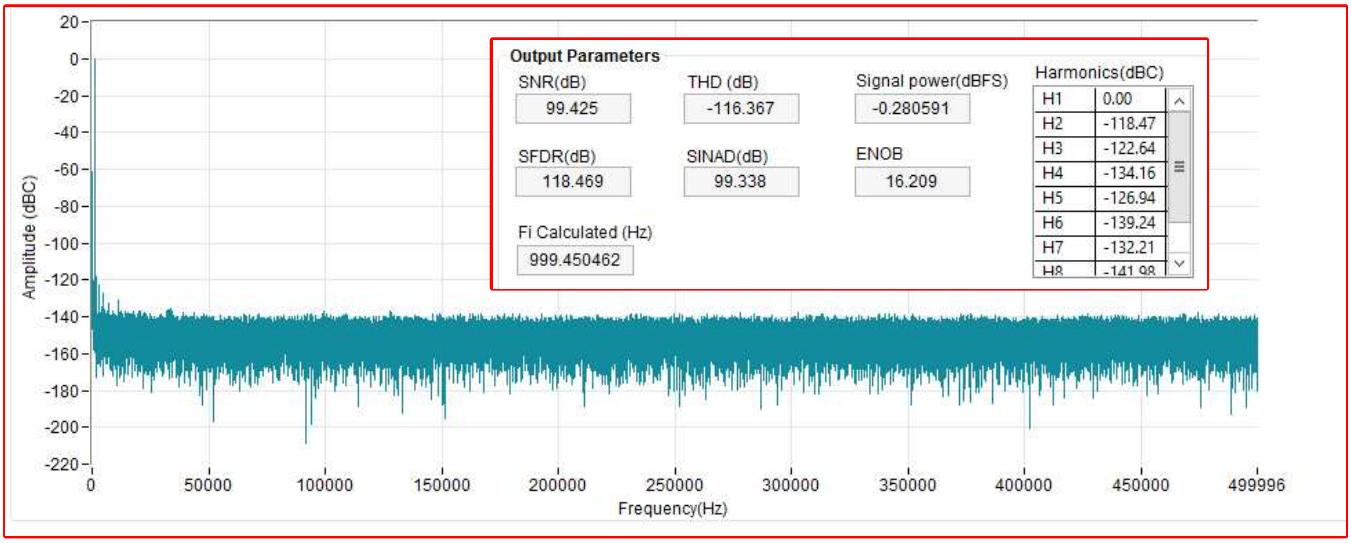
$$E_{n\_tot} = \sqrt{E_{n\_se}{}^2 + E_{n\_se}{}^2} = \sqrt{(14.7\mu V)^2 + (14.7\mu V)^2} = 20.7\mu V \quad \text{rms} \quad \text{Total noise for differential amplifier}$$

Note that calculated and simulated match well. Refer to *Calculating the Total Noise for ADC Systems* for detailed theory on this subject.



Measure FFT

This performance was measured on a modified version of the ADS8910BEVM. The AC performance indicates SNR = 99.4dB, and THD = –116.4dB. See *Introduction to Frequency Domain* for more details on this subject.



Noise Measurement

The following measured result is for both inputs connected to ground. The histogram shows the system offset and noise. The standard deviation in codes is given by the EVM GUI (0.81), and this can be used to calculate the RMS noise (30.9µV rms) as shown in the following equation.

$$LSB = \frac{FSR}{2^N} = \frac{10\ V}{2^{18}} = 38.14 \mu V$$

$$E_{n\_measured} = E_{nSigma} \cdot LSB = (0.81) \cdot (34.14\ \ \mu V) = 30.9 \mu Vrms$$

Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS8910B (1)	18-bit resolution, 1-Msps sample rate, Integrated reference buffer, fully differential input, Vref input range 2.5V to 5V.	http://www.ti.com/product/ADS8900B	Parametric Search
OPA320 (2)	20-MHz bandwidth, Rail-to-Rail with Zero Crossover Distortion, VosMax = 150 µV, VosDriftMax = 5uV/°C, en = 7nV/rtHz	http://www.ti.com/product/OPA320	http://www.ti.com/opamps
REF5050 (3)	3 ppm/°C drift, 0.05% initial accuracy, 4µVpp/V noise	http://www.ti.com/product/REF5050	http://www.ti.com/vref

(1) The REF5050 can be directly connected to the ADS8910B without any buffer because the ADS8910B has a built in internal reference buffer. Also, the REF5050 has the required low noise and drift for precision SAR ADC applications. The OPA320 is also commonly used in 1Msps SAR applications as it has sufficient bandwidth to settle to charge kickback transients from the ADC input sampling. Furthermore, the zero crossover distortion rail-to-rail input allows for linear swing across most of the ADC input range.

(2) The REF5050 can be directly connected to the ADS8910B without any buffer because the ADS8910B has a built in internal reference buffer. Also, the REF5050 has the required low noise and drift for precision SAR ADC applications. The OPA320 is also commonly used in 1Msps SAR applications as it has sufficient bandwidth.

(3) The REF5050 can be directly connected to the ADS8910B without any buffer because the ADS8910B has a built in internal reference buffer. Also, the REF5050 has the required low noise and drift for precision SAR ADC applications. The OPA320 is also commonly used in 1Msps SAR applications as it has sufficient bandwidth.

Link to Key Files for High Voltage Battery Monitor

Design files for this circuit (http://www.ti.com/lit/zip/sbac171)

For direct support from TI Engineers use the E2E commumity:

e2e.ti.com/

Other Links

www.ti.com/adcs

www.ti.com/precisionadc

Single-Ended-to-Differential Circuit Using an Op Amp and Fully Differential Amplifier (FDA) for Bipolar Signals

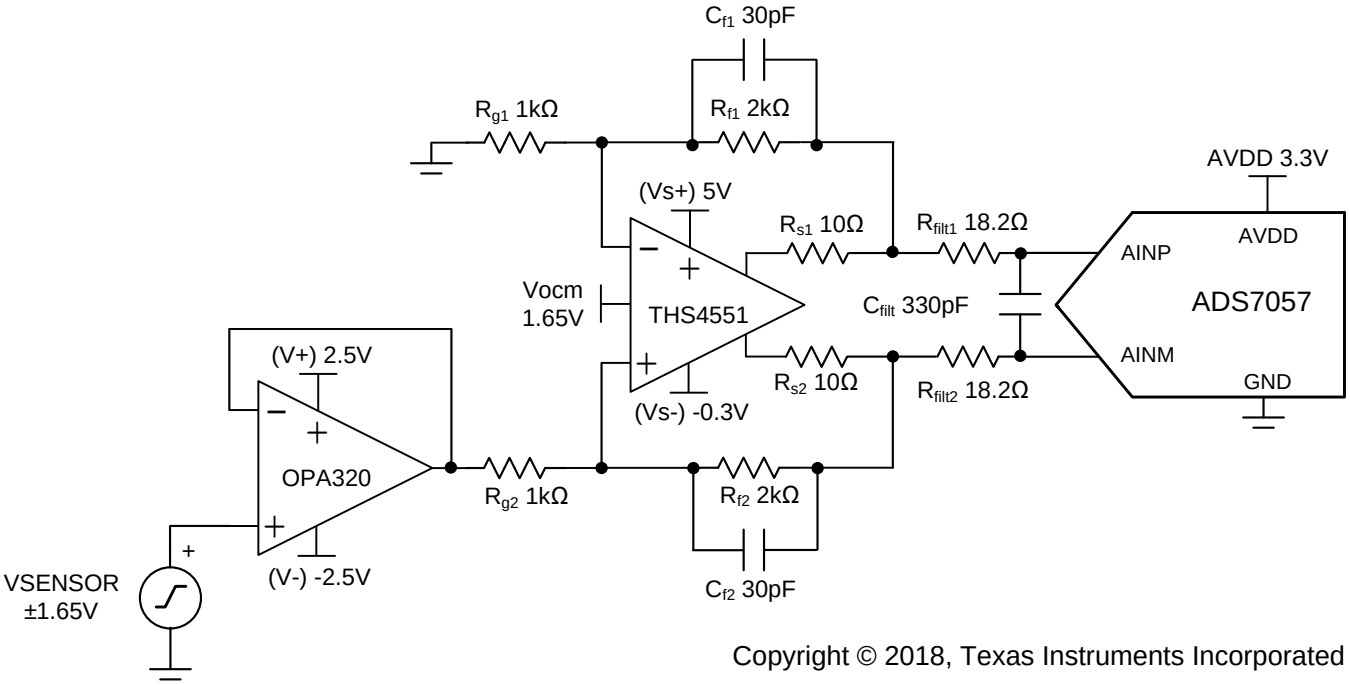
Evan Sawyer

Input	ADC Input	Digital Output ADS7057
V_{in} Min = –3.3V	AINP = 0V AINM = 3.3V	2000_H 8192_{10}
V_{in} Max = 3.3V	AINP = 3.3V AINM = 0V	$1FFF_H$ 8191_{10}

Power Supplies		
AVDD	**GND**	**DVDD**
3.3V	0V	1.8V

Design Description

This design is intended to demonstrate how to convert a bipolar, single-ended signal into a unipolar, fully-differential signal and drive a differential ADC (for more information on these and other signal types, please refer to the *TI Precision Labs* training titled *SAR ADC Input Types*). Compared to a single-ended device, a fully-differential ADC has twice the dynamic range which improves the AC performance of the converter. Many common systems, for example *Sonar Receivers*, *Flow Meters*, and *Motor Controls*, benefit from the higher performance of a differential ADC. The equations and explanation of component selection in this design can be customized based on system specifications and needs. For more information on a similar design using a unipolar input signal, see the cookbook circuit titled *Single-Ended to Differential Signal Conversion for Unipolar Inputs*.



Specifications

Specification	Calculated	Simulated
Transient ADC Input Settling (at 250ksps)	< 0.5 · LSB = 201µV	134.7µV
Conditioned Signal Range (at 250ksps)	> 99% ADC FSR = > 6.53V	6.60V
Noise	43.8µV / √Hz	44.3µV / √Hz

Design Notes

1. The ADS7057 was selected because of its throughput (2.5Msps), size (2.25mm²) and low-latency (successive approximation register, or SAR, architecture).
2. Determine the linear range of the fully-differential amplifier (ADC driver) based on common mode, output swing, and linear open-loop gain specification. This is covered in the component selection section.
3. Determine the linear range of the op amp (signal conditioning) based on common mode, output swing, and linear open-loop gain specification. This is covered in the component selection section.
4. Select COG (NPO) capacitors for C_{filt}, to minimize distortion.
5. For best performance, consider using a 0.1% 20ppm/°C film resistor, or better, to minimize distortion.
6. The *TI Precision Labs - ADCs* training video series covers methods for selecting the charge bucket circuit R_{filtx} and C_{filt}. These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here will give good settling and AC performance for the amplifier and data converter in this example. If the design is modified, a different RC filter must be selected. Refer to *Introduction to SAR ADC Front-end Component Selection* (a *TI Precision Labs* training video) for an explanation of how to select the RC filter for best settling and AC performance.

Component Selection

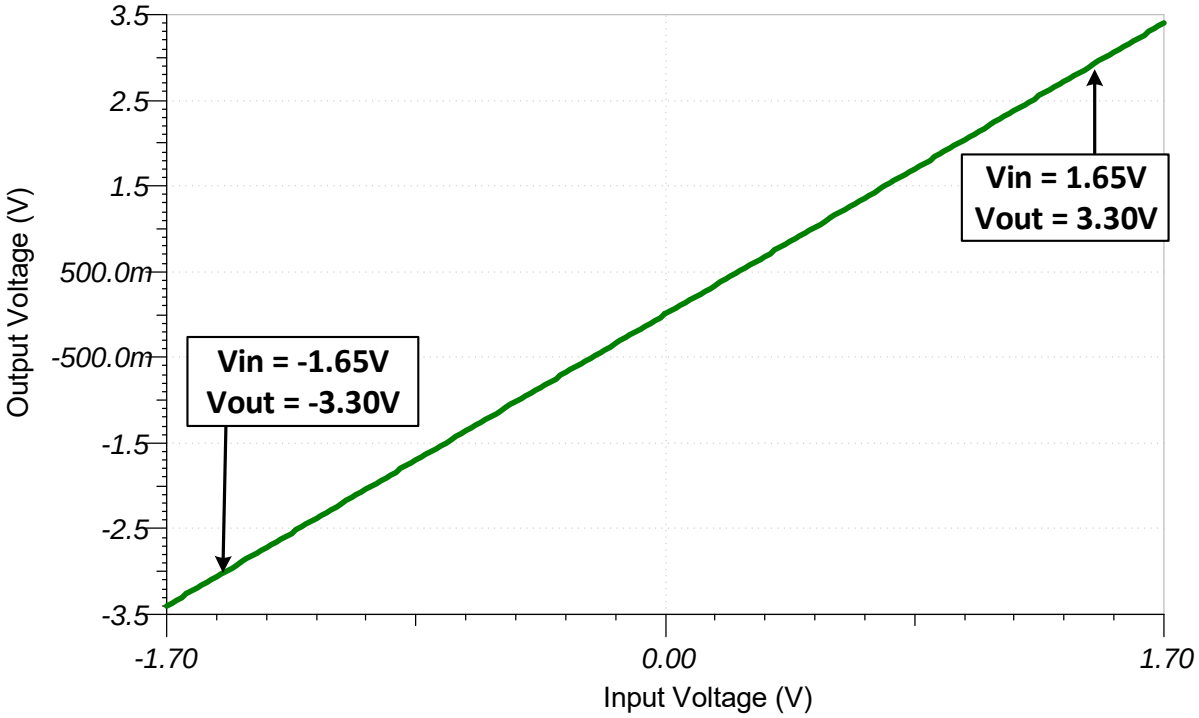
1. Select a fully-differential amplifier capable of driving the ADC:
   THS4551 – Low noise, precision, 150MHz, fully-differential amplifier
   - Wide input common-mode voltage:
     $$V_{s-} - 0.1V < V_{cm} < V_{s+} - 1.3V$$
   - Linear output (requirement: 0V to 3.3V at each output):
     $$V_{s-} + 0.22V < V_{out} < V_{s+} - 0.22V$$
2. Select a wide bandwidth operational amplifier:
   OPA320 – Precision, zero-crossover, 20MHz, RRIO, operational amplifier
   - Gain bandwidth product > 12.5MHz (> 5 times the sampling rate)
   - Input common-mode voltage (requirement: ±1.65V):
     $$V_{-} - 0.1V < V_{cm} < V_{+} + 0.1V$$
   - Linear output:
     $$V_{-} + 0.03V < V_{out} < V_{+} - 0.03V$$
     $$V_{-} + 0.2V < V_{out} < V_{+} - 0.2V$$
   - Combined worst-case linear range (calculated from supplies used with OPA320):
     $$-2.3V < V_{out} < 2.3V$$

NOTE: The operational amplifier is used to protect the sensor from any charge kickbacks that occur when the ADC connects or disconnects the sampling capacitor. This amplifier may not be needed if the sensor has a high output impedance. A negative rail is used for both the OPA320 and THS4551 based on the assumption that the sensor is operating with a negative rail. This also ensures the highest performance from the ADC by providing the full scale input range.

3. Select R_{fx} and R_{gx}
   - The combination of R_{fx} and R_{gx} sets the gain of the system. With an input range of ±1.65V and an ADC full scale of ±3.3V, a gain of 2 was selected for this system.
   - The values of R_{fx} = 2k and R_{gx} = 1k were selected to both provide the desired gain as well as limit the current through the feedback network, thus minimizing power consumption of the system.
4. Select R_{sx}
   - It is important to connect small resistors at the output of the amplifier, in this case 10Ω, to flatten the output impedance and improve stability of the system.
5. Select R_{filtx} and C_{filt} values for settling of 250-kHz input signal and sample rate of 2.5Msps:
   - *Refine the R_{filt} and C_{filt} Values* is a *TI Precision Labs* video showing the methodology for selecting R_{filtx} and C_{filt}. The final value of 18.2Ω and 330pF proved to settle to well below ½ of a least significant bit (LSB) within the acquisition window.

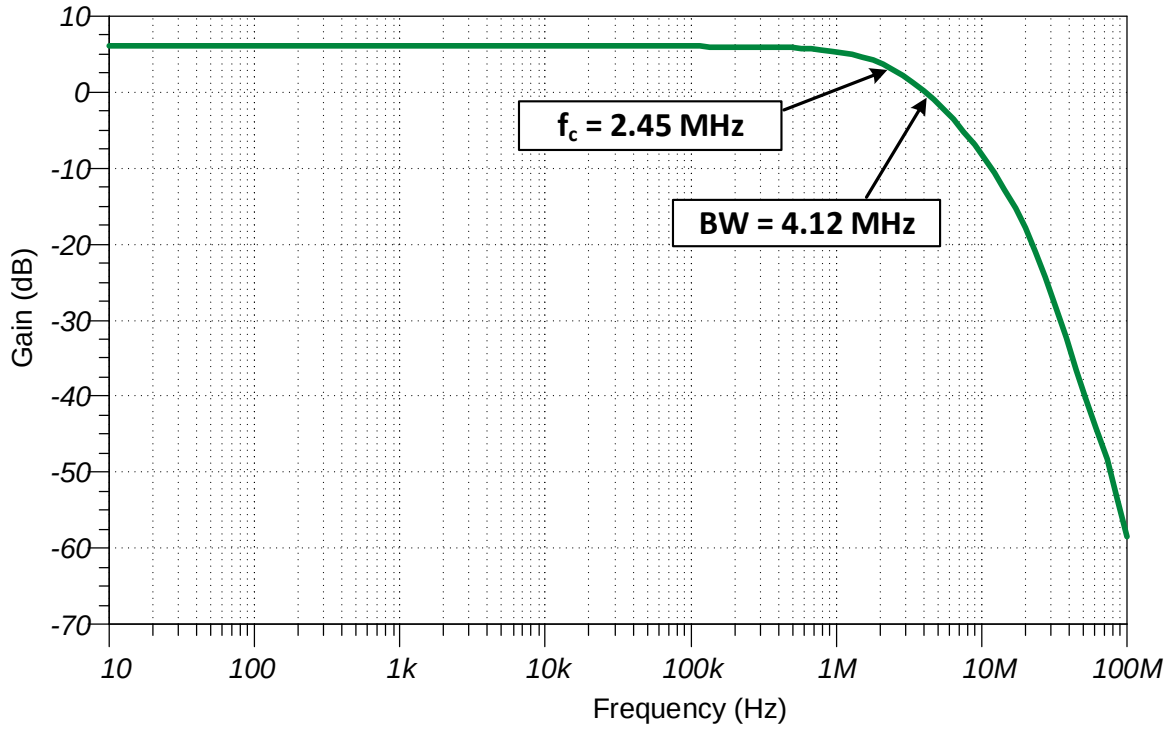
DC Transfer Characteristics

The following graph shows the simulated output for a ±1.65-V input. The analog front end has a linear output of ±3.3V which matches the full-scale range (FSR) of the ADC (with AVDD = 3.3V).



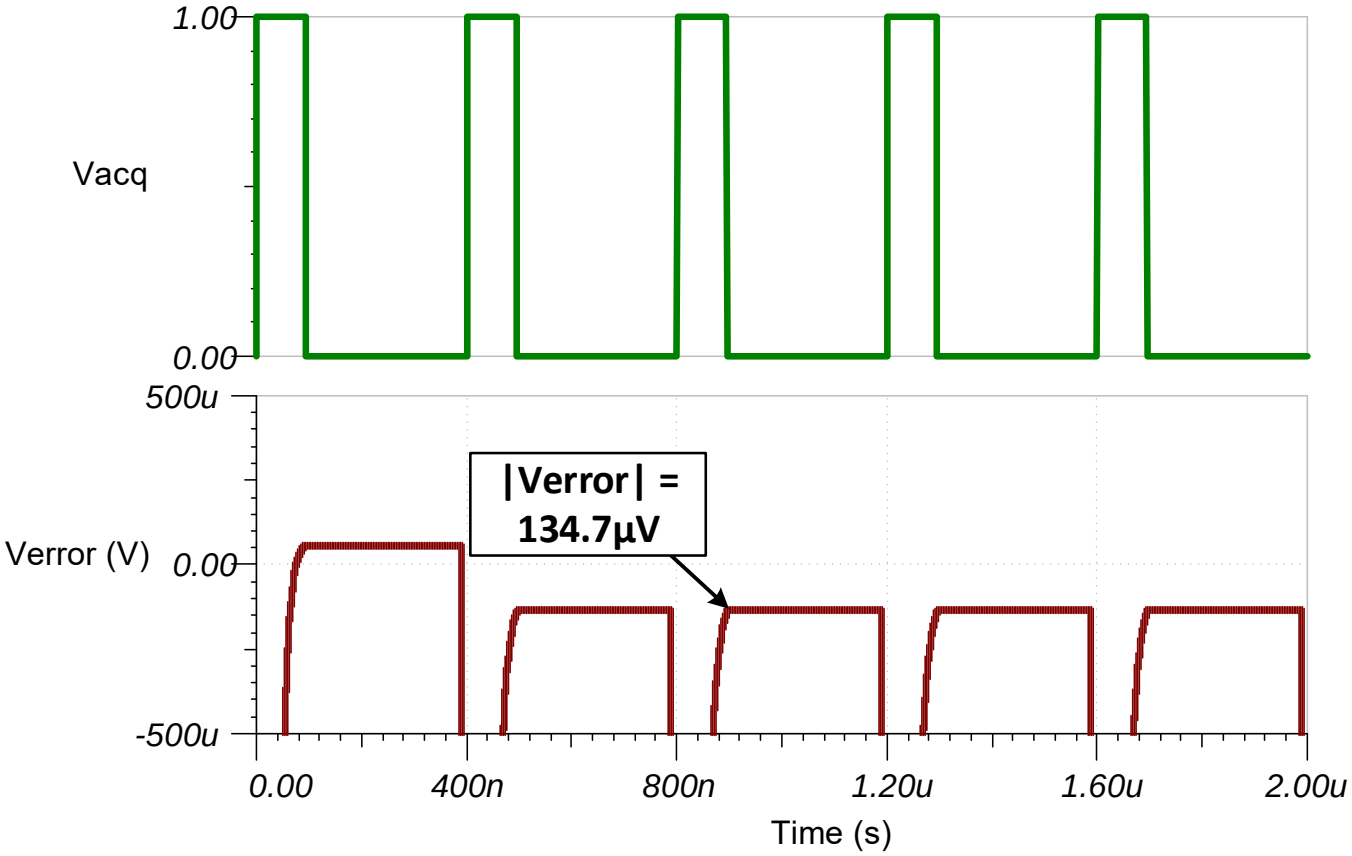
AC Transfer Characteristics

The bandwidth of the analog front end is simulated to be 4.12MHz at the gain of 0dB which is a linear gain of 1. This bandwidth will allow the inputs of the ADC to adequately settle for a 250-ksps input signal.



Transient ADC Input Settling Simulation

The following simulation shows the ADC sample and hold capacitor settling for a 3.3-V DC input signal. This simulation shows that the analog front end is able to drive the ADC with a large step input (from 0V to 3.3V) so it settles to within ½ of an LSB (approximately 200µV) in the allotted acquisition time (95ns). Refer to *Introduction to SAR ADC Front-End Component Selection* for detailed theory on this subject, and follow the link at the end of this design to download these simulation files.



Noise Simulation

This section walks through a simplified noise calculation, providing a rough estimate to compare with the simulated result. The resistor noise is included in this calculation as it is a significant portion of the overall noise of the system. Note that the resistor noise can be reduced by using smaller value resistors, but at the expense of increased power consumption through the feedback network.

$$f_c \quad \frac{1}{2\times\pi\times R_{filt}\times C_{filt}} \quad \frac{1}{2\times\pi\times 2k\Omega\times 30pF} \quad 2.65MHz$$

$$E_n \quad e_{OPA320}\times\sqrt{2\times K_n\times f_c} \quad \left(7nV/\sqrt{Hz}\right)\times\sqrt{2\times 1.57\times 2.65MHz} \quad 20.2\mu V/\sqrt{Hz}$$

$$E_{n\_OPA320} \quad E_n\times Gain \quad 20.2\mu V/\sqrt{Hz}\times 2 \quad 40.4\mu V/\sqrt{Hz}$$

$$E_{n\_THS4551} \quad e_{nTHS4551}\times\sqrt{2\times K_n\times f_c} \quad \left(3.3nV/\sqrt{Hz}\right)\times\sqrt{2\times 1.57\times 2.65MHz} \quad 9.52\mu V/\sqrt{Hz}$$

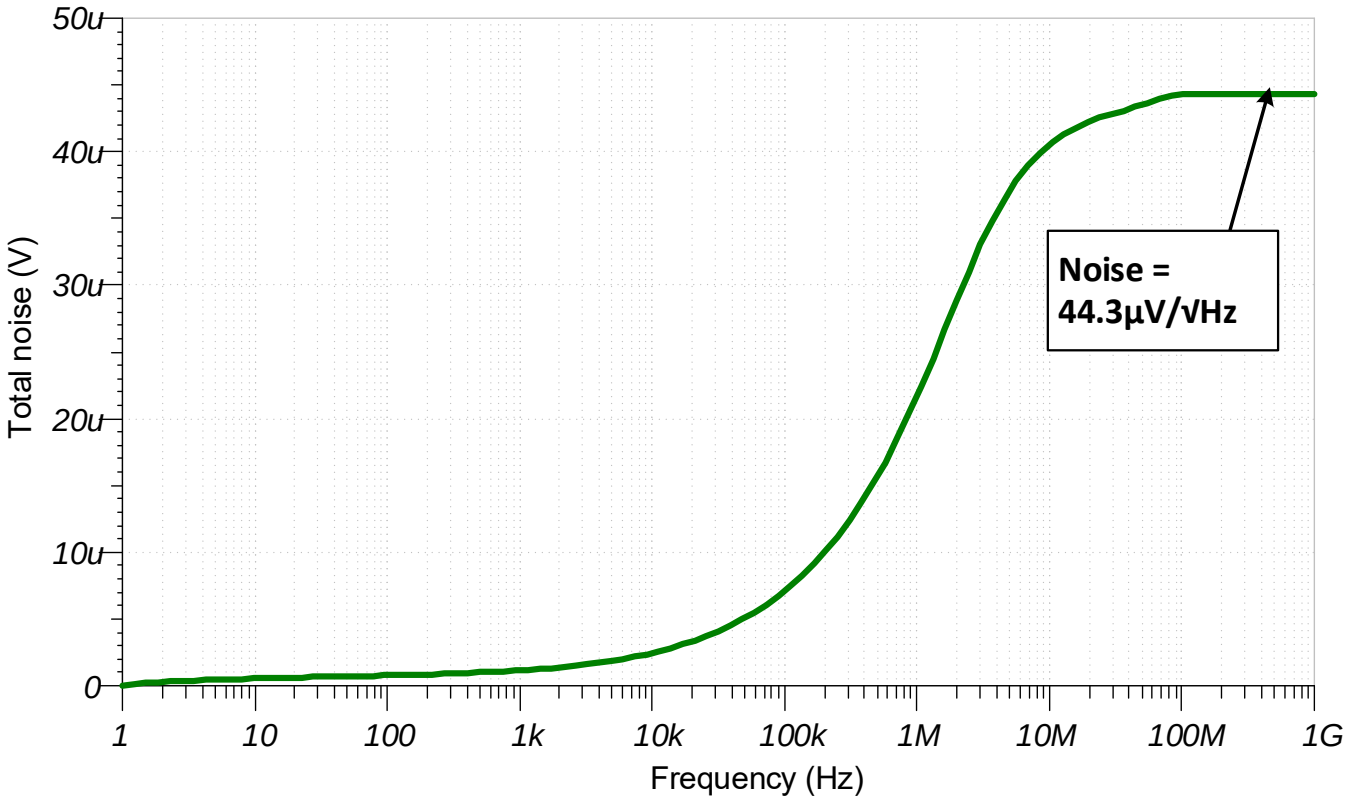
$$E_{Rg} \quad \frac{\sqrt{4\times k\times T\times R_g}}{1\times 10^{-9}}\times\frac{R_f}{R_g}\times\sqrt{2} \quad \frac{\sqrt{4\times 1.38\times 10^{-23}\times(273.15+25)\times 1000}}{1\times 10^{-9}}\times\frac{2000}{1000}\times\sqrt{2}=11.47\mu V/\sqrt{Hz}$$

$$E_{Rf}=\frac{\sqrt{4\times k\times T\times R_f}}{1\times 10^{-9}}\times\sqrt{2} \quad \frac{\sqrt{4\times 1.38\times 10^{-23}\times(273.15+25)\times 2000}}{1\times 10^{-9}}\times\sqrt{2} \quad 8.11\mu V/\sqrt{Hz}$$

Total noise at output equation:

$$E_n=\sqrt{E_{nOPA320}{}^2+E_{n\_THS4551}{}^2+E_{Rg}{}^2+E_{Rf}{}^2} \quad \sqrt{40.4^2+9.52^2+11.47^2+8.11^2} \quad 43.8\mu V/\sqrt{Hz}$$

Note that calculated and simulated match well. Refer to the *TI Precision Labs - ADCs* training video series for detailed theory on this subject.



Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS7057	*14 bit, 2.5 Msps, fully-differential input, SPI, 2.25mm^2 package*	http://www.ti.com/product/ADS7057	Similar Devices
THS4551	*150MHz, 3.3nV/√Hz input voltage noise, fully-differential amplifier*	http://www.ti.com/product/THS4551	Similar Devices
OPA320	*Precision, zero-crossover, 20MHz, 0.9pA Ib, RRIO, operational amplifier*	http://www.ti.com/product/OPA320	Similar Devices

NOTE: The ADS7057 uses the AVDD as the reference input. A high-PSRR LDO, such as the TPS7A47, should be used as the power supply.

Link to Key files (TINA):

Design files for this circuit (http://www.ti.com/lit/zip/sbac181)

Link to Related Cookbooks:

Single-Ended to Differential Signal Conversion for Unipolar Input

For direct support from TI Engineers use the E2E community:

e2e.ti.com

TI Precision Labs Training Series community:

TI Precision Labs - https://training.ti.com/ti-precision-labs-overview

Other Links:

www.ti.com/adcs

www.ti.com/opamp

High-Input Impedance, True Differential, Analog Front End (AFE) Attenuator Circuit for SAR ADCs

Luis Chioye

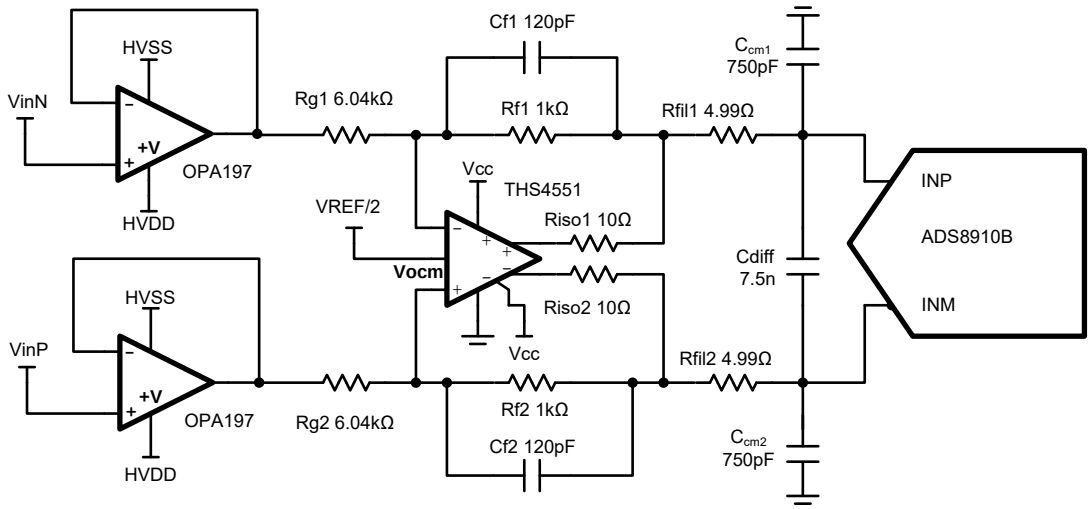
Input Voltage (OPA197 Buffers)	THS4551 Output, ADC Input	ADS8912B Digital Output
VinP = –12V, VinN = +12V, VinMin (Dif) = –24V	VoutDif = –4.00V, VoutP = 0.25V, VoutN = 4.25V	$238E3_H$ -116509_{10}
VinP = +12V, VinN = –12V, VinMax (Dif) = +24V	VoutDif = +4.0V, VoutP = 4.25V, VoutN = 0.25V	$1C71C_H$ +116508_{10}

Supplies and Reference					
HVDD	**HVSS**	**Vcc**	**Vee**	**Vref**	**Vcm**
+15V	–15V	+5.0V	0V	+4.5V	2.5V

Design Description

This analog front end (AFE) and SAR ADC data acquisition solution can measure true differential voltage signals in the range of ±24V (or absolute input range VinP = ±12V, VinN = ±12V) offering high-input impedance supporting data rates up to 500ksps with 18-bit resolution. A precision, 36-V rail-to-rail amplifier with low-input bias current is used to buffer the inputs of a fully-differential amplifier (FDA). The FDA attenuates and shifts the signal to the differential voltage and common-mode voltage range of the SAR ADC. The values in the *component selection* section can be adjusted to allow for different input voltage levels.

This circuit implementation is used in accurate measurement of true differential voltage in *Application-Specific Test Equipment*, *Data Acquisition (DAQ) cards*, and *Analog Input Modules* used in *Programmable Automation Control (PAC)*, *Discrete Control System (DCS)*, and *Programmable Logic Control (PLC)* applications.



Specifications

Specification	Goal	Calculated	Simulated
Transient ADC Input Settling (500ksps)	<< 1 LSB; << 34µV	N/A	0.5µV
Noise (at ADC Input)	$10\mu V_{RMS}$	$9.28\mu V_{RMS}$	$9.76\mu V_{RMS}$
Bandwidth	1.25MHz	1.25MHz	1.1MHz

Design Notes

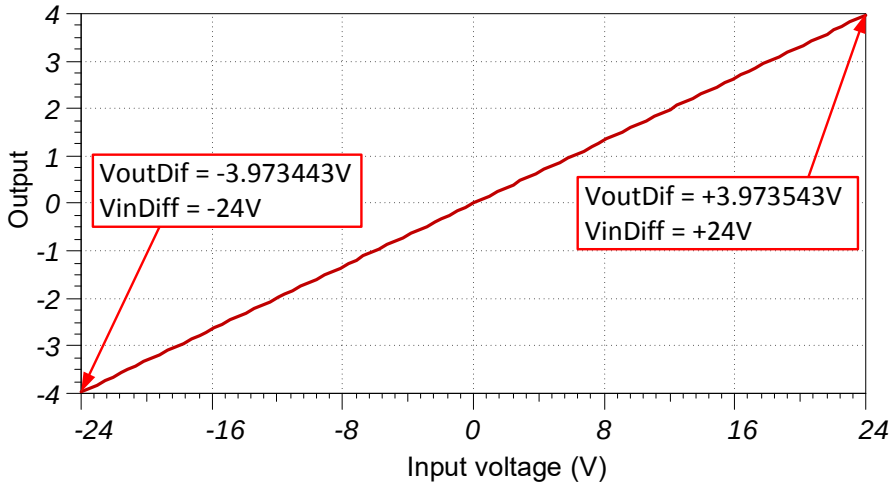
1. Verify the linear range of the op amp (buffer) based on the common mode, output swing specification for linear operation. This is covered in the *component selection* section. Select an amplifier with low input bias current.
2. Find ADC full-scale range and common-mode range specifications. This is covered in the *component selection*.
3. Determine the required attenuation for the FDA based on the input signal amplitude, the ADC full-scale range and the output swing specifications of the FDA. This is covered in the *component selection* section.
4. Select COG capacitors to minimize distortion.
5. Use 0.1% 20ppm/°C film resistors or better for good accuracy, low gain drift, and to minimize distortion.
6. *Understanding and Calibrating the Offset and Gain for ADC Systems* covers methods for error analysis. Review the link for methods to minimize gain, offset, drift, and noise errors
7. *Introduction to SAR ADC Front-End Component Selection* covers methods for selecting the charge bucket circuit Rfilt and Cfilt. These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here will give good settling and AC performance for the amplifier, gain settings, and data converter in this example. If the design is modified, a different RC filter must be selected. Refer to the *Precision Labs* videos for an explanation of how to select the RC filter for best settling and AC performance.

Component Selection and Settings for Buffer Amplifier and FDA

1. Verify the buffer amplifier input range for linear operation:
   Select Supplies $(V-) = -15V$, $(V+) = +15V$ to allow VinP = ±12V VinN = ±12V range
   $(V-) - 0.1V < V_{cm} < (V+) - 3V$ from OPA197 common-mode voltage specification
   $-15.1V < V_{cm} < +12V$ allows required ±12V input voltage range
2. Verify the buffer amplifier output range for linear operation:
   $(V-)+0.6V<V_{out}<(V+)-0.6V$ from OPA197 Aol specification for linear operation
   $-14.4V<V_{out}<14.4V$ allows required±12Voutput voltage range
3. Find ADC full-scale input range. In this circuit, V_{REF} = 4.5V:
   $ADC_{Full\text{-}Scale\ Range} = \pm V_{REF} = \pm 4.5V$ from ADS8910B datasheet
4. Find the required ADC common-mode voltage:
   $V_{CM} \quad \frac{+V_{REF}}{2} \quad +2.25V$ from ADS8910B datasheet, therefore set FDA VCOM = 2.25V
5. Find FDA absolute output voltage range for linear operation:
   $0.23 < V_{out} < 4.77V$ from THS4551 output low/high specification for linear operation
   However, the positive range is limited by $ADC_{Full-Scale\ Range} \quad \pm 4.5V$, therefore
   $0.23V < V_{out} < 4.5V$ where $V_{outMin} = 0.23V$, $V_{outMax} = 4.5V$
6. Find FDA differential output voltage range for linear operation. The general output voltage equations for this circuit follow:
   $V_{outMin} \quad \frac{V_{outDifMin}}{2} + V_{cm}$ and $V_{outMax} \quad \frac{V_{outDifMax}}{2} + V_{cm}$
   Re-arrange the equations and solve for $V_{outDifMin}$and $V_{outDifMax}$.
   Find maximum differential output voltage range based on worst case:
   $V_{outDifMax} = 2 \cdot V_{outMax} - 2 \cdot V_{cm} = 2 \cdot (4.5V) - 2 \cdot (2.25V) = 4.5V$
   $V_{outDifMin} \quad 2 \cdot V_{outMin} - 2 \cdot V_{cm} \quad 2 \cdot (0.23V) - 2 \cdot (2.5V) \quad -4.04V$
   Based on combined worst case, choose $V_{outDifMin}$ = -4.04V and $V_{outDifMax}$ = +4.04V
7. Find the FDA differential input voltage range:
   $V_{inDifmax} = V_{inPmax} - V_{inNmin} = +12V - (-12V) = +24V$
   $V_{inDifmin} = V_{inPmin} - V_{inNmax} = -12V - (+12V) = -24V$
8. Find FDA required attenuation ratio:
   $Gain_{FDA} \quad \frac{V_{outDifMax} - V_{outDifMin}}{V_{inDifMax} - V_{inDifMin}} \quad \frac{(+4.04V) - (-4.04V)}{(+24V) - (-24V)} \quad 0.166\frac{V}{V} \approx \frac{1}{6}\frac{V}{V}$
9. Find standard resistor values to set the attenuation:
   $Gain_{FDA} \quad \frac{R_f}{R_g} \quad \frac{1}{6} V/V \Rightarrow \frac{R_g}{R_f} \quad \frac{1.00k\Omega}{6.04k\Omega} \quad \frac{1}{6.04} V/V$
10. Find C_f for cutoff frequency f_c, R_{flNA} = 1kΩ:
    $C_f \quad \frac{1}{2 \cdot \pi \cdot f_c \cdot R_{flNA}} \quad \frac{1}{2 \cdot \pi \cdot (1.25MHz) \cdot (1k\Omega)} = 127\,pF\ or\ 120\,pF\ standard\ value$

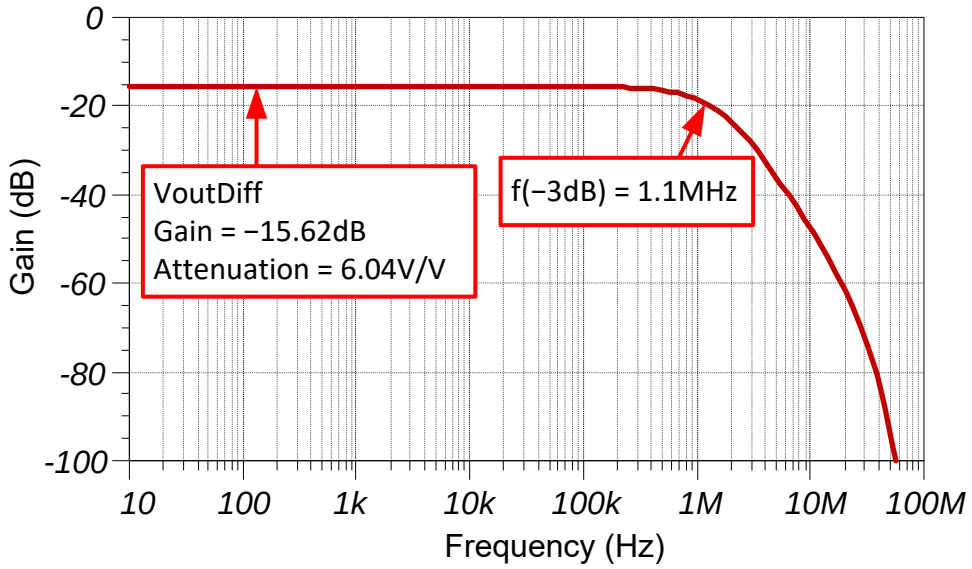
DC Transfer Characteristics

The following graph shows a linear output response for differential inputs from +24V to –24V.



AC Transfer Characteristics

The simulated bandwidth is approximately 1.1MHz and the gain is –15.62dB which is a linear gain of approximately 0.166V/V (attenuation ratio 6.04V/V).



Noise Simulation

Simplified Noise calculation for rough estimate:

$$f_c \quad \frac{1}{2\cdot\pi\cdot R_f\cdot C_f} \quad \frac{1}{2\cdot\pi\cdot(1k\Omega)\cdot(120\,pF)} = 1.33MHz$$

Noise contribution of OPA197 buffer referred to ADC input

$$E_{nOPA197} = e_{nOPA197}\cdot\sqrt{K_n\cdot f_c}\cdot Gain_{FDA}$$

$$E_{nOPA197} = \left(5.5nV/\sqrt{Hz}\right)\cdot\sqrt{1.57\cdot 1.33MHz}\cdot 0.166V/V = 1.319\mu V_{RMS}$$

Noise of THS4551 FDA referred to ADC input

$$\text{Noise gain: } NG = 1 + R_f/R_g = 1 + \frac{1.00k\Omega}{6.04k\Omega} = 1.166V/V$$

$$e_{noFDA} \quad \sqrt{\left(e_{nFDA}\cdot NG\right)^2 + 2\left(i_{nFDA}\cdot R_f\right)^2 + 2\left(4kTR_f\cdot NG\right)}$$

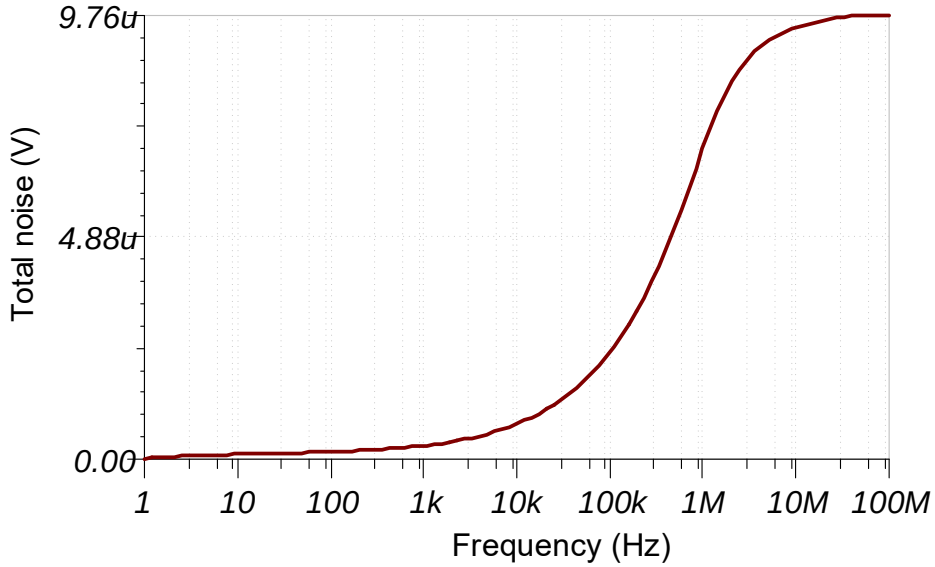
$$e_{noFDA} \quad \sqrt{\left(3.4nV/\sqrt{Hz}\cdot 1.166V/V\right)^2 + 2\left(0.5pA/\sqrt{Hz}\cdot 1k\Omega\right)^2 + 2\left(16.56\cdot 10^{-18}\cdot 1.166V/V\right)}$$

$$e_{noFDA} \quad 7.40nV/\sqrt{Hz}$$

$$E_{nFDA} \quad e_{noFDA}\cdot\sqrt{K_n\cdot f_c} \quad \left(7.40nV/\sqrt{Hz}\right)\cdot\sqrt{1.57\cdot 1.33MHz} \quad 9.28\mu V_{RMS}$$

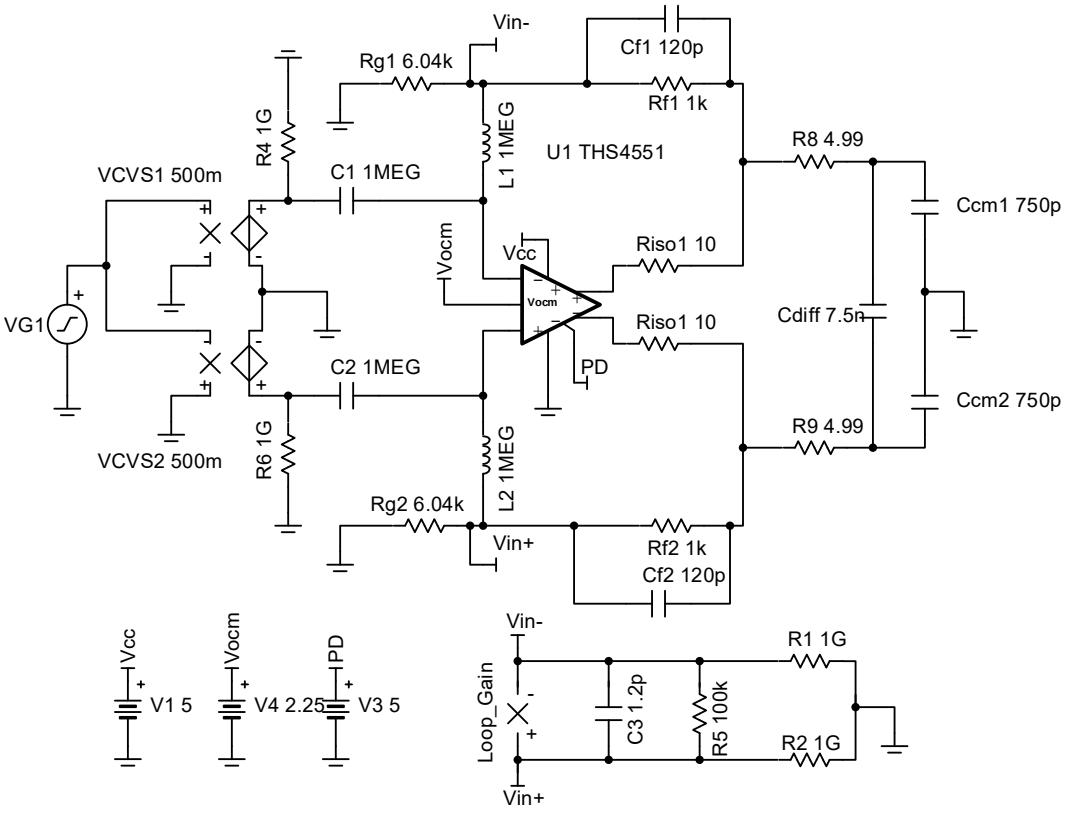
$$\textit{Total Noise} \quad \sqrt{E_{nFDA}{}^2 + E_{nOPA197}{}^2} \quad \sqrt{\left(9.28\mu V_{RMS}\right)^2 + \left(1.32\mu V_{RMS}\right)^2} = 9.37\mu V_{RMS}$$

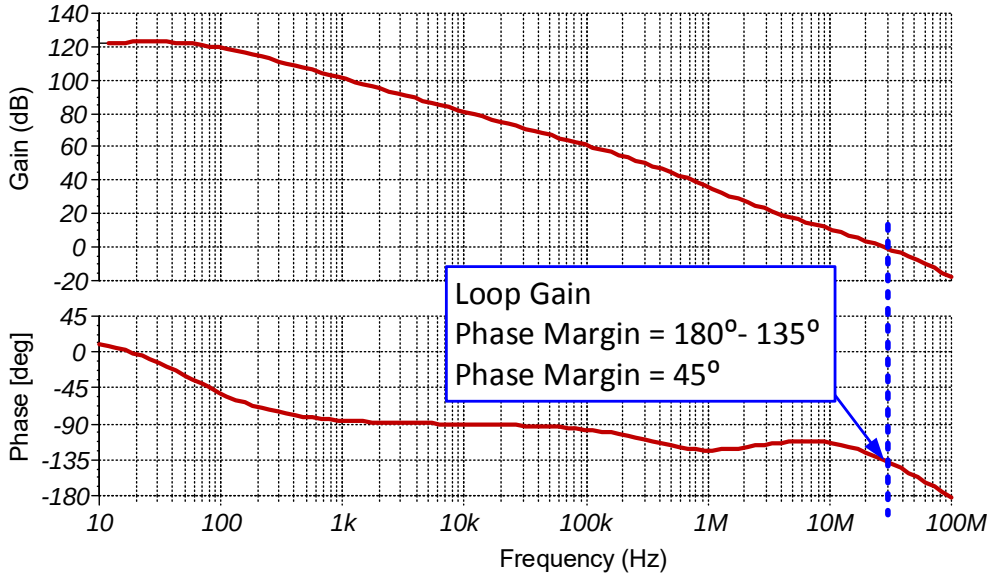
Note that calculated and simulated match well. Refer to *Calculating the Total Noise for ADC Systems* for detailed theory on this subject.



Stability Simulation

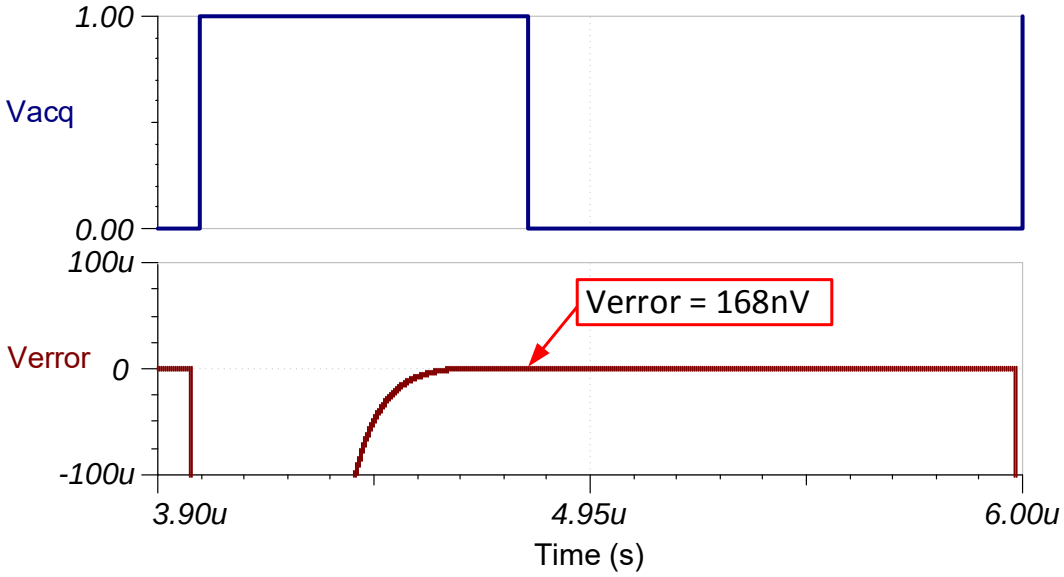
The following circuit is used in TINA to measure loop gain and verify phase margin using AC transfer analysis in TINA. Resistors R_{ISO} = 10Ω are used inside the feedback loop to increase phase margin. The circuit has 45 degrees of phase margin. Refer to *TI Precision Labs - Op Amps: Stability 4* for detailed theory on this subject.





Transient ADC Input Settling Simulation

The following simulation shows settling to a 24-V DC differential input signal with the OPA197 buffers inputs set at +12V and –12V. This type of simulation shows that the sample and hold kickback circuit is properly selected. Refer to *Refine the Rfilt and Cfilt Values* for detailed theory on this subject.



Design Featured Devices

Device	Key Features	Other Possible Devices
ADS8912B[1]	18-bit resolution, 500-ksps sample rate, integrated reference buffer, fully-differential input, Vref input range 2.5V to 5V.	Link to similar devices
THS4551	FDA, 150-MHz bandwidth, Rail-to-Rail Output, VosDriftMax = 1.8µV/°C, e_n = 3.3nV/rtHz	Link to similar devices
OPA197	36V, 10-MHz bandwidth, Rail-to-Rail Input/Output, VosMax = ±250µV, VosDriftMax = ±2.5µV/°C, bias current = ±5pA	Link to similar devices
REF5045	VREF = 4.5V, 3 ppm/°C drift, 0.05% initial accuracy, 4µVpp/V noise	Link to similar devices

(1) The REF5045 can be directly connected to the ADS8912B without any buffer because the ADS8912B has a built in internal reference buffer. Also, the REF5045 has the required low noise and drift for precision SAR applications. The THS4551 provides the attenuation and common-mode level shifting to the voltage range of the SAR ADC. In addition, this FDA is commonly used in high-speed precision fully-differential SAR applications as it has sufficient bandwidth to settle to charge kickback transients from the ADC input sampling. The OPA197 is a 36-V operational amplifier that provides a very high input impedance front end, buffering the FDA inputs

Link to Key Files

Source files for this design - http://www.ti.com/lit/zip/sbac183

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e2e.ti.com

TI Precision Labs Training Series community:

TI Precision Labs - https://training.ti.com/ti-precision-labs-overview

Circuit to Increase Input Range on an Integrated Analog Front End (AFE) SAR ADC

Cynthia Sosa

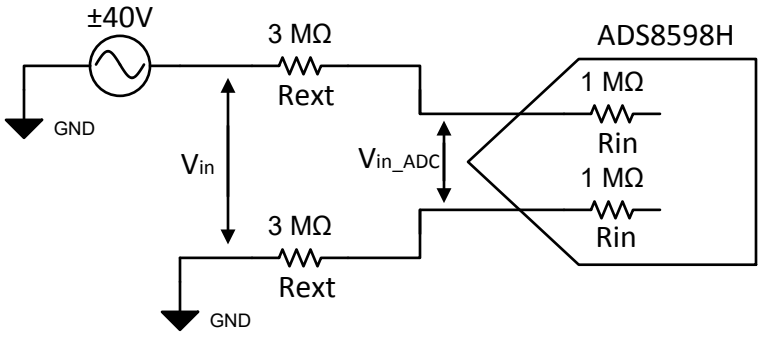
Input	ADC Input	Digital Output ADS7042
VinMin = –40V	AIN-xP = –10V	-131072_{10}
	AIN-xGND = 0V	20000_{H}
VinMax = 40V	AIN-xP = 10V	131071_{10}
	AIN-xGND = 0V	$1FFFF_{H}$

Power Supplies	
AVDD	**DVDD**
5V	3.3V

Design Description

This cookbook design describes how to expand the input range of a SAR ADC with an integrated analog front end (AFE) and decrease the loss of accuracy by implementing a two-point calibration method. This design uses the ADS8598H at the full scale range of ±10V and expands the accessible input range to ±40V. This allows for a wider input range to be used without extra analog circuitry to step down the voltage; instead a simple voltage divider is used to interact with the AFE of the device to step down the voltage near the device input. A calibration method can be implemented to eliminate any error that could occur.

A similar cookbook design, *Reducing Effects of External RC Filter on Gain and Drift Error for Integrated AFE: ±10 V, up to 200kHz, 16 bit*, explaining how to measure introduced drift from external components can prove to also be helpful in this application. Increasing the input range that the ADC can measure proves useful in end equipment such as: *Multi Function Relays*, *AC Analog Input Modules*, and *Control Units for Rail Transport*.



Specifications

Specification	Measured Accuracy Without Calibration	Measured Accuracy With Calibration
±40V	0.726318%	0. 008237%

Design Notes

1. Use low-drift resistors to decrease any error introduced due to temperature drift, such as 50 ppm/°C with 1% tolerance or better. Note that as resistor values increase to 1MΩ and beyond, low-drift precision resistors can become more expensive.
2. An input filter is frequently required for this configuration. Placing it directly after the large input impedance can cause errors because of the capacitor leakage. If an input filtering capacitor is needed, an alternate schematic is shown in this design.

Component Selection

The internal impedance of the device is 1MΩ, the external resistor is selected based on the desired extended input range (Vin), in this case ±40V. This external resistor forms a voltage divider with the internal impedance of the device, stepping down the input voltage within the ADC input range of ±10V.

1. Rearrange the voltage divider equation to solve for the external resistor value. This same equation can later be used to calculate the expected Vin_{ADC} value from the input voltage.

$$V_{in\_ADC} \quad V_{in} \cdot \frac{R_{in}}{R_{in} + R_{ext}}$$

$$R_{ext} \quad \frac{V_{in} \cdot R_{in}}{V_{in\_ADC}} - R_{in}$$

2. Solve for the external resistor value for the desired extended input voltage. Vin = ±40V, Rin = 1M Ω

$$R_{ext} \quad \frac{40V \cdot 1M\Omega}{10V} - 1M\Omega$$

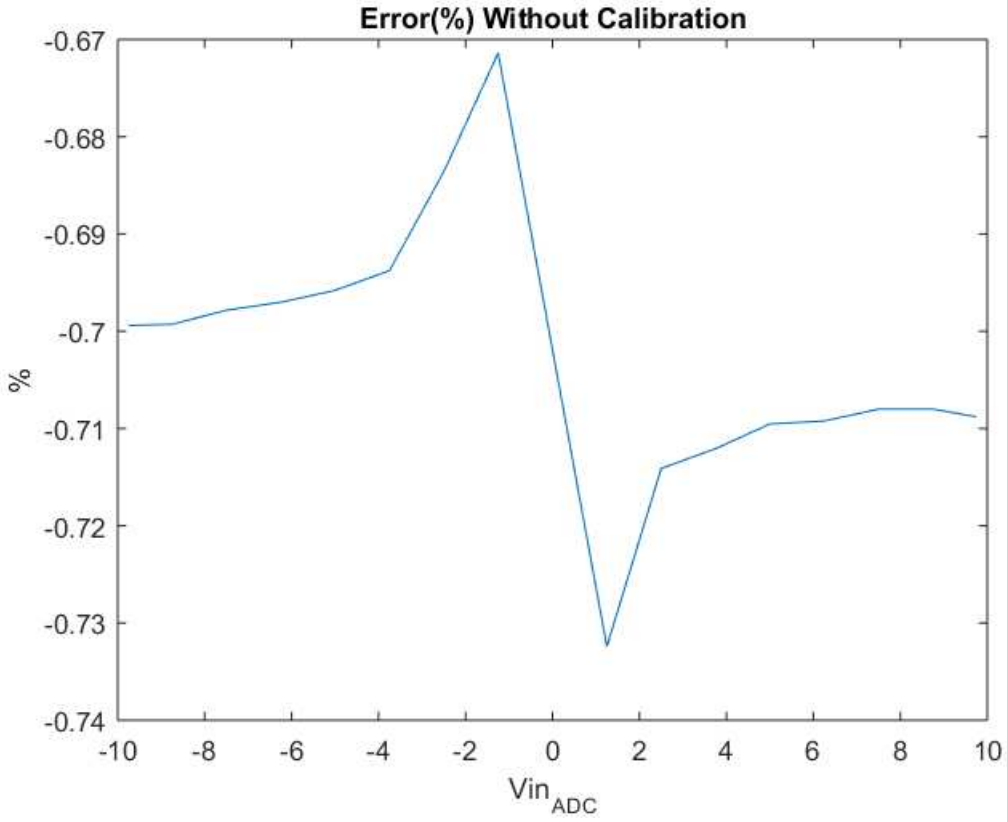
The input can be extended to a variety of ranges, depending on what external resistor value is used.

Vin	Rext
±40	3MΩ
±30	2MΩ
±20	1MΩ
±12	200kΩ

Non Calibrated Measurements

Different DC input values ranging through the full ±40-V scale were used to measure the ADC voltage input and the accuracy of the measurement. The percent error of the value was calculated using the following equation:

$$\text{Error}(\%) \quad \frac{\text{Vin}_{ADC} - \text{Vout}_{ADC}}{\text{Vin}_{ADC}} \cdot 100$$



Two-Point Calibration

Calibration can be applied in order to eliminate the reading error introduced by the external resistor. The two-point calibration applies and samples two test signals at 0.25V from the full scale input range within the linear range of the ADC. These sample measurements are then used to calculate the slope and offset of the linear transfer function. Calibration will eliminate both the gain error introduced by the external resistor and the internal device gain error.

1. Apply test signal at 9.75V:

Vmin	Measured Code
–9.75V	–128689

2. Apply test signal at –9.75V:

Vmin	Measured Code
–9.75V	128701

3. Calculate slope and offset calibration coefficients:

$$m \quad \frac{Code_{max} - Code_{min}}{V_{max} - V_{min}} \quad \frac{128701 - (-128689)}{9.75V - (-9.75V)} \quad 13199.487$$

$$b = Code_{min} - m \cdot V_{min} \quad -128689 - 13199.487 \cdot (-9.75V) = 5.998$$

4. Apply calibration coefficients to all subsequent measurements:

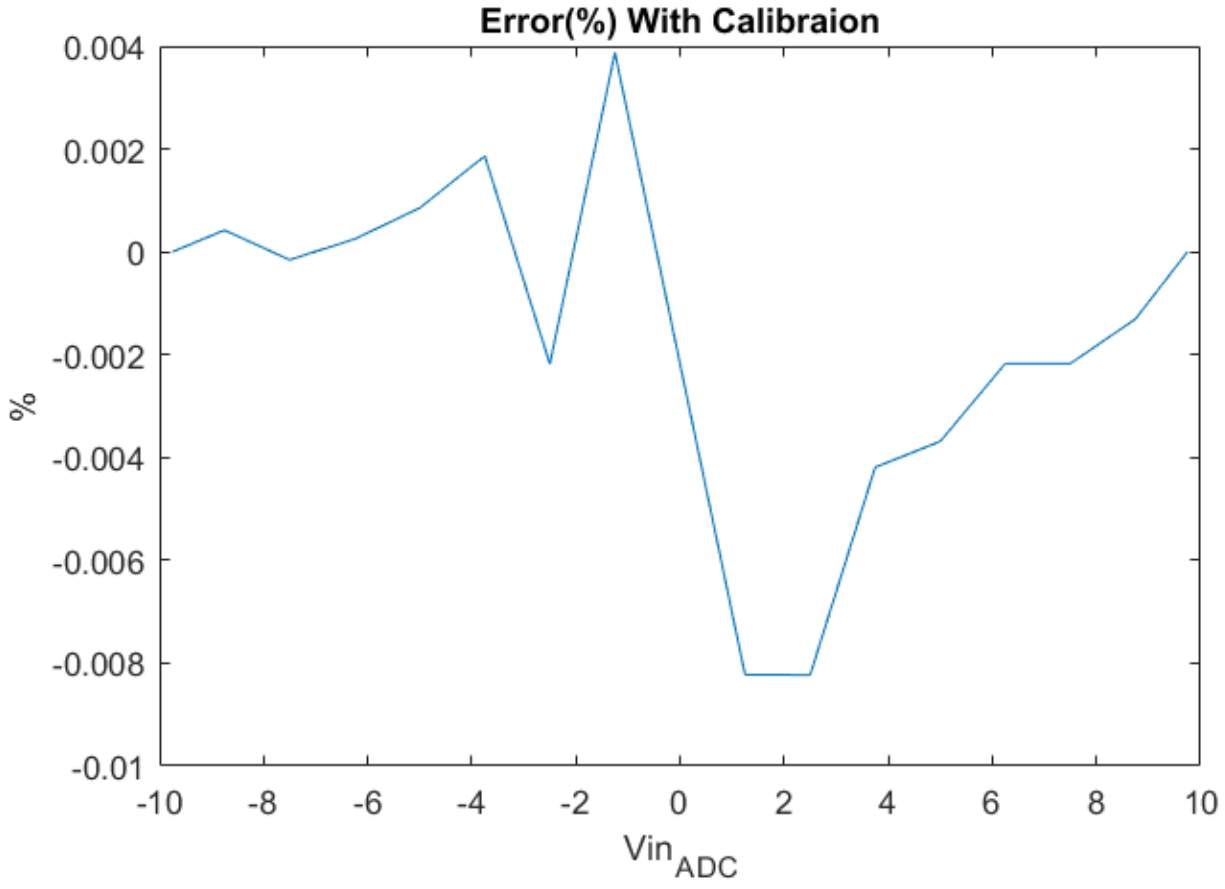
$$Vin_{ADC\_Calibrate} \quad \frac{Code - b}{m} \quad \frac{128701 - 6}{13199.487} \quad 9.5000$$

Two-Point Calibration Measurements

Calibration Coefficients

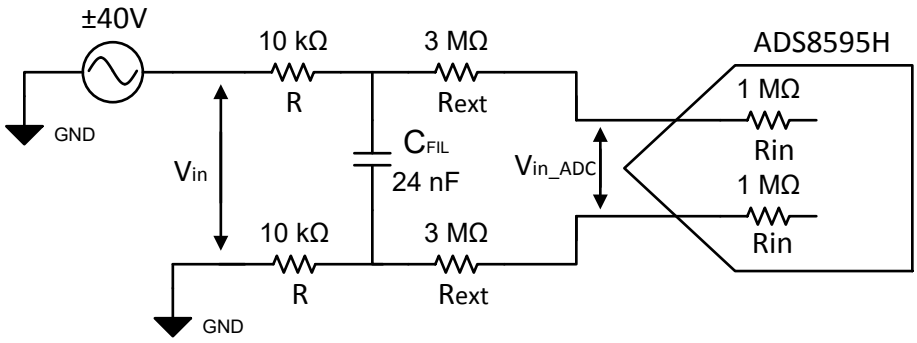
m = 13199.487; *b* = 5.998

When calibration is applied the readings error is dramatically reduced.



Alternate Schematic With Filter Capacitor

Due to the high-value resistors used, introducing a capacitor would lead to significant impact in readings, such as increase drift experienced. This is because of the capacitor leakage. This leakage will vary over time and temperature and will generate errors that are difficult to calibrate out. If an input filter is needed, the alternate schematic can be used to implement it. The capacitor is placed with a balanced resistor-capacitor filter before the external resistors in relation to the input signal.



Alternate Schematic With Filter Capacitor - Component Selection

External anti-aliasing RC filters reduce noise and protect from electrical overstress. A balanced RC filter configuration is required for better common-mode noise rejection; matching external resistors are added to both the negative and positive input paths. These external resistors should also be low-drift resistors as stated in the *Design Notes*.

1. Choose a value of R based on the desired cutoff frequency. This example uses a cutoff frequency of 320Hz, and a resistor value of 10kΩ.

   R = 10kΩ

2. Select C_{FIL}

$$C_{FIL} \quad \frac{1}{2 \cdot \pi \cdot f_c \cdot 2 \cdot R} \quad \frac{1}{2 \cdot \pi \cdot 320Hz \cdot 2 \cdot 10k\Omega} \quad 24.8nF$$

   Nearest standard capacitor value available, C_{FIL}= 24 nF

Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS8598H	18-bit high-speed 8-channel simultaneous-sampling ADC With bipolar inputs on a single supply	Datasheet	Parametric Search

For direct support from TI Engineers use the E2E community:

e2e.ti.com

Other Links

www.ti.com/adcs

www.ti.com/precisionadc

Circuit for Driving High-Voltage SAR ADCs for High-Voltage, True Differential Signal Acquisition

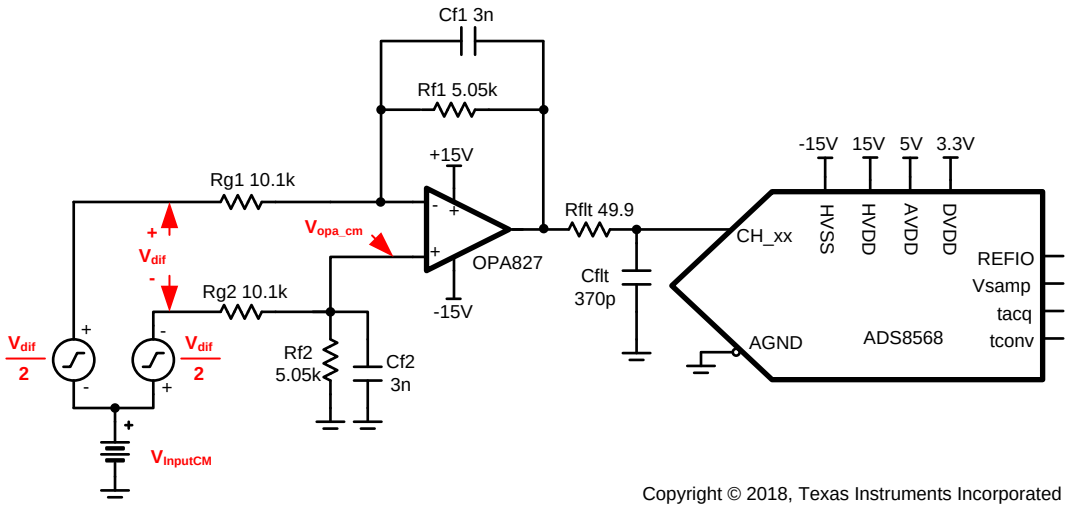
Dale Li

Input	ADC Input	Digital Output ADS7042
VinDiffMin = –20V	CH_x = +10V	7FFF $_{H}$, or 32767 $_{10}$
VinDiffMax = +20V	CH_x = –10V	8000 $_{H}$, or 32768 $_{10}$

Power Supplies			
AVDD	**DVDD**	**V_{CC} (HVDD)**	**V_{SS} (HVSS)**
5.0V	3.3V	+15V	–15V

Design Description

This design shows a solution to drive high-voltage SAR ADC to implement data capture for high-voltage fully differential signal which may have a wide common-mode voltage range depended on amplifier's power supply and input signal's amplitude. A general high-voltage precision amplifier performs the differential to single-ended conversion and drives high-voltage SAR ADC single-ended input scale of ±10V at highest throughput. This type of application is popular in end equipment such as: *Multi-Function Relays*, *AC Analog Input Modules*, and *Control Units for Rail Transport*. The values in the *component selection* section can be adjusted to allow for different level differential input signal, different ADC data throughput rates, and different bandwidth amplifiers.



Specifications

Specification	OPA827 Calculated	OPA827 Simulated	OPA192 Calculated	OPA192 Simulated
Common Mode Input Range (with Vdif = ±20V)	±26V	±26V	±35V	±35V
Transient ADC Input Settling Error	< 1/2LSB (< 152µV)	0.002 LSB (0.568µV)	< 1/2LSB (< 152µV)	0.006 LSB (1.86µV)
Phase Margin of driver	> 45°	67.1°	> 45°	68.6°
Noise (at ADC Input)	14.128µVrms	15.88µVrms	5.699µVrms	6.44µVrms

Design Notes

1. Determine the amplifier gain based on the differential input signal level, the ADC's configuration for input range. This is covered in the *component selection* section.
2. Determine amplifier's linear range based on common mode voltage, input swing, and power supplies. This is covered in the *component selection* section.
3. In this design circuit, the common-mode voltage of the input signal can be any value in the range of $V_{InputCM}$. The derivation of this range is provided in the *component selection* section for the OPA827 and OPA192.
4. Select COG capacitors to minimize distortion.
5. Use 0.1% 20ppm/°C film resistors or better for good accuracy, low gain drift, and to minimize distortion. Review *Statistics Behind Error Analysis* for methods to minimize gain, offset, drift, and noise errors.
6. Refer to *Introduction to SAR ADC Front-End Component Selection* for an explanation of how to select Rfilt and Cfilt for best settling and AC performance. These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here provide good settling and AC performance for the amplifier and data converter in this example. If the design is modified, select a different RC filter.

Component Selection

1. Find the gain based on differential input signal and ADC full-scale input range.

$$Gain_{OPA} = \frac{\pm V_{ADC(range)}}{\pm V_{DifIn(range)}} = \frac{\pm 10V}{\pm 20V} = 0.5V/V$$

2. Find standard resistor values for differential gain. Use the *Analog Engineer's Calculator* ("Amplifier and Comparator\Find Amplifier Gain" section) to find standard values for Rf/Rg ratio.

$$Gain_{OPA} = \frac{R_f}{R_g} = \frac{5.05k\Omega}{10.1k\Omega} = 0.5$$

3. Find the amplifier's maximum and minimum input for linear operation (that is, the common mode range of the amplifier, V_{cm_amp}). For this example, the OPA827 is used.

$V_- + 3V < V_{cm\_opa} < V_+ - 3V$ from the OPA827 common mode specification

$-12V < V_{cm\_opa} < 12V$ *for* $\pm 15V$ *supplies*

4. Calculate the maximum common-mode voltage range based on amplifier's input range and previously shown configuration. Refer to the schematic diagram on the first page for better understanding of how V_{cm_opa}, $V_{InputCM}$, and V_{dif} relate to the circuit.

$$V_{cm\_opa} = \left(V_{InputCM} \pm \frac{V_{dif}}{2}\right) \cdot \left(\frac{R_f}{R_f + R_g}\right)$$

$$V_{cm\_opaMin} \cdot \left(\frac{R_f + R_g}{R_f}\right) + \frac{V_{dif}}{2} < V_{InputCM} < V_{cm\_opaMax} \cdot \left(\frac{R_f + R_g}{R_f}\right) - \frac{V_{dif}}{2}$$

5. Solve the equation for the input common-mode range $V_{InputCM}$ for the amplifier. For this example (OPA827), the common mode input can be ±26V with a ±20-V differential input. Using the same method on OPA192 shows a common mode range of ±35V with a ±20-V differential input. Exceeding this common-mode range will distort the signal. Note that this common-mode range was calculated using ±15-V power supplies. The common mode range could be extended by increasing the supply (maximum ±18V).

$$V_{cm\_opaMin} \cdot \left(\frac{R_f + R_g}{R_f}\right) + \frac{V_{dif}}{2} < V_{InputCM} < V_{cm\_opaMax} \cdot \left(\frac{R_f + R_g}{R_f}\right) - \frac{V_{dif}}{2}$$

$$(-12V) \cdot \left(\frac{5.05k\Omega + 10.1k\Omega}{5.05k\Omega}\right) + \frac{20V}{2} < V_{InputCM} < (12V) \cdot \left(\frac{5.05k\Omega + 10.1k\Omega}{5.05k\Omega}\right) - \frac{20V}{2}$$

$$-26V < V_{InputCM} < 26V$$

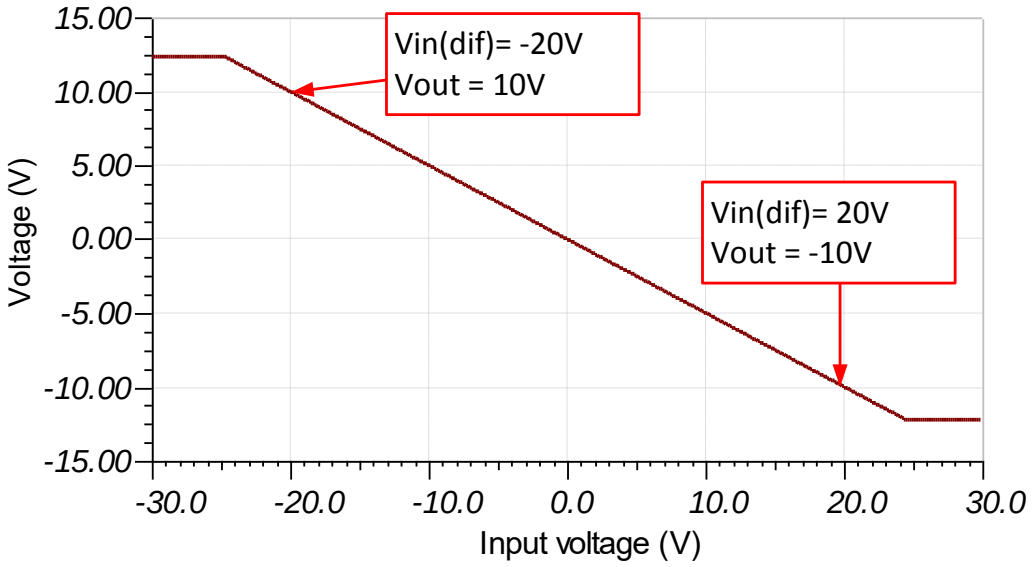
6. Find the value for Cf that will achieve the desired closed-loop bandwidth. In this example we want approximately 10-kHz bandwidth. Note: if you adjust the bandwidth you will need to verify the charge bucket filter settling (C_{filt} and R_{filt}) as the closed-loop bandwidth effects settling.

$$C_f = \frac{1}{2 \cdot \pi \cdot R_f \cdot f_c} = \frac{1}{2 \cdot \pi \cdot (5.05k\Omega) \cdot (10kHz)} = 3.1nF \quad or \quad 3nF \quad standard \quad value$$

7. Find the value for Cfilt and Rfilt using *TINA SPICE* and the methods described in *Introduction to SAR ADC Front-End Component Selection*. The value of Rfilt and Cfilt shown in this document will work for these circuits; however, if you use different amplifiers or different gain settings you must use TINA SPICE to find new values.

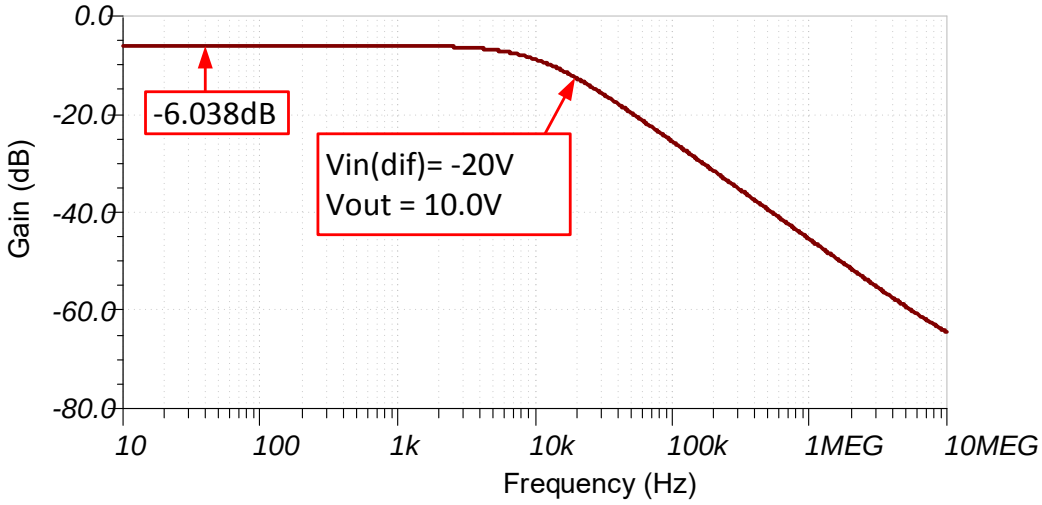
DC Transfer Characteristics

The following graph shows a linear output response for inputs from differential –20V to +20V. The full-scale range (FSR) of the ADC falls within the linear range of the op amp. Refer to *Determining a SAR ADC's Linear Range when using Operational Amplifiers* for detailed theory on this subject.



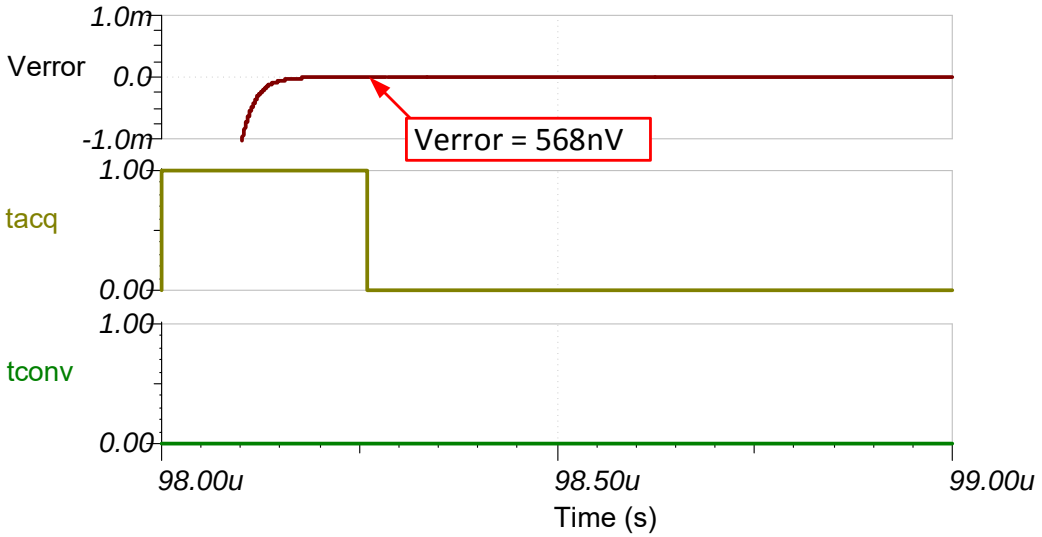
AC Transfer Characteristics

The bandwidth is simulated to be 10.58kHz and the gain is –6.038dB which is a linear gain of 0.5V/V. See the *Op Amps: Bandwidth 1* video for more details on this subject.



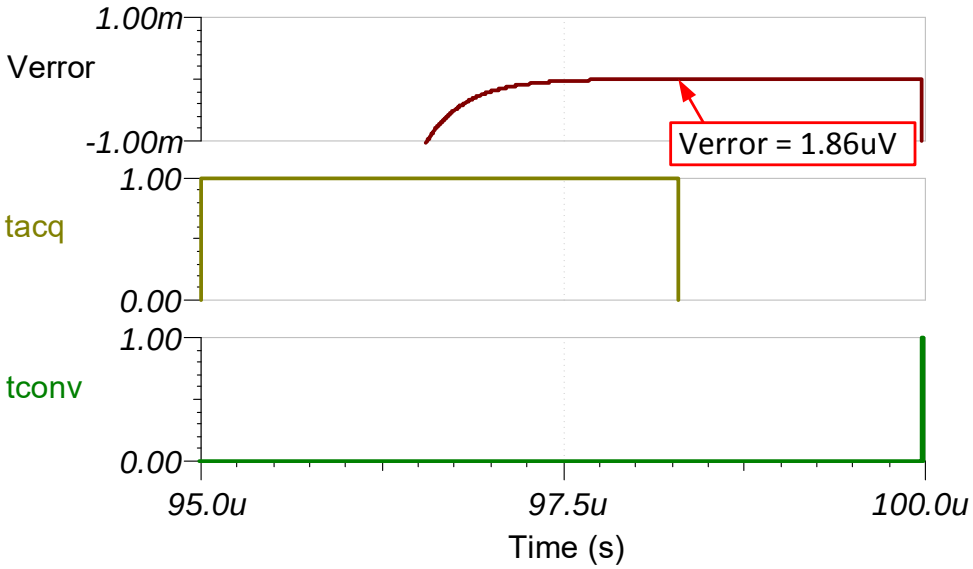
Transient ADC Input Settling Simulation Highest Sampling rate – 510ksps on ADS8568+OPA827

The following simulation shows settling to a 20-V DC input signal with OPA827. This type of simulation shows that the sample and hold kickback circuit is properly selected to within ½ of a LSB (152µV). Refer to *Introduction to SAR ADC Front-End Component Selection* for detailed theory on this subject.



Transient ADC Input Settling Simulation Lower Sampling rate – 200ksps on ADS8568+OPA192

The following simulation shows settling to a 20-V DC input signal with OPA192. This type of simulation shows that the sample and hold kickback circuit is properly selected to within ½ of a LSB (152µV).



Noise Calculation

This section demonstrates a full-noise analysis including resistor noise. Also, we look at the noise below f_c (Noise Gain = 1.5), and the noise above f_c (noise Gain = 1). In this example, the noise is dominated by wide band amplifier noise so the resistors do not contribute significantly. However, in many cases the resistor noise may be important, so the full noise calculation is provided. Refer to *Calculating the Total Noise for ADC Systems* and *Op Amps: Noise 1* for more detailed theory on this subject.

Bandwidth for feedback loop:

$$f_c = \frac{1}{2 \cdot \pi \cdot R_f \cdot C_f} = \frac{1}{2 \cdot \pi \cdot (5.05k\Omega) \cdot (3nF)} = 10.6kHz$$

Noise from OPA827: 3.8nV/rtHz

$$E_{n\_amp1} = e_{n\_827} \cdot \sqrt{K_n \cdot f_c} = (3.8nV / \sqrt{Hz}) \cdot \sqrt{(1.57) \cdot (10.6kHz)} = 490nVrms$$

Thermal noise density from feedback loop (R_{f1} and R_{g1}) and RC non-inverting input (R_{f2} and R_{g2}):

$$R_{eq} = R_f || R_g = \frac{R_f \cdot R_g}{R_f + R_g} = \frac{(5.05k\Omega) \cdot (10.1k\Omega)}{5.05k\Omega + 10.1k\Omega} = 3.37k\Omega$$

$$e_{n\_feedback} = \sqrt{4 \cdot K_n \cdot T_K \cdot R_{eq}} = \sqrt{4 \cdot \left(1.38 \cdot 10^{-23}\right) \cdot \left(298\right) \cdot \left(3.37k\Omega\right)} = 7.4nV / \sqrt{Hz}$$

$$E_{n\_feedback} = e_{n\_feedback} \cdot \sqrt{K_n \cdot f_c} = (7.4nV / \sqrt{Hz}) \cdot \sqrt{(1.57) \cdot (10.6kHz)} = 0.955\mu Vrms$$

Noise from resistors on the non-inverting input is the same as noise from the feedback resistors.

$$E_{n\_input} = E_{n\_feedback} = 0.955\mu Vrms$$

Total noise (in gain) referred to output of amplifier:

$$E_{n\_below\_fc} = (G_n) \sqrt{E_{n\_amp1}^2 + E_{n\_feedback}^2 + E_{n\_input}^2}$$

$$E_{n\_below\_fc} = (1.5) \sqrt{(0.49\mu V)^2 + (0.995\mu V)^2 + (0.995\mu V)^2} = 2.155\mu Vrms$$

Noise above fc is limited by the output filter (cutoff given below):

$$f_{output} = \frac{1}{2 \cdot \pi \cdot R_{filt} \cdot C_{filt}} = \frac{1}{2 \cdot \pi \cdot (49.9\Omega) \cdot (370pF)} = 8.6MHz$$

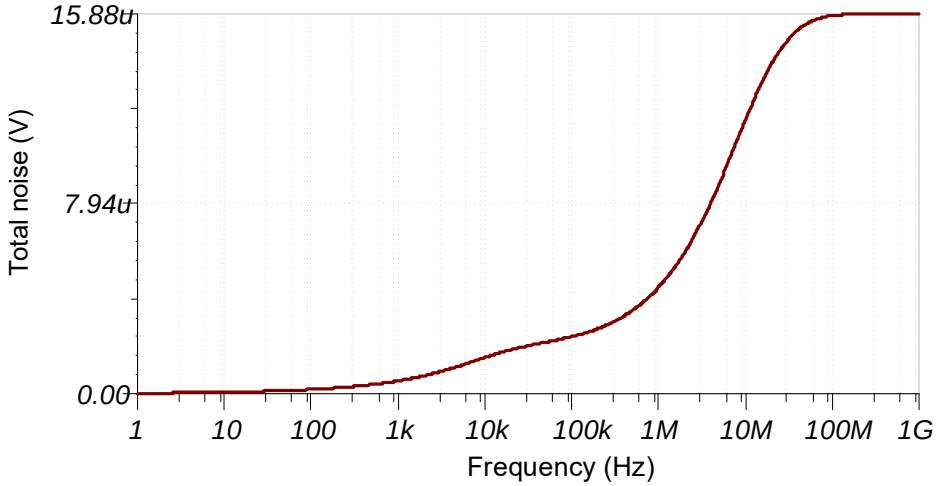
$$E_{n\_above\_fc} = e_{n\_827} \cdot \sqrt{K_n \cdot f_{output}} = (2.8nV / \sqrt{Hz}) \cdot \sqrt{(1.57) \cdot (8.6MHz)} = 13.963\mu V$$

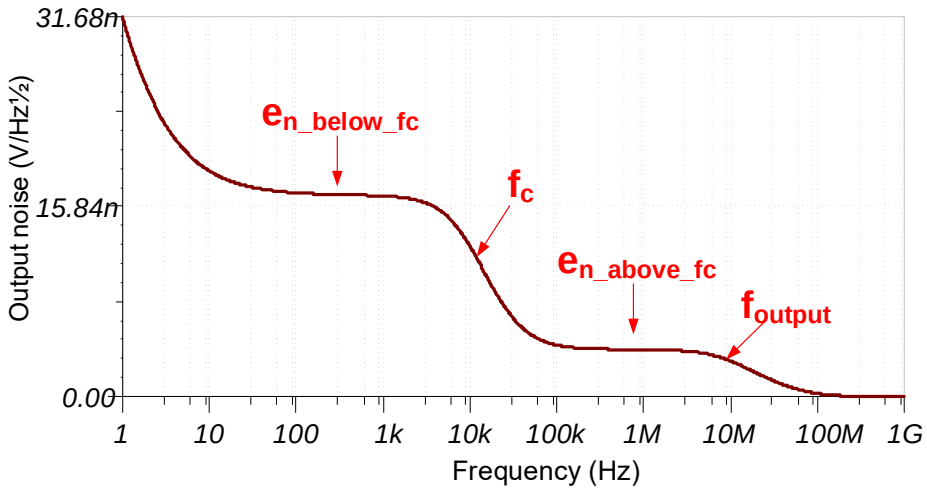
Total noise applied to input of the ADC:

$$E_{n\_total} = \sqrt{E_{n\_below\_fc}^2 + E_{n\_above\_fc}^2} = \sqrt{(2.155\mu V)^2 + (13.963\mu V)^2} = 14.128\mu Vrms$$

Noise Simulation

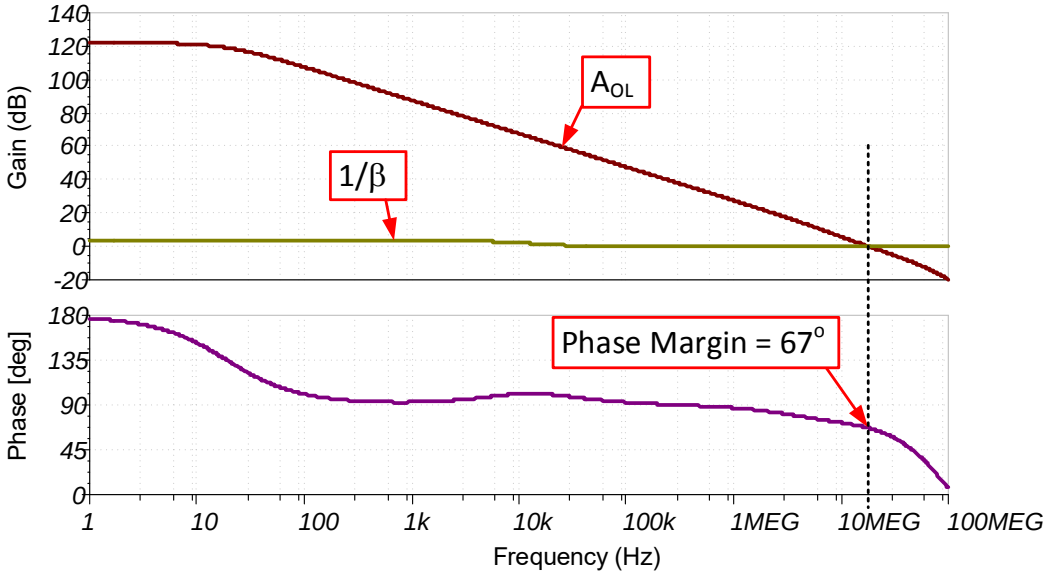
The simulated results compare well with the calculated results (that is, simulated = 15.88μVrms, calculated = 14.128μVrms).

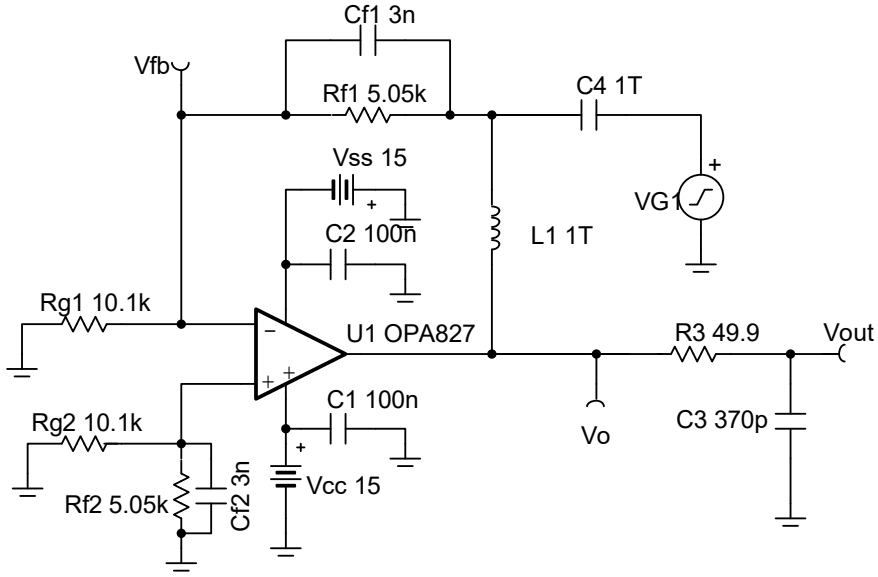




Stability Test

The phase margin for this OPA827 driving circuit is 67.1°, which meets the >45° requirement and is stable. Refer to *Op Amps: Stability 1* for detailed theory explaining stability analysis.





Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS8568[(1)]	16-bit, 8 Channel Simultaneous-Sampling, Bipolar-Input SAR ADC	http://www.ti.com/product/ADS8568	Similar Devices
OPA827	Low-Noise, High-Precision, JFET-Input Operational Amplifier	http://www.ti.com/product/OPA827	Precision Op Amps - Products
OPA192	High-Voltage, Rail-to-Rail Input/Output, 5μV, 0.2μV/°C, Precision operational amplifier	http://www.ti.com/product/OPA192	Precision Op Amps - Products

(1) The ADS8568 has integrated a precision voltage reference which can meet most design requirements, but an external REF5050 can be directly connected to the ADS8568 without any additional buffer because the ADS8568 has a built in internal reference buffer for every ADC channel pair. Also, REF5050 has the required low noise and drift for precision SAR applications. C1 is added to balance CMRR (common-mode rejection ratio). Clean analog power supplies are required to achieve best performance specified in the data sheet of the ADC.

Link to Key Files (TINA)

Design files for this circuit (http://www.ti.com/lit/zip/sbac180)

For direct support from TI Engineers use the E2E community:

e2e.ti.com/

TI Precision Labs Training Series

TI Precision Labs - https://training.ti.com/ti-precision-labs-overview

Other Links

www.ti.com/adcs

High-Current Battery Monitor Circuit: 0-10 A, 0-10 kHz, 18 Bit

Luis Chioye

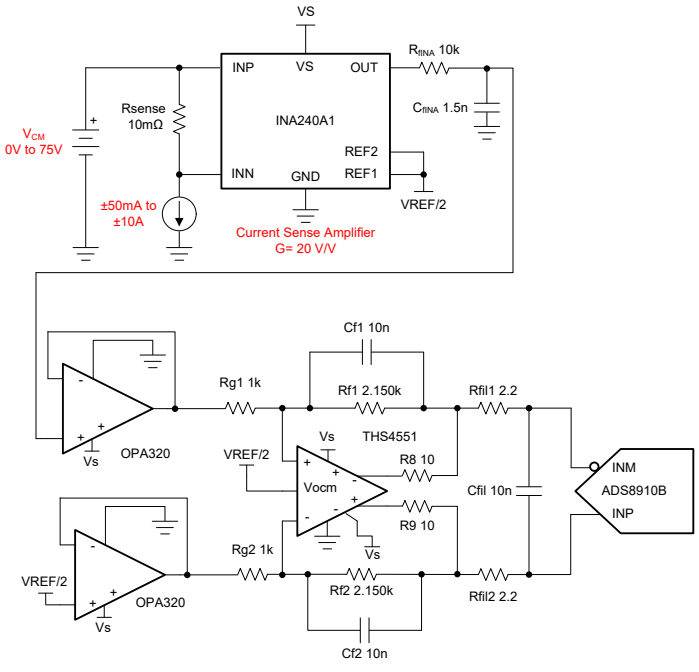
Sense Resistor Current	INA Out, Amplifier Input	ADC Input	Digital Output ADS8910B
MinCurrent = ±50mA	Out = ±10mV	VoutDif = ±21.3mV	233_H 563_{10}, $3FDCB_H$ -564_0
MaxCurrent = +10A	Out = ±2V	VoutDif = ± 4.3V	$1B851^H$ 112722_{10} $247AE_H$ -112722_{10}

Supply and Reference			
Vs	**Vee**	**Vref**	**Vcm**
5.3 V <Vs <5.5V	0V	5V	2.5V

Design Description

This single-supply current sensing solution can measure a current signal in the range of ±50 mA to ±10 A across a shunt resistor. The current sense amplifier can measure shunt resistors over a wide common-mode voltage range from 0V to 75V. A fully differential amplifier (FDA) performs the single-ended to differential conversion and drives the SAR ADC differential input scale of ±5V at full data rate of 1MSPS. The values in the *component selection* section can be adjusted to allow for different current levels.

This circuit implementation is applicable in accurate voltage measurement applications such as Battery Maintenance Systems, Battery Analyzers, *Battery Testing Equipment*, *ATE*, and Remote Radio Units (RRU) in wireless base stations.



Specifications:

Error Analysis	Calculated	Simulated	Measured
Transient ADC Input Settling	> 1LSB > 38µV	6.6µV	N/A
Noise (at ADC Input)	221.8µV rms	207.3µV rms	227µV rms
Bandwidth	10.6kHz	10.71kHz	10.71kHz

Design Notes

1. Determine the shunt sense resistor value and select the current sense amplifier based on the input current range and input common mode voltage requirements. This is covered in the *component selection* section.
2. Determine the fully differential amplifier gain based on the current sense amplifier output, the ADC full-scale range input and the output swing specifications of the fully differential amplifier. This is covered in the *component selection* section.
3. Select COG capacitors to minimize distortion.
4. Use 0.1% 20ppm/°C film resistors or better for good accuracy, low gain drift, and to minimize distortion.
5. The TI Precision Labs training video series covers methods for error analysis. Review the following links for methods to minimize gain, offset, drift, and noise errors: *Error and Noise*.
6. The *TI Precision Labs – ADCs* training video series covers methods for selecting the charge bucket circuit R_{filt} and C_{filt}. These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here will give good settling and ac performance for the amplifier, gain settings, and data converter in this example. If the design is modified, select a different RC filter. Refer to *Introduction to SAR ADC Front-End Component Selection* for an explanation of how to select the RC filter for best settling and ac performance.

Component Selection for Current Sense Circuit

1. Choose the Rsense resistor and find the gain for the current sense amplifier (bidirectional current).

$$R_{sh} = \frac{V_{sh(max)}}{I_{load(max)}} = \frac{100mV}{10A} = 0.01\Omega$$

$$\pm V_{out(range)} = \pm \frac{V_{REF}}{2} = \pm \frac{5V}{2} = \pm 2.5V$$

$$G_{INA} = \frac{\pm V_{out(range)}}{I_{load(max)} \cdot R_{sh}} = \frac{\pm 2.5V}{10A \cdot 0.01\Omega} = 25V/V$$

2. Calculate the current sense amplifier output range.

$$V_{ina\_outmax} = G_{INA} \cdot (I_{load(max)} \cdot R_{sh}) + \frac{V_{ref}}{2} = (20V/V) \cdot (10A \times 0.01\Omega) + \frac{5V}{2} = 4.5V$$

$$V_{ina\_outmax} = G_{INA} \cdot (I_{load(max)} \cdot R_{sh}) + \frac{V_{ref}}{2} = (20V/V) \cdot (-10A \cdot 0.01\Omega) + \frac{5V}{2} = 0.5V$$

3. Find ADC full-scale input range and results from step 3.

$$ADC_{Full-Scale\ Range} = \pm V_{REF} = \pm 5V$$

4. Find FDA maximum and minimum output for linear operation.

$0.23V < V_{out} < 4.77V$ from THS4551 output low / high specification for linear operation

$V_{out\_FDA\_max} = 4.77V - 0.23V = 4.54V$ Differential max output

$V_{out\_FDA\_min} = -V_{out\_FDA\_max} = -4.54V$ Differential min output

5. Find differential gain based on ADC full-scale input range, FDA output range and results from step 3.

$$Gain = \frac{V_{out\_FDA\_max} - V_{out\_FDA\_min}}{V_{INA\_outmax} - V_{INA\_outmin}} = \frac{4.54V - (-4.54V)}{4.5V - 0.5V} = 2.77V/V$$

$Gain \approx 2.15V/V$ for margin

6. Find standard resistor values for differential gain.

$$Gain_{FDA} = \frac{R_f}{R_g} = 2.15V/V$$

$$\frac{R_f}{R_g} = 2.15V/V = \frac{2.15k\Omega}{1.00k\Omega} = 2.15V/V$$

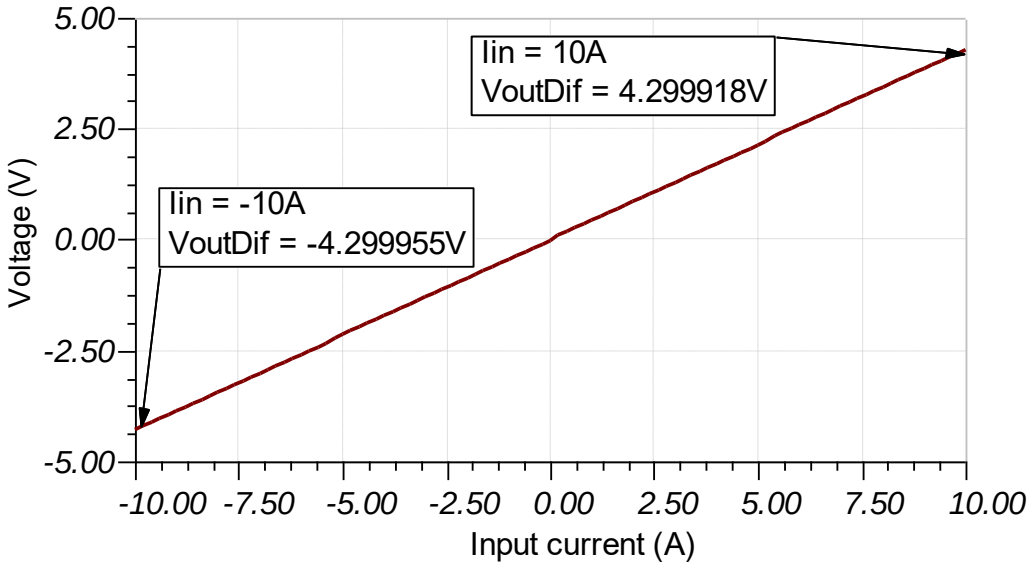
7. Find R_{flNA}, C_{flNA} for cutoff frequency.

$$C_{flNA} = \frac{1}{2 \cdot \pi \cdot f_c \cdot R_{flNA}} = \frac{1}{2 \cdot \pi \cdot 10kHz \cdot 10k\Omega} = 1.591nF \text{ or } 1.5nF \text{ for standard value}$$

$$f_{fina} = \frac{1}{2 \cdot \pi \cdot C_{flNA} \cdot R_f} = \frac{1}{2 \cdot \pi \cdot 1.5nF \cdot 10k\Omega} = 10.6kHz$$

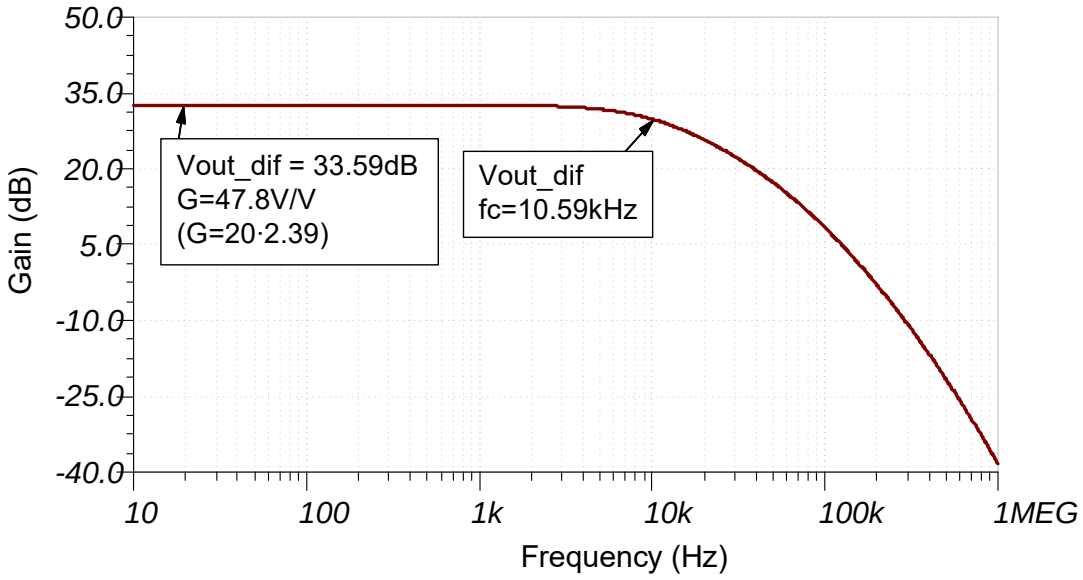
Fully Differential DC Transfer Characteristics

The following graph shows a linear output response for inputs from –10A to +10A.



AC Transfer Characteristics

The bandwidth is simulated to be 10.5kHz and the gain is 32.66dB which is a linear gain of 43V/V (G = 20·2.15V/V).



Noise Simulation

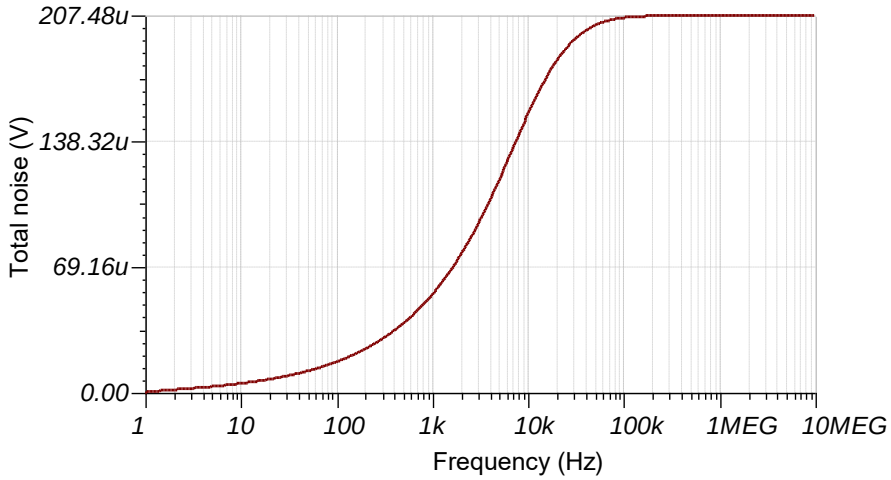
The following simplified noise calculation is provided for a rough estimate. Since the current sense amplifier INA240 is the dominant source of noise, the noise contribution of the OPA320 buffers and THS4521 is omitted in the noise estimate. We neglect resistor noise in this calculation as it is attenuated for frequencies greater than 10.6kHz.

$$f_C = \frac{1}{2\pi \cdot R_{flNA} \cdot C_{flNA}} = \frac{1}{2\pi \cdot 10k\Omega \cdot 1.5nF} = 10.6kHz$$

$$E_{nINA240} = e_{nINA240} \cdot G_{INA} \cdot \sqrt{K_n \cdot f_C} = (40nV/\sqrt{Hz}) \cdot (20V/V) \cdot \sqrt{1.57 \cdot 10.6kHz} = 103.2\mu V$$

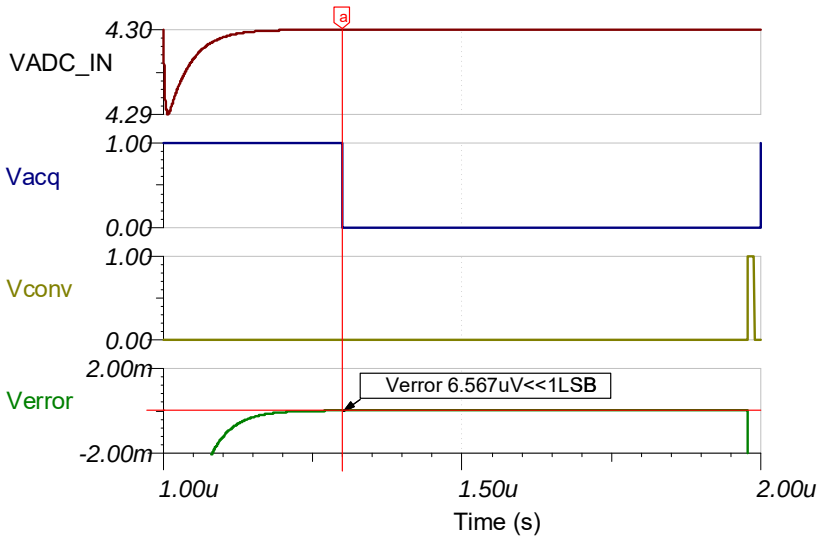
$$E_{nADCIN} = E_{nINA240} \cdot G_{FDA} = (103.2\mu Vrms) \cdot (2.15V/V) = 221.8\mu Vrms$$

Note that calculated and simulated match well. Refer to *Op Amps: Noise 4* for detailed theory on amplifier noise calculations, and *Calculating Total Noise for ADC Systems* for data converter noise.



Transient ADC Input Settling Simulation

The following simulation shows settling to a 10-A DC input signal (ADC differential input signal +4.3V). This type of simulation shows that the sample and hold kickback circuit is properly selected. Refer to *Final SAR ADC Drive Simulations* for detailed theory on this subject.



Design Featured Devices:

Device	Key Features	Other Possible Devices
ADS8910B[1]	18-bit resolution, 1-Msps sample rate, integrated reference buffer, fully differential input, Vref input range 2.5V to 5V	Parametric Search
INA240	High- and low-Side, bi-directional, zero-drift current sense amp, GainError = 0.20%, Gain = 20V/V, wide common-mode = –4V to 80V	www.ti.com/precisionamp
THS4551	Fully differential amplifier (FDA), 150-MHz bandwidth, Rail-to-Rail output, VosDriftMax = 1.8 µV/°C, e_n = 3.3 nV/rtHz	THS4551
OPA320	20-MHz bandwidth, Rail-to-Rail with zero crossover distortion, VosMax = 150 µV, VosDriftMax = 5 µV/C, e_n = 7 nV/rtHz	www.ti.com/opamp
REF5050	3 ppm/°C drift, 0.05% initial accuracy, 4 µVpp/V noise	www.ti.com/vref

(1) The REF5050 can be directly connected to the ADS8910B without any buffer because the ADS8910B has a built in internal reference buffer. Also, the REF5050 has the required low noise and drift for precision SAR applications. The INA240 offers high common-mode range and low gain error in current sensing solutions. The THS4551 is commonly used in high-speed precision fully differential SAR applications as it has sufficient bandwidth to settle to charge kickback transients from the ADC input sampling. The OPA320 is required to isolate the INA240 from any residual charge kickback at the inputs of the FDA..

Link to Key Files

ADS8900B Design File (http://www.ti.com/lit/zip/sbam340)

For direct support from TI Engineers use the E2E community:

e2e.ti.com/

Other Links

www.ti.com/adcs

www.ti.com/precisionadc

Low-Input Bias Current Front End SAR ADC Circuit

Mike Stout

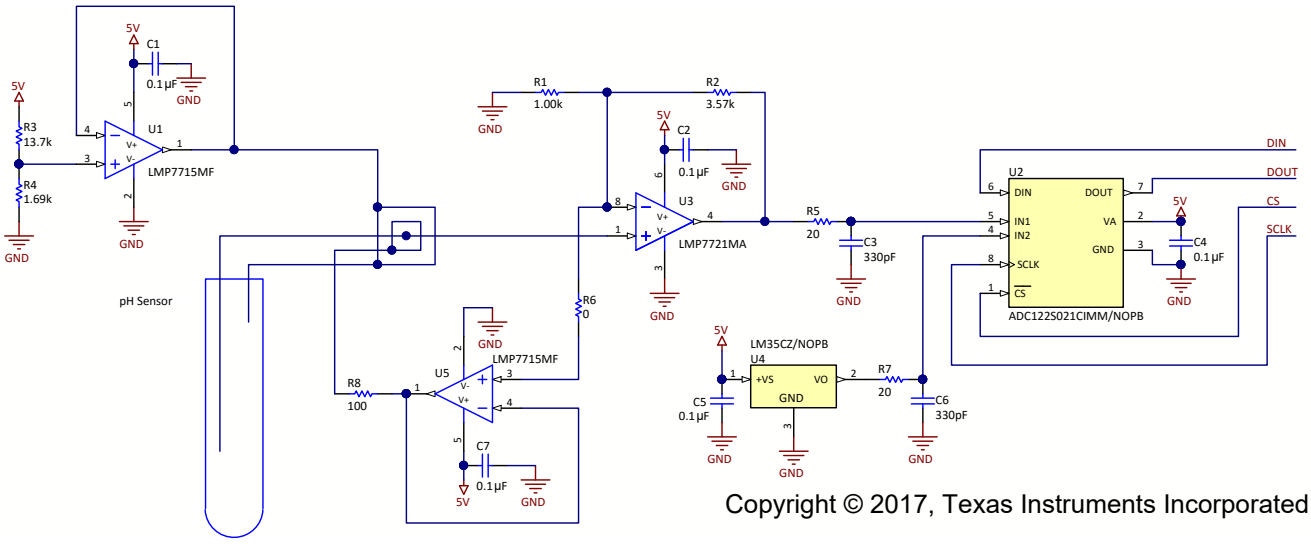
Input	ADC Input	Digital Output ADC122S021
VinMin = 0.03V	IN1 = 0.14	115 = 0x073
VinMax = 1.07V	IN1 = 4.88	3998 = 0xF9E
VinMin = 0V	IN2 = 0V	0 = 0x000
VinMax = 1V	IN2 = 1V	819 = 0x333

Power Supplies	
V+, VA	V–
5V	0V

Design Description

This design shows a low Ibias amplifier being used to drive a SAR ADC. A sensor with high output impedance requires an amplifier with a low input bias current to minimize errors. Examples of applications where this type of sensor might be used include *gas detectors*, *blood gas analyzers*, and *air quality detectors*. In this design, a pH probe is used for the sensor. The output impedance of a pH probe can be from 10MΩ to 1000MΩ. If a pH probe is used that has an output impedance of 10MΩ with an op amp that has 3nA of input bias current, the error due to the input bias current of the op amp will be 30mV. Using the input signal amplitude and gain described in the *component selection* section, this 30mV equates to an error of about 2.9%. If an op amp with an input bias current of 3fA is used, the error is decreased to 30nV.

The output of the pH sensor does not quickly change, so a lower speed ADC can be used. The value from the pH sensor changes as the temperature changes so a two channel ADC was selected so that one channel could be used to monitor the temperature. The ADC122S021 used in this design is a 2-channel, 12-bit, ADC that can sample up to 200ksps.



Specifications

Specification	Calculated	Simulated	Measured
Ibias	20fA	118fA	20fA

Design Notes

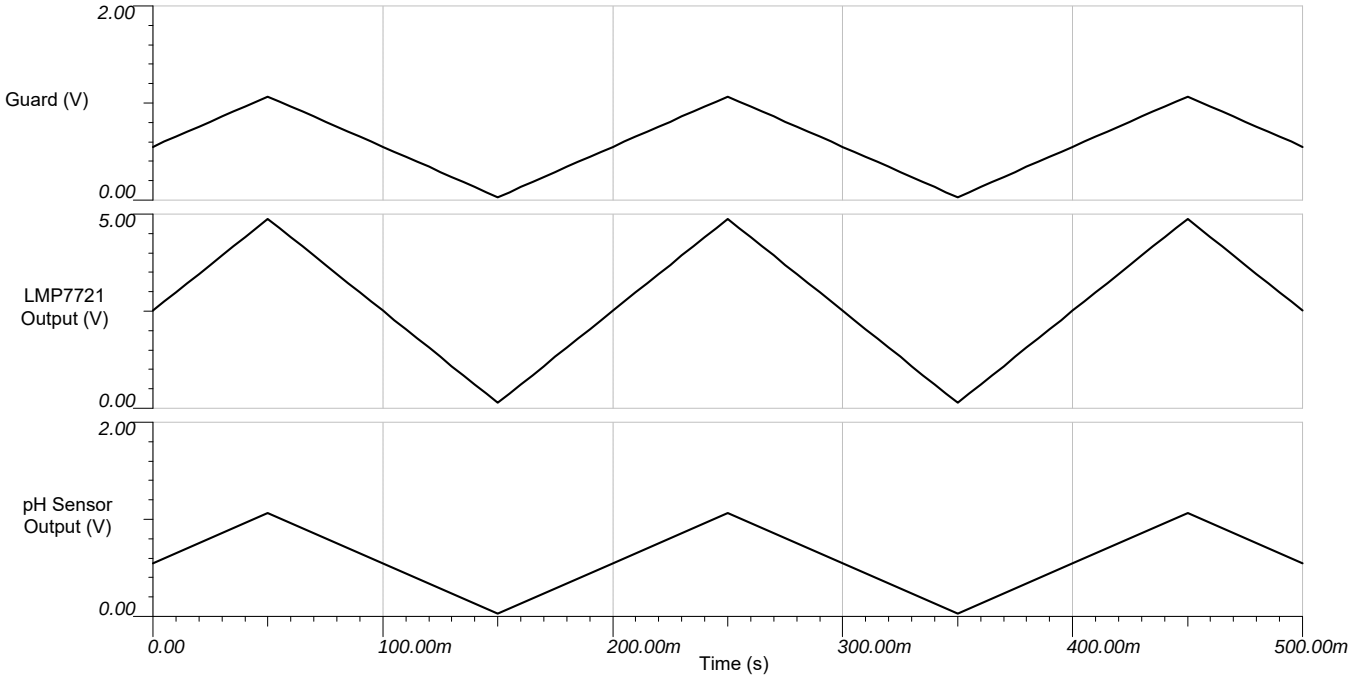
1. Use COG (NPO) capacitors for C3 and C6.
2. Each IC should have a bypass capacitor of 0.1μF.
3. PCB layout is very important. See the *LMP7721 Multi-Function Evaluation Board Users' Guide*.
4. The PCB must be clean. See the *LMP7721 Multi-Function Evaluation Board Users' Guide*.
5. For more information on low leakage design, see *Design femtoampere circuits with low leakage*.

Component Selection

1. The output voltage of a pH sensor changes as the temperature changes. At 0°C it outputs 54.2mV/pH, at 25°C it outputs 59.16mV/pH, and at 100°C it outputs 74.04mV/pH. This means that the maximum swing of the pH sensor around the bias point of the pH sensor will be ±518.3mV at 100°C. The maximum output of the LMP7721 should be limited to ±2.4V to allow for headroom. That sets the gain of the LMP7721 at:
   2.4V / 0.5183V = 4.6V/V
   Setting resistors R2 = 3.57kΩ and R1 = 1kΩ, will set this gain.
2. Since the input of the LMP7721 must be from 0V to 5V, the pH sensor needs to be biased above ground. Resistors R3 = 13.7kΩ and R4 = 1.69kΩ in a voltage divider configuration will set the input of U1 to:
   5V · 1.69kΩ / (1.69kΩ + 13.7kΩ) = 549mV
   U1 has a gain of 1V/V so the bias of the pH sensor will also be at 549mV. Since the pH sensor can swing –518.3mV below the bias point, this keeps the input of the LMP7721 above ground. The output of the LMP7721 will be centered at:
   0.549V · 4.6V/V = 2.52V
   and can swing ±2.4V above and below the center point.
3. U5 is used to set the voltage of the guard ring. It is set with a gain of 1V/V and the input is the signal on the –IN pin of the LMP7721.
4. The output of the LMP7721 is connected to one of the inputs of the ADC122S021 SAR ADC. The sampling capacitor of the ADC is 33pF and the external capacitor placed next to the pin of the ADC should be 10 times larger, or 330pF. A small resistor of 20Ω is added in series to isolate the capacitor from the LMP7721.
5. Because the output of the pH sensor changes as the temperature changes the LM35, a temperature sensor, is connected to channel 2 of the ADC122S021. A 330-pF capacitor along with a 20-Ω series resistor is used on the output of the temperature sensor.

DC Transfer Characteristics

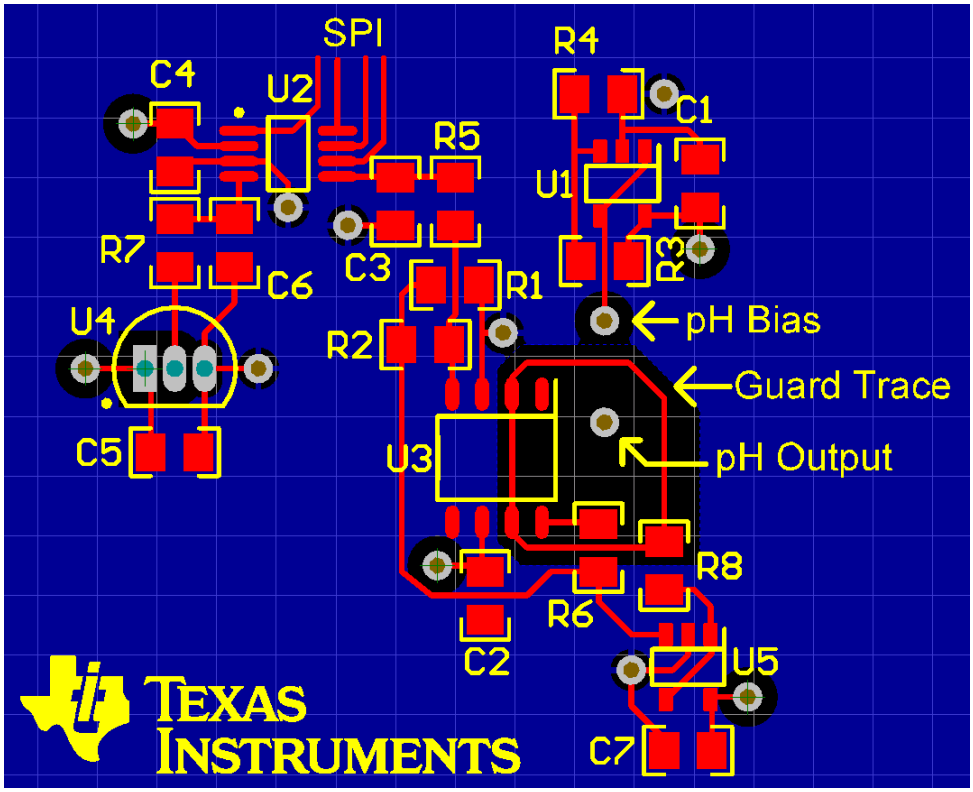
The following graph shows the pH sensor input to the LMP7721, the Guard voltage, and the LMP7721 output. This data is for 100°C, when the pH sensor output has the largest possible output swing.



Layout

The PCB layout is very important for a low Ibias circuit. Current leakage will occur between two traces when there a voltage potential between the traces. This is the reason for the guard trace. The guard trace is set to a voltage close to the input voltage to minimize the leakage between the input of the LMP7721 and the outside world. The LMP7721 includes two unused pins (pins 2 and 7) that can be used to simplify the layout of a guard trace.

The following image shows a sample layout. The output of the pH sensor and the +IN input of the LMP7721 are separated from the rest of the circuit by the guard trace, which is close to the input voltage. This will minimize the leakage on the input of the LMP7721. The bias of the pH sensor is located outside of the guard. Leakage between the bias point and the rest of the circuit is not important. Solder mask should not cover the area inside the guard trace. If there is a ground plane on the bottom side of the board or other internal planes, they should have a 'keep out' area underneath the guard area.



Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADC122S021	12 bit, SPI, 2 channel, 50ksps to 200ksps, single ended input	http://www.ti.com/product/adc122s021	http://www.ti.com/adcs
LMP7721	Ultra-low input bias current of 3fA, with a specified limit of ±20fA at 25°C, offset voltage ±26µV, GBW 17MHz	http://www.ti.com/product/lmp7721	http://www.ti.com/opamps
LMP7715	Input offset voltage ±150µV, input bias current 100fA, input voltage noise 5.8nV/√Hz, gain bandwidth product 17MHz	http://www.ti.com/product/lmp7715	http://www.ti.com/opamps
LM35	Calibrated directly in degrees Celsius, Linear + 10-mV/°C scale factor, 0.5°C ensured accuracy (at 25°C), rated for full –55°C to 150°C range	http://www.ti.com/product/lm35	http://www.ti.com/sensing-products/temperature-sensors/overview.html

For direct support from TI Engineers use the E2E community:

e2e.ti.com

Other Links:

www.ti.com/adcs

www.ti.com/data-converters/adc-circuit/precision-adcs/overview.html

Circuit for Driving a Switched-Capacitor SAR ADC with an Instrumentation Amplifier

Art Kay, Bryan McKay

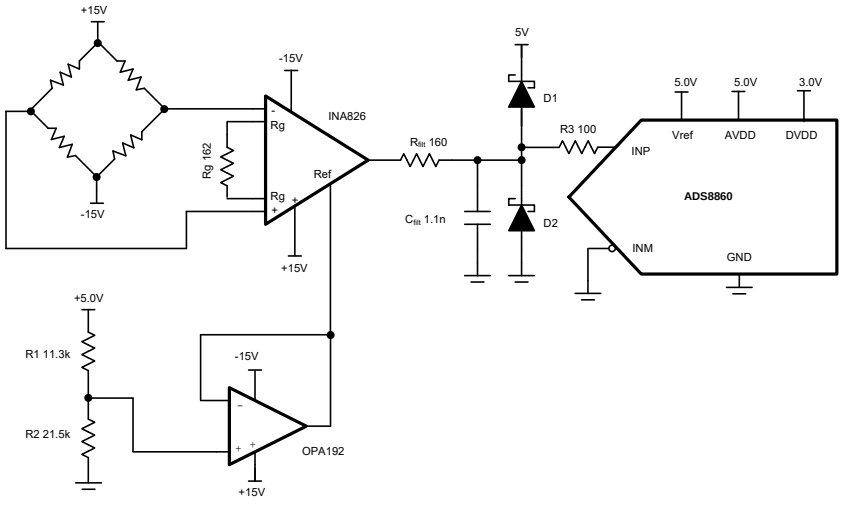
Input	ADC Input	Digital Output ADS8860
–5mV	Out = 0.2V	$0A3D_{H}$ or 2621_{10}
15mV	Out = 4.8V	$F5C3_{H}$ or 62915_{10}

Power Supplies					
AVDD	DVDD	V_{ref_INA}	V_{ref}	V_{cc}	V_{ee}
5.0V	3.0V	3.277V	5.0V	+15V	–15V

Design Description

Instrumentation amplifiers are a common way of translating low level sensor outputs to high level signals to drive an ADC. Typically, instrumentation amplifiers are optimized for low noise, low offset, and low drift. Unfortunately, the bandwidth of many instrumentation amplifiers may not be sufficient to achieve good settling to ADC charge kickback at maximum sampling rates. This document shows how sampling rate can be adjusted to achieve good settling. Furthermore, many instrumentation amplifiers are optimized for high-voltage supplies and it may be required to interface the high-voltage output (that is, ±15V) to a lower voltage ADC (for example, 5V). This design shows how to use Schottky diodes and a series resistor to protect the ADC input from an overvoltage condition. Note that the following circuit shows a bridge sensor, but this method could be used for a wide range of different sensors. A modified version of this circuit, *Driving a Switched-Capacitor SAR With a Buffered Instrumentation Amplifier* shows how a wide bandwidth buffer can be used to achieve higher sampling rate.

This circuit implementation is applicable to all *Bridge Transducers in PLC's* and *Analog Input Modules* that require Precision Signal-Processing and Data-Conversion.



Specifications

Specification	Calculated	Simulated
Sampling rate	200ksps	200ksps, settling to –6µV
Offset (ADC Input)	40µV · 306.7 = 12.27mV	16mV
Offset Drift	(0.4µV/ºC) · 306.7 = 123µV/ºC	NA
Noise	978µV	874µV

Design Notes

1. Select the gain to achieve an input swing that matches the input range of the ADC. Use the instrumentation amplifier reference pin to shift the signal offset to match the input range. This is covered in the *component selection* section.
2. The input Schottky diode configuration is used to prevent driving the input voltage outside of the absolute maximum specifications. The BAT54S Schottky is a good option for design as this device integrates both diodes into one package and the diodes are low leakage and have a low forward voltage. This is covered in the *component selection* section.
3. The buffer amplifier following the voltage divider is required for driving the reference input of most instrumentation amplifiers. Choose precision resistors and a precision low-offset amplifier as the buffer. Refer to *Selecting the right op amp* for more details on this subject.
4. Check the common-mode range of the amplifier using the *Common-Mode Input Range Calculator for Instrumentation Amplifiers* software tool.
5. Select C0G capacitors for C_{CM1}, C_{CM2}, C_{DIF}, and C_{filt} to minimize distortion.
6. Use 0.1% 20ppm/°C film resistors or better for the gain set resistor R_g. The error and drift of this resistor will directly translate into gain error and gain drift.
7. The *TI Precision Labs – ADCs* training video series covers methods for selecting the charge bucket circuit R_{filt} and C_{filt}. Although this method was designed for op amps, it can be modified for instrumentation amplifiers. Refer to *Introduction to SAR ADC Front-End Component Selection* for details on this subject.

Component Selection

1. Find the gain set resistor for the instrumentation amplifier to set the output swing to 0.2V to 4.8V.

$$\text{Gain} \quad \frac{V_{out\_max} - V_{out\_min}}{V_{in\_max} - V_{in\_min}} \quad \frac{4.9V - 0.2V}{5mV - (-10mV)} \quad 306.7$$

$$\text{Gain} = 1 + \frac{49.4k\Omega}{R_g}$$

$$R_g \quad \frac{49.4k\Omega}{\text{Gain} - 1.0} \quad \frac{49.4k\Omega}{(306.7) - 1.0} \quad 151.6\Omega \text{ or } 162\Omega \text{ for standard 0.1\% resistor}$$

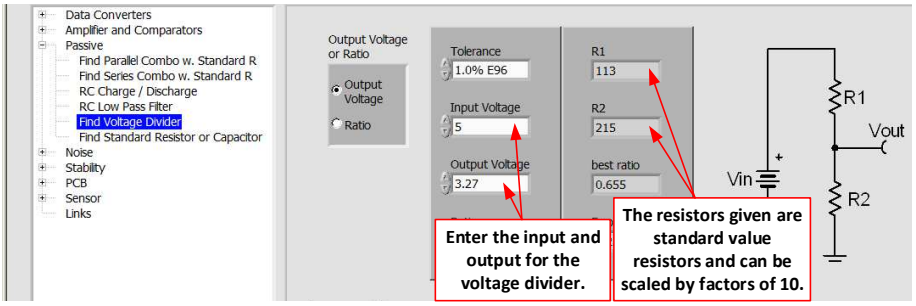
2. Find the INA826 reference voltage (V_{ref}) to shift the output swing to the proper voltage level.

$$V_{out} = \text{Gain} \cdot V_{in} + V_{ref\_INA}$$

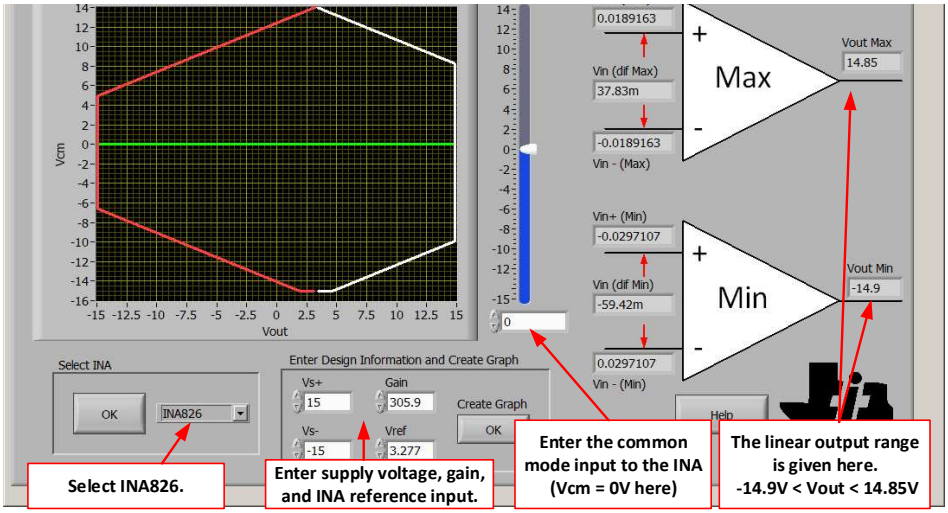
$$V_{ref\_INA} \quad V_{out} - \text{Gain} \cdot V_{in} = 4.8V - \left(1 + \frac{49.4k\Omega}{162\Omega}\right) \cdot (5mV) = 3.27V$$

3. Select standard value resistors to set the INA826 reference voltage (V_{ref} = 3.27V). *Use Analog Engineer's Calculator* ("Passive\Find Voltage Divider" section) to find standard values for the voltage divider.

$$V_{ref\_INA} \quad \frac{R_2}{R_1 + R_2} \cdot V_{in\_div} \quad \frac{21.5k\Omega}{11.3k\Omega + 21.5k\Omega} \cdot (5V) = 3.277V$$

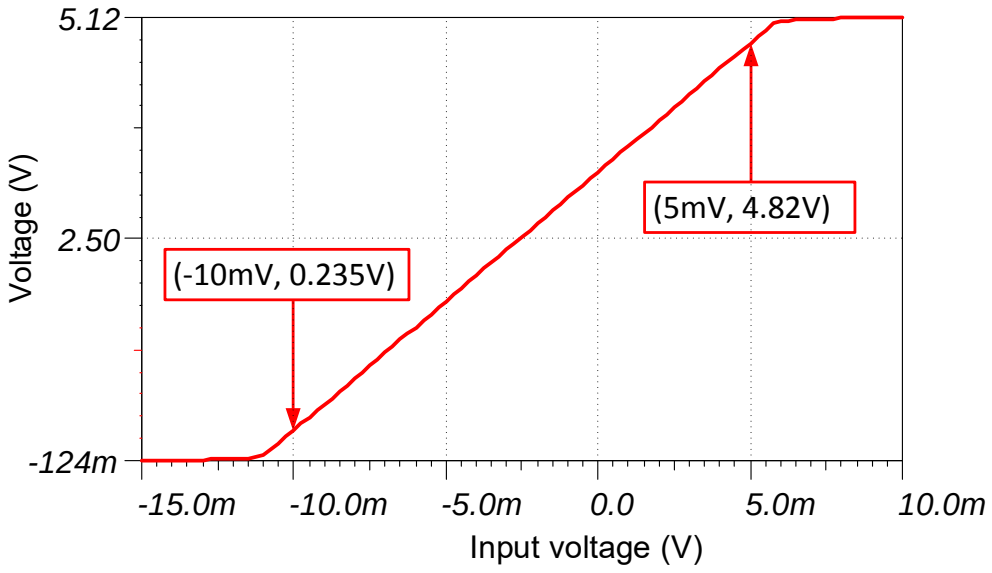


4. Use the *Common-Mode Input Range Calculator for Instrumentation Amplifiers* to determine if the INA826 is violating the common-mode range.



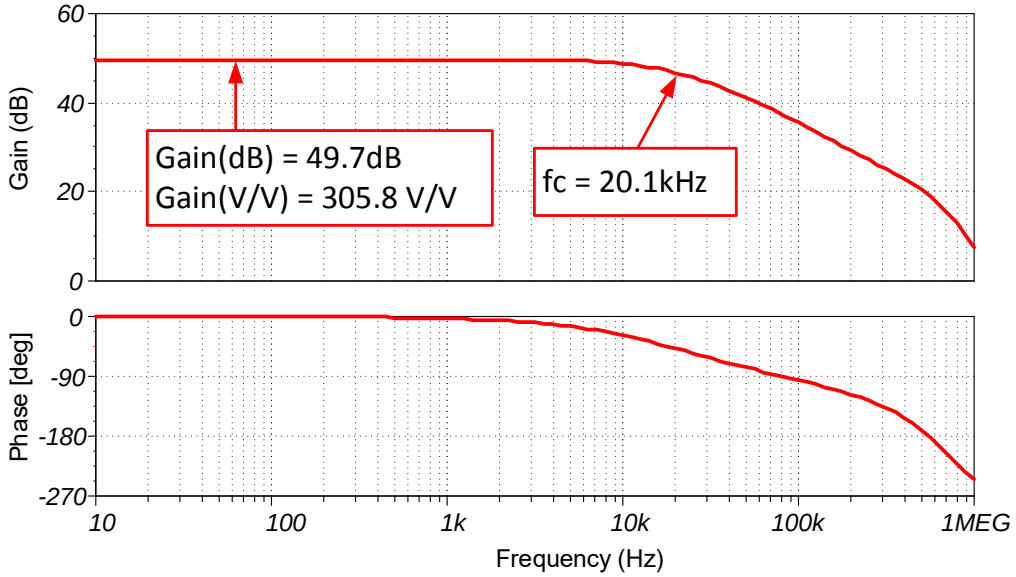
DC Transfer Characteristics

The following graph shows a linear output response for inputs from –5mV to +15mV. Refer to *Determining a SAR ADC's Linear Range when using Instrumentation Amplifiers* for detailed theory on this subject. Note that the output range is intentionally limited to –0.12V to 5.12V using Schottky diodes to protect the ADS8860. Note that Schottky diodes are used because the low forward voltage drop (typically less than 0.3V) keeps the output limit very near the ADC supply voltages. The absolute maximum rating for the ADS8860 is –0.3V < Vin < REF +0.3V.



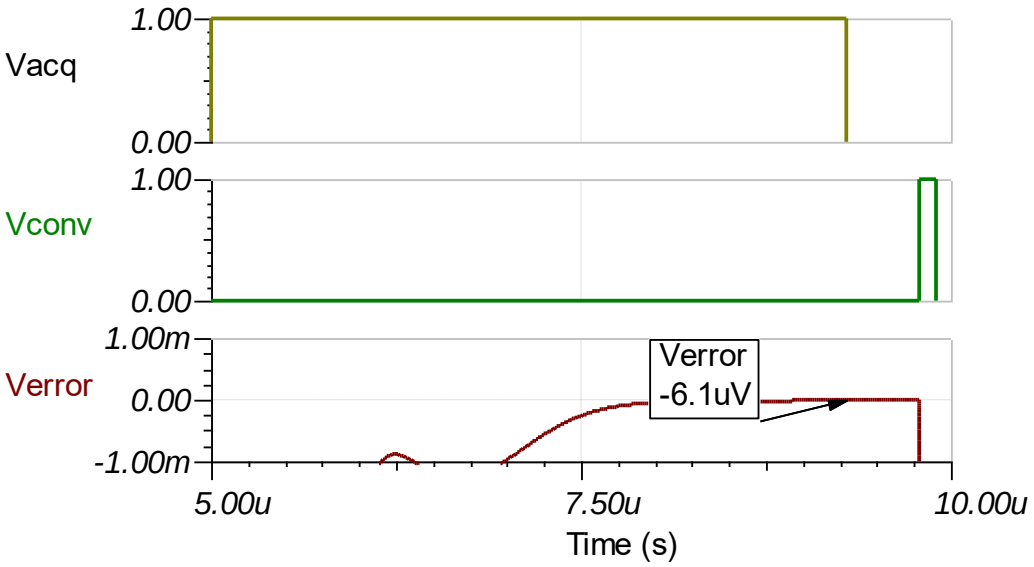
AC Transfer Characteristics

The bandwidth is simulated to be 20.1kHz, and the gain is 49.7dB which is a linear gain of 305.8. See the video series on *Op Amps: Bandwidth 1* for more details on this subject.



Transient ADC Input Settling Simulation

The following simulation shows settling to a +15mV dc input signal. This type of simulation shows that the sample and hold kickback circuit is properly selected. Refer to *Introduction to SAR ADC Front-End Component Selection* for detailed theory on this subject



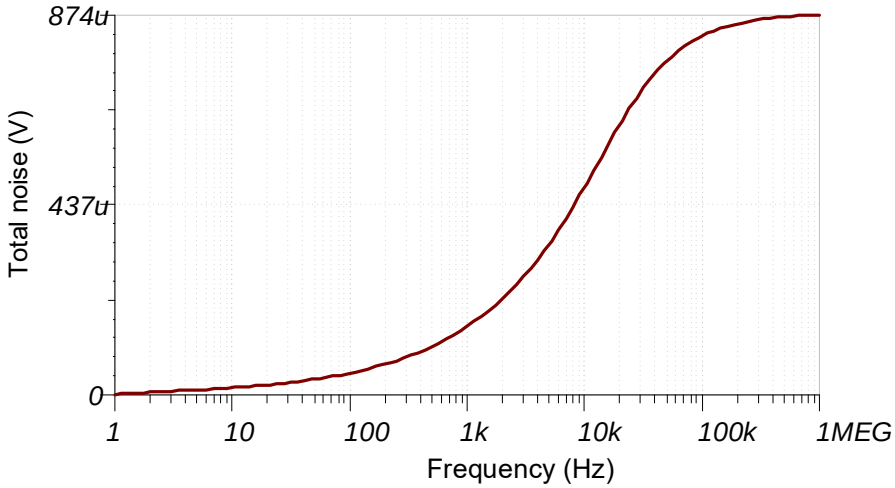
Noise Simulation

The following simplified noise calculation is provided for a rough estimate. We neglect noise from the OPA192 as the instrumentation amplifier is in high gain, so its noise is dominant.

$$E_n = \text{Gain} \cdot \sqrt{e_{NI}^2 + \left(\frac{e_{NO}}{\text{Gain}}\right)^2} \cdot \sqrt{K_n \cdot f_c}$$

$$E_n = (305.8) \cdot \sqrt{\left(18\text{nV}/\sqrt{\text{Hz}}\right)^2 + \left(\frac{110\text{nV}/\sqrt{\text{Hz}}}{305.8}\right)^2} \cdot \sqrt{1.57 \cdot (20.1\text{kHz})} = 978\mu\text{V}/\sqrt{\text{Hz}}$$

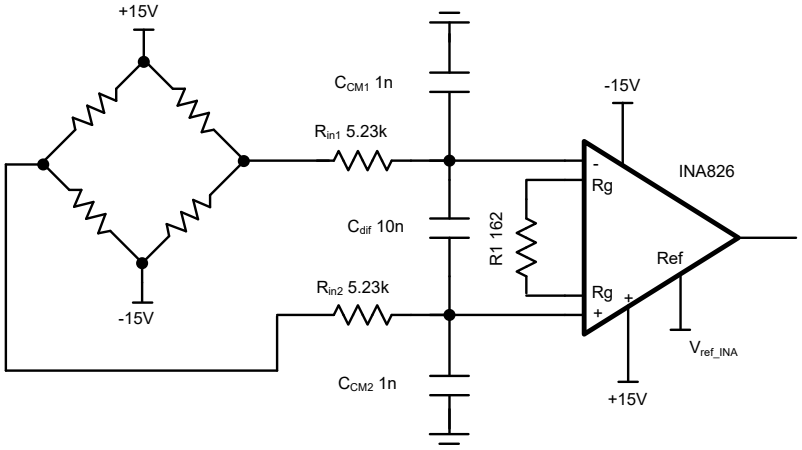
Note that calculated and simulated match well. Refer to *TI Precision Labs - Op Amps: Noise 4* for detailed theory on amplifier noise calculations, and *Calculating the Total Noise for ADC Systems* for data converter noise.



Optional Input Filter

The following figure shows a commonly used instrumentation amplifier input filter. The differential noise is filtered with C_{dif}, and the common-mode noise is filtered with C_{cm1} and C_{cm2}. Note that it is recommended that $C_{dif} \geq 10C_{cm}$. This prevents conversion of common-mode noise to differential noise due to component tolerances. The following filter was designed for a differential cutoff frequency of 15kHz.

$$\begin{aligned}
&\text{Let } C_{dif} = 1\text{nF and } f_{dif} = 15\text{kHz} \\
&R_{in} < \frac{1}{4 \cdot \pi \cdot f_{dif} \cdot C_{dif}} \quad \frac{1}{4 \cdot \pi \cdot (15\text{kHz}) \cdot (1\text{nF})} = 5.305\text{k}\Omega \text{ or } 5.23\text{k}\Omega \text{ for 1\% standard value} \\
&C_{cm} \quad \frac{1}{10} \cdot C_{dif} = 100\text{pF} \\
&f_{cm} \quad \frac{1}{2 \cdot \pi \cdot R_{in} \cdot C_{cm}} \quad \frac{1}{2 \cdot \pi \cdot (5.23\text{k}\Omega) \cdot (100\text{pF})} = 304\text{kHz} \\
&f_{dif} \quad \frac{1}{4 \cdot \pi \cdot R_{in} \cdot \left(C_{dif} + \frac{1}{2} C_{cm} \right)} \quad \frac{1}{4 \cdot \pi \cdot (5.23\text{k}\Omega) \cdot \left(1\text{nF} + \frac{1}{2} \cdot 100\text{pF} \right)} = 14.5\text{kHz}
\end{aligned} \tag{1}$$



Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS8860	16-bit resolution, SPI, 1Msps sample rate, single-ended input, Vref input range 2.5 V to 5.0 V.	http://www.ti.com/product/ADS8860	Link to similar devices
OPA192	Bandwidth 10MHz, Rail-to-Rail input and output, low noise 5.5nV/rtHz, low offset ±5μV, low offset drift ±0.2μV/ºC. (Typical values)	http://www.ti.com/product/OPA192	Link to similar devices
INA826	Bandwidth 1MHz (G = 1), low noise 18nV/rtHz, low offset ±40μV, low offset drift ±0.4μV/ºC, low gain drift 0.1ppm/ºC. (Typical values)	http://www.ti.com/product/INA826	Link to similar devices

Link to Key Files

Source files for this design - http://www.ti.com/lit/zip/sbac184

For direct support from TI Engineers use the E2E community:

http://e2e.ti.com/

TI Precision Labs Training Series community:

TI Precision Labs - https://training.ti.com/ti-precision-labs-overview

Circuit for Driving a Switched-Capacitor SAR ADC with a Buffered Instrumentation Amplifier

Art Kay

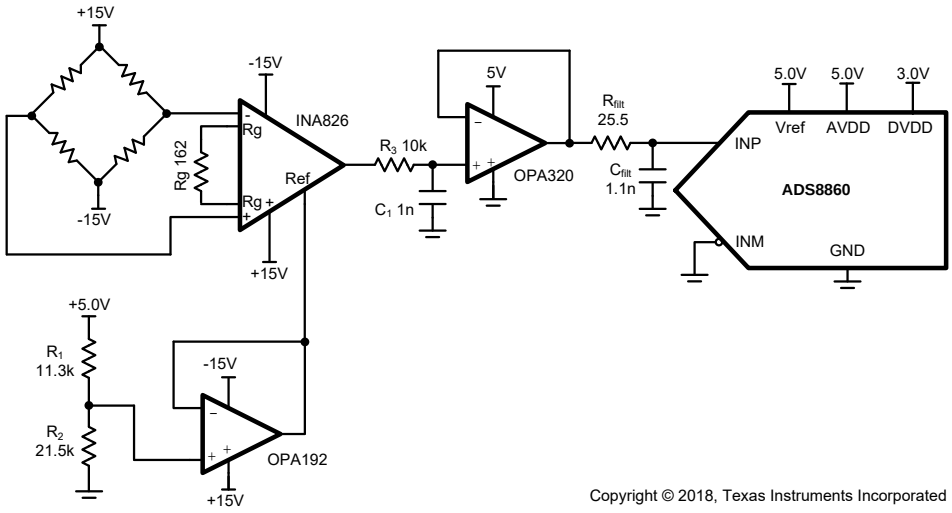
Input	ADC Input	Digital Output ADS8860
–10mV	Out = 0.2V	$0A3D_H$ or 2621_{10}
5mV	Out = 4.8V	$F5C3_H$ or 62915_{10}

Power Supplies					
AVDD	DVDD	V_{ref_INA}	V_{ref}	V_{cc}	V_{ee}
5.0V	3V	3.277V	5.0V	15V	–15V

Design Description

Instrumentation amplifiers are a common way of translating low-level sensor outputs to high-level signals to drive an ADC. Typically, instrumentation amplifiers are optimized for low noise, low offset, and low drift. Unfortunately, the bandwidth of many instrumentation amplifiers may not be sufficient to achieve good settling to ADC charge kickback at maximum sampling rates. This document shows how a wide-bandwidth buffer can be used with an instrumentation amplifier to achieve good settling at high sampling rates. Furthermore, many instrumentation amplifiers are optimized for high voltage supplies and it may be required to interface the high voltage output (that is, ±15V) to a lower voltage amplifier (for example, 5V). This design shows how a current-limiting resistor can protect the amplifier from electrical overstress in cases where the instrumentation amplifier is outside the input range of the op amp. A related cookbook circuit shows a simplified approach that does not include the wide-bandwidth buffer (*Driving a Switched-Capacitor SAR With an Instrumentation Amplifier*). The simplified approach has limited sampling rate as compared to the buffered design. Note that the following circuit shows a bridge sensor, but this method could be used for a wide range of different sensors.

This circuit implementation is applicable in applications such as *Analog Input Modules*, *Electrocardiogram (ECG)*, *Pulse Oximeters*, *Lab Instrumentation*, and *Control Units for Rail Transport*.



Specifications

Specification	Calculated	Simulated
Sampling rate	1Msps	1Msps, settling to –44µV
Offset (ADC Input)	40µV · 306.7 = 12.27mV	16mV
Offset Drift	(0.4µV/ºC) · 306.7 = 123µV/ºC	N/A
Noise	978µV	586μV_{RMS}

Design Notes

1. The bandwidth of instrumentation amplifiers is typically too low to drive SAR data converters at high data rates (the INA826 bandwidth is 10.4kHz for a gain of 305V/V in this example). Wide bandwidth is needed because the SAR has a switched capacitor input that needs to be charged during each conversion cycle. The OPA320 buffer was added to allow the ADC to run at full data rate (ADS8860 1Msps).
2. Select the gain to achieve an input swing that matches the input range of the ADC. Use the instrumentation amplifier reference pin to shift the signal offset to match the input range. This is covered in the *component selection* section.
3. The INA826 gain is scaled so that the op amp input voltage levels are inside the normal operating range of the amplifier. However, during power up or when a sensor is disconnected the output may drive to either power supply rail (±15V). The resistor R_3 is used to limit the current . This is covered in the *Overvoltage Protection Filter Between Instrumentation Amplifier and Op Amp* section of this document.
4. The buffer amplifier following the voltage divider is required for driving the reference input of most instrumentation amplifiers. Choose precision resistors and a precision low offset amplifier as the buffer. Refer to *Selecting the right op amp* for more details on this subject.
5. Check the common mode range of the amplifier using the *Common-Mode Input Range Calculator for Instrumentation Amplifiers* software tool.
6. Select COG capacitors for C_1, and C_{filt} to minimize distortion.
7. Use 0.1% 20ppm/°C film resistors or better for the gain set resistor R_g. The error and drift of this resistor will directly translate into gain error and gain drift.
8. The *TI Precision Labs – ADCs* training video series methods for selecting the charge bucket circuit R_{filt} and C_{filt}. Refer to *Introduction to SAR ADC Front-End Component Selection* for details on this subject.

Component Selection

1. Find the gain set resistor for the instrumentation amplifier to set the output swing to 0.2V to 4.8V.

$$Gain \quad \frac{V_{out\_max} - V_{out\_min}}{V_{in\_max} - V_{in\_min}} \quad \frac{4.9V - 0.2V}{5mV - (-10mV)} \quad 306.7$$

$$Gain \quad 1 + \frac{49.4k\Omega}{R_g}$$

$$R_g \quad \frac{49.4k\Omega}{Gain - 1.0} \quad \frac{49.4k\Omega}{(306.7) - 1.0} \quad 151.6\Omega \text{ or } 162\Omega \text{ for standard 0.1\% resistor}$$

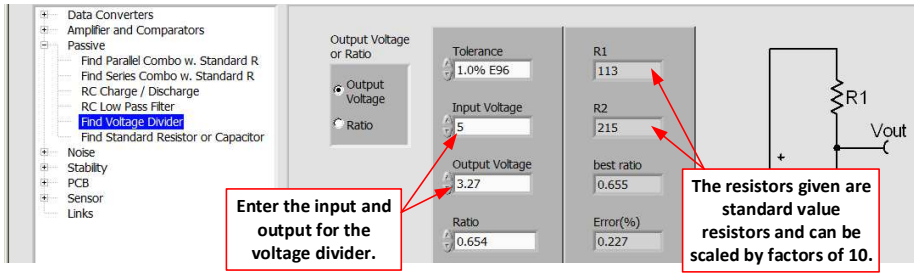
2. Find the INA826 reference voltage (Vref) to shift the output swing to the proper voltage level

$$V_{out} \quad Gain \cdot V_{in} + V_{ref\_INA}$$

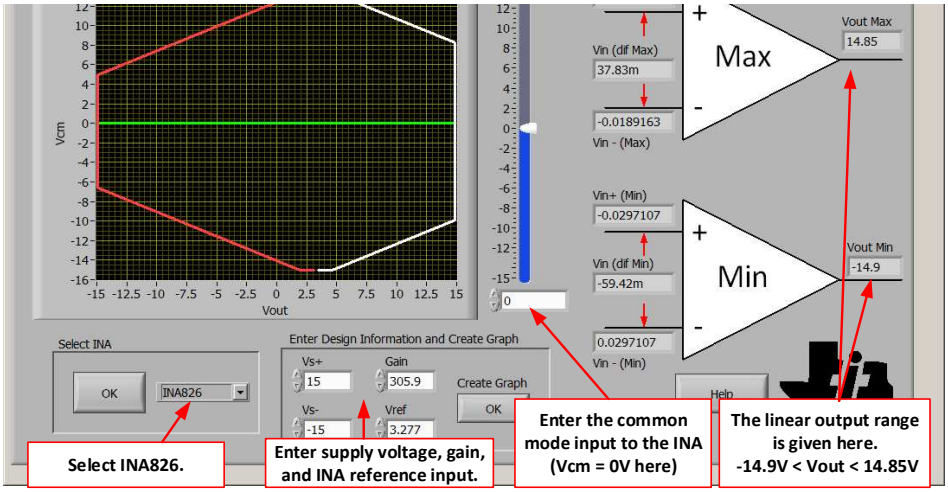
$$V_{ref\_INA} = V_{out} - Gain \cdot V_{in} \quad 4.8V - \left(1 + \frac{49.4k\Omega}{162\Omega}\right) \cdot (5mV) \quad 3.27V$$

3. Select standard value resistors to set the INA826 reference voltage (V_{ref_INA} = 3.27V). Use the *Analog Engineer's Calculator* ("Passive\Find Voltage Divider" section) to find standard values for the voltage divider.

$$V_{ref\_INA} \quad \frac{R_2}{R_1 + R_2} \cdot V_{in\_div} \quad \frac{21.5k\Omega}{11.3k\Omega + 21.5k\Omega} \cdot (5V) \quad 3.277V$$

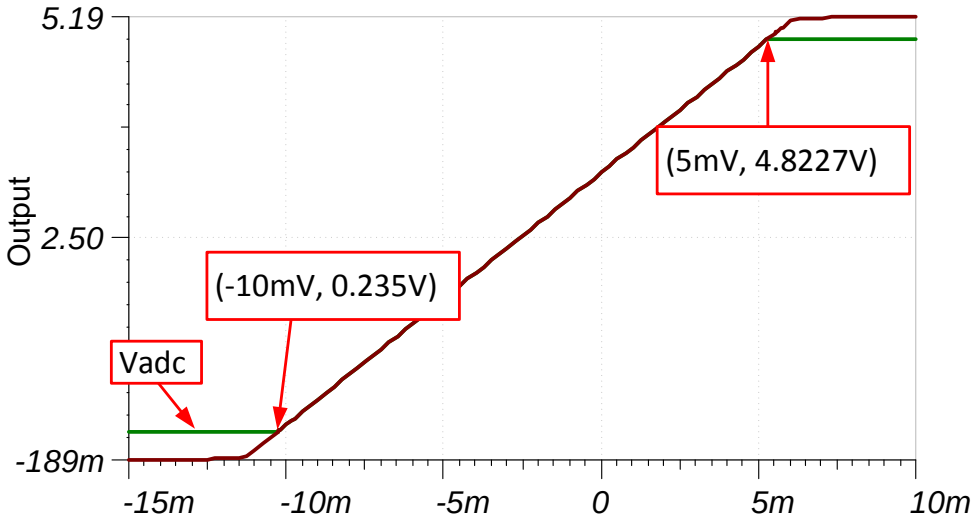


4. Use the *Common-Mode Input Range Calculator for Instrumentation Amplifiers* to determine if the INA826 is violating the common mode range.



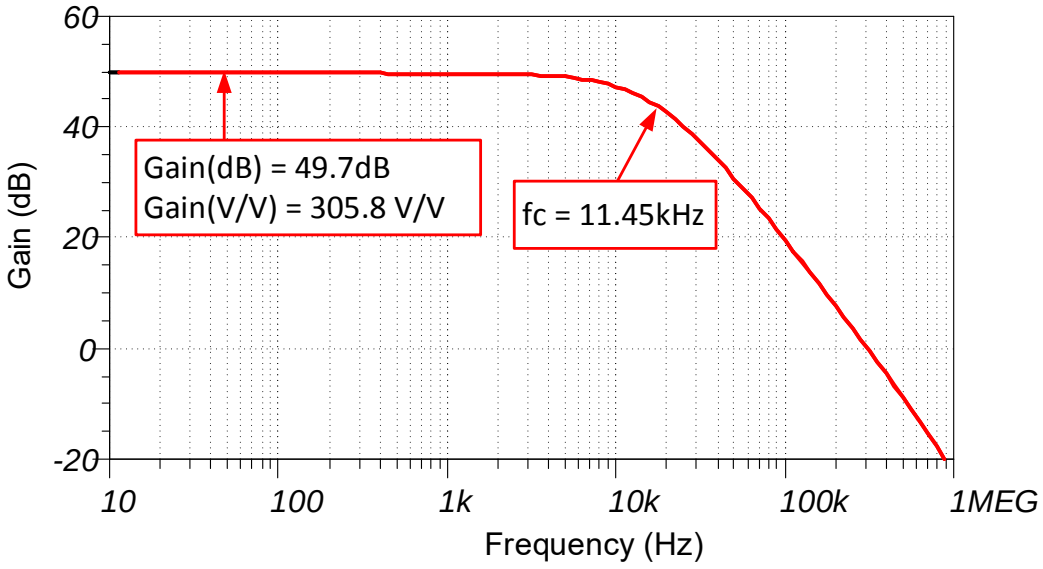
DC Transfer Characteristics

The following graph shows a linear output response for inputs from –5mV to +15mV. Refer to *Determining a SAR ADC's Linear Range when using Instrumentation Amplifiers* for detailed theory on this subject. In cases where the INA826 output exceeds the op amp input range, the ESD diodes turn on and limit the input. The resistor R3 protects the amplifier from damage by limiting the input current (see the *Overvoltage Protection Filter Between Instrumentation Amplifier and Op Amp* section). The op amp output is inside the absolute maximum rating of the ADS8860 (–0.3V < V_{IN} < REF +0.3V).



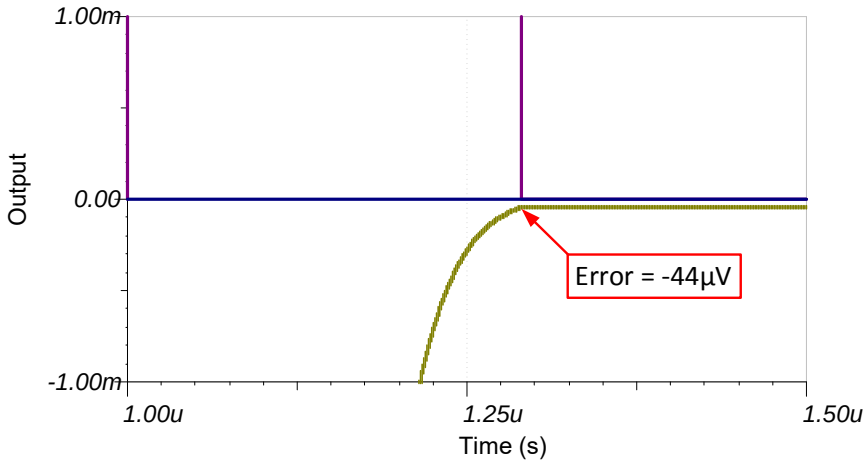
AC Transfer Characteristics

The bandwidth is simulated to be 11.45 kHz in this configuration. In this bandwidth it is not possible to drive the SAR converter at full speed. See the *TI Precision Labs* video series *Op Amps: Bandwidth 1* for more details on this subject.



Transient ADC Input Settling Simulation

The OPA320 buffer (20MHz) is used because it is capable of responding to the rapid transients from the ADC8860 charge kickback. This type of simulation shows that the sample and hold kickback circuit is properly selected. Refer to *Introduction to SAR ADC Front-End Component Selection* for detailed theory on this subject.



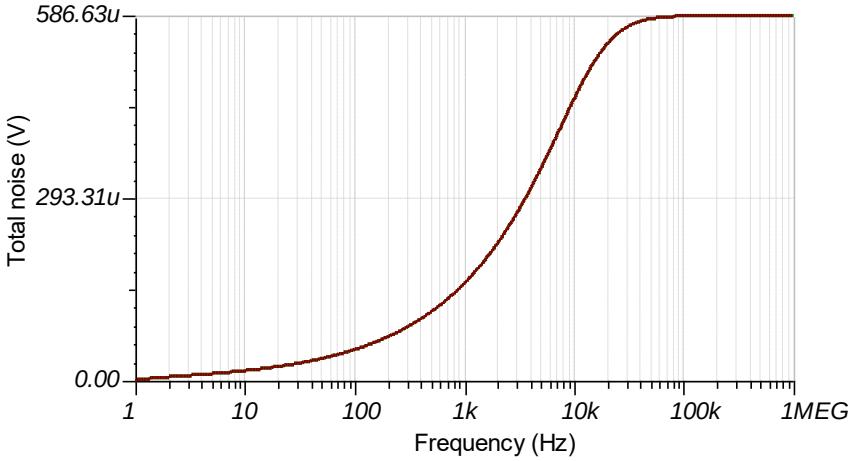
Noise Simulation

Use a simplified noise calculation for a rough estimate. We neglect the noise from the OPA192 as the instrumentation amplifier is in high gain so its noise is dominant.

$$E_n = Gain \cdot \sqrt{e_{NI}^{\ 2} + \left(\frac{e_{NO}}{Gain}\right)^2} \cdot \sqrt{K_n \cdot f_c}$$

$$E_n \quad (305.8) \cdot \sqrt{\left(18nV/\sqrt{Hz}\right)^2 + \left(\frac{110nV/\sqrt{Hz}}{305.8}\right)^2} \cdot \sqrt{1.57 \cdot (11.45kHz)} \quad 738\mu V/\sqrt{Hz}$$

Note that the calculated and simulated match well. Refer to *TI Precision Labs - Op Amps: Noise 4* for detailed theory on amplifier noise calculations, and *Calculating the Total Noise for ADC Systems* for data converter noise.

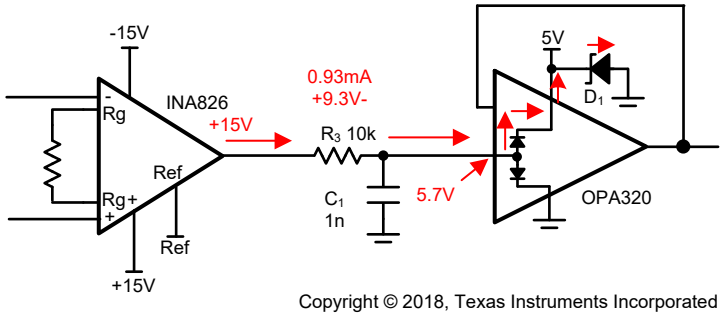


Overvoltage Protection Filter Between Instrumentation Amplifier and Op Amp

The filter between the INA826 and OPA320 serves two purposes. It protects the OPA320 from overvoltage, and acts as a noise or anti-aliasing filter. The INA826 gain should be scaled so that under normal circumstances, the output is inside the range of the OPA320 (that is, 0V to 5V). Thus, normally the overvoltage signals applied to the input of the OPA320 is not seen. However, during power up or in cases where the sensor is disconnected, the INA826 output may be at either power supply rail (that is, ±15V). In overvoltage cases, the resistor (R3) will limit current into the OPA320 for protection. The internal ESD diodes on the OPA320 will turn on during overvoltage events and direct the overvoltage signal to the positive or negative supply. In the following example, the overvoltage signal is directed to the positive supply and the transient voltage suppressor (D_1, SMAJ5.0A) turns on to sink the current. Note that the resistor is scaled to limit the current to the OPA320 absolute maximum input current (10mA). See *TI Precision Labs - Op Amps: Electrical Overstress (EOS)* for detailed theory on this subject.

$$R_3 > \frac{V_{INA} - V_{OpaSupply} - 0.7V}{I_{ABS\_MAX\_OPA}} \quad \frac{15V - 5.0V - 0.7V}{10mA} \quad 9.3k\Omega \text{ choose } 10k\Omega \text{ for margin.}$$

$$C_1 \quad \frac{1}{2 \cdot \pi \cdot R_3 \cdot f_c} \quad \frac{1}{2 \cdot \pi \cdot (10k\Omega) \cdot (15kHz)} \quad 1.06nF \text{ or 1nF standard value}$$



Optional Input Filter

The following figure shows a commonly used instrumentation amplifier input filter. The differential noise is filtered with C_{dif}, and the common mode noise is filtered with C_{cm1} and C_{cm2}. Note that it is recommended that $C_{dif} \geq 10C_{cm}$. This prevents conversion of common mode noise to differential noise due to component tolerances. The following filter was designed for a differential cutoff frequency of 15kHz.

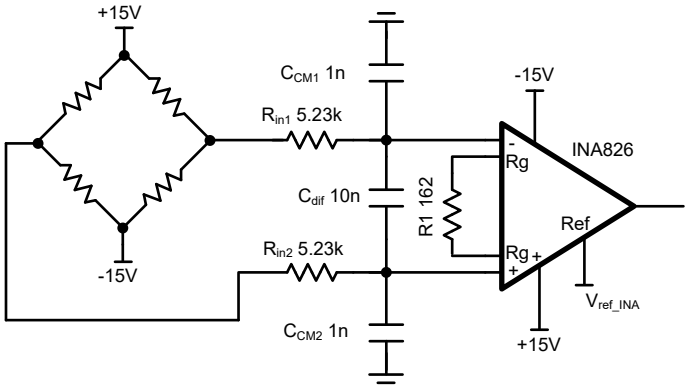
Let $C_{dif} = 1nF$ and $f_{dif} = 15kHz$

$$R_{in} < \frac{1}{4 \cdot \pi \cdot f_{dif} \cdot C_{dif}} \quad \frac{1}{4 \cdot \pi \cdot (15kHz) \cdot (1nF)} \quad 5.305k\Omega \text{ or } 5.23k\Omega \text{ for 1\% standard value}$$

$$C_{cm} \quad \frac{1}{10} \cdot C_{dif} = 100pF$$

$$f_{cm} \quad \frac{1}{2 \cdot \pi \cdot R_{in} \cdot C_{cm}} \quad \frac{1}{2 \cdot \pi \cdot (5.23k\Omega) \cdot (100pF)} \quad 304kHz$$

$$f_{dif} \quad \frac{1}{4 \cdot \pi \cdot R_{in} \cdot \left(C_{dif} + \frac{1}{2} C_{cm} \right)} \quad \frac{1}{4 \cdot \pi \cdot (5.23k\Omega) \cdot \left(1nF + \frac{1}{2} \cdot 100pF \right)} = 14.5kHz$$



Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS8860	16-bit resolution, SPI, 1-Msps sample rate, single-ended input, Vref input range 2.5V to 5.0V.	http://www.ti.com/product/ADS8860	Links to similar devices
OPA192	8-kHz bandwidth, Rail-to-Rail output, 450-nA supply current, unity gain stable	http://www.ti.com/product/OPA192	Links to similar devices
INA826	Bandwidth 1MHz (G=1), low noise 18nV/rtHz, low offset ±40µV, low offset drift ±0.4µV/ºC, low gain drift 0.1ppm/ºC. (typical values)	http://www.ti.com/product/INA826	Links to similar devices

Link to Key Files

Source Files for this circuit - http://www.ti.com/lit/zip/SBAC184

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e2e.ti.com

Reducing Effects of External RC Filter Circuit on Gain and Drift Error for Integrated Analog Front Ends (AFEs): ±10 V, up to 200 kHz, 16 Bit

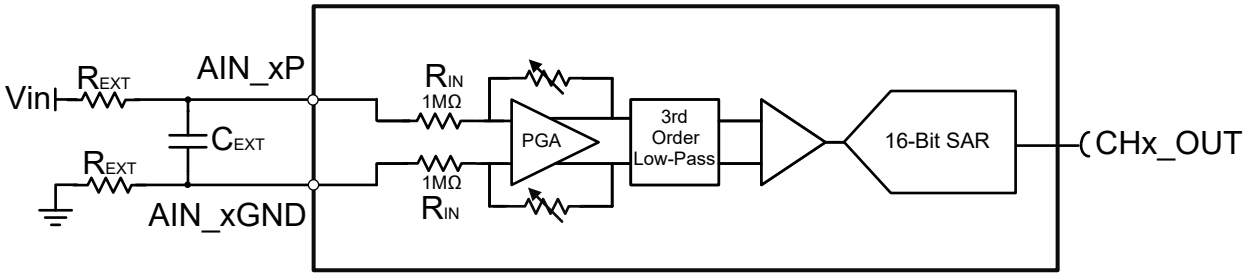
Cynthia Sosa

Input	ADC Input	Digital Output
VinMin = –10V	AIN-xP = –10V	-32768_{10}
	AIN-xGND = 0V	8000_{H}
VinMax = 10V	AIN-xP = 10V	32767_{10}
	AIN-xGND = 0V	$7FFF_{H}$

Power Supplies	
AVDD	DVDD
5V	5V

Design Description

This cookbook design describes how to select filter component values and how to minimize the gain error and drift introduced by this filter on a fully-integrated analog front end (AFE) SAR ADC. The design uses the input impedance drift at the full scale range of ±10V of the ADS8588S. This external RC filter minimizes external noise and provides protection from electrical overstress. Minimizing gain error and drift are important to end equipment such as: *Multi-Function Relays*, *AC Analog Input Modules*, and *Terminal Units*. This design describes two correction methods, a no-calibration correction factor and a 2-point calibration. Implementing calibration can minimize both the gain error introduced by the external resistor and the internal device gain error to negligible levels.



Specifications

Specification	Calculated	Measured
Introduced Gain Error (25°C)	0.9901%	0.9894%
Introduced Gain Error (125°C)	0.995%	–1.1388%
Introduced Gain Error Drift	0.49ppm/°C	–0.8031ppm/°C

Design Notes

1. Use low drift R_{EXT} resistors to maintain low drift and minimize gain error. This design uses resistors with a temperature coefficient of 25ppm/°C and ±0.1% tolerance.
2. The internal programmable gain amplifier (PGA) presents a constant resistive impedance of 1MΩ
3. The R_{EXT} value introduced is directly proportional to its introduced error
4. Calibration can also be used to eliminate system offset gain error
5. The *TI Precision Labs – ADCs* training video series covers methods for calculating gain and offset error and eliminating these errors through calibration, see *Understanding and Calibrating the Offset and Gain for ADC Systems*. *Using SPICE Monte Carlo Tool for Statistical Error Analysis* explains how to use *Monte Carlo Analysis* for statistical error analysis.

Component Selection

External anti-aliasing RC filters reduce noise and protect from electrical overstress; if a large resistor value is used, this will further limit the input current. A large external resistive value will also provide a low cutoff frequency, which is desired for relay protection applications as the input frequencies are usually 50 or 60 Hz. Furthermore, a balanced RC filter configuration is required for better common-mode noise rejection; matching external resistors are present on both the negative and positive input paths. To minimize the introduced drift error, the external resistors should be low drift; 25ppm/°C resistors.

1. Choose a high-value R_{EXT} based on the desired cutoff frequency. A cutoff frequency of 320Hz was used to eliminate harmonics from a 50- or 60-Hz input signal.

   R_{EXT} = 10kΩ
2. Choose C_{EXT}

$$C_{EXT} \quad \frac{1}{2 \cdot \pi \cdot f_C \cdot 2 \cdot R_{EXT}} \quad \frac{1}{2 \cdot \pi \cdot 320\ \text{Hz} \cdot 2 \cdot 10\ \text{k}\Omega} \quad 24.8\ \text{nF}$$

   Nearest standard capacitor value available, C_{EXT} = 24nF

Calculate Gain Error Drift

This section demonstrates how to calculate the introduced gain error drift. The additional drift from the external filter resistor is small compared to the internal device drift.

R_{IN} = 1MΩ, R_{EXT} = 10kΩ, C_{EXT} = 24nF

1. Calculate effective internal impedance due to maximum negative drift (–25ppm/°C)

$$R_{IN(-25\,\text{ppm}/^\circ\text{C})} \quad R_{IN} \cdot [\text{Drift (ppm}/^\circ\text{C}) \cdot \delta T(^\circ\text{C}) + 1]$$

$$R_{IN(-25\,\text{ppm}/^\circ\text{C})} \quad 1\text{M}\Omega \cdot [-25\ \text{ppm}/^\circ\text{C} \cdot (125^\circ\text{C} - 25^\circ\text{C}) + 1]$$

$$R_{IN(-25\,\text{ppm}/^\circ\text{C})} \quad 0.9975\ \text{M}\Omega$$

2. Calculate effective external resistance due to maximum positive drift (25ppm/°C)

$$R_{EXT\ (+25\,\text{ppm}/^\circ\text{C})} = R_{EXT} \cdot [\text{Drift (ppm}/^\circ\text{C}) \cdot \delta T(^\circ\text{C}) + 1]$$

$$R_{EXT\ (+25\,\text{ppm}/^\circ\text{C})} \quad 10\,\text{k}\Omega \cdot [25\ \text{ppm}/^\circ\text{C} \cdot (125^\circ\text{C} - 25^\circ\text{C}) + 1]$$

$$R_{EXT\ (+25\,\text{ppm}/^\circ\text{C})} \quad 10.025\ \text{k}\Omega$$

3. Calculate nominal gain error introduced by the external resistor at room temperature

$$\text{GainError}\,(R_{EXT})_{RoomTemp} \quad \frac{1}{1+\frac{R_{IN}}{R_{EXT}}}$$

$$\text{GainError}\,(R_{EXT})_{RoomTemp} \quad \frac{1}{1+\frac{1\text{M}\Omega}{10\,\text{k}\Omega}}$$

$$\text{GainError}\,(R_{EXT})_{RoomTemp} \quad 0.009901 \text{ or } 0.9901\,\%$$

4. Calculate nominal gain error introduced by the external resistor at highest rated temperature

$$\text{GainError}\,(R_{EXT})_{125°C} \quad \frac{1}{1+\frac{0.9975\,\text{M}\Omega}{10.025\,\text{k}\Omega}}$$

$$\text{GainError}\,(R_{EXT})_{125°C} \quad 0.009950 \text{ or } 0.995\,\%$$

5. Calculate gain error drift introduced by the external resistor

$$\text{GainError\_Drift}(R_{EXT}) \quad \frac{\text{GainError}(R_{EXT})_{RoomTemp} - \text{GainError}(R_{EXT})_{125°C}}{\delta T} \cdot 10^6$$

$$\text{GainError\_Drift}(R_{EXT}) \quad \frac{0.009901 - 0.00950}{(125°\text{C} - 25°\text{C})} \cdot 10^6$$

$$\text{GainError\_Drift}(R_{EXT}) = -0.49\text{ppm}/°\text{C}$$

The maximum gain error temperature drift of the ADS8588S is ±14ppm/°C, which is orders of magnitude larger than the calculated drift error introduced, making the introduced error negligible. The minimal drift error introduced by the external resistors has greatly to do with the low drift coefficient of the input impedance (±25ppm/ºC).

To measure the introduced gain error drift, two test signals are sampled and applied at 0.5V from the full scale input range within the linear range of the ADC. The signals are applied and sampled with and without the external RC filter present. These measurements are performed at both temperatures, 25°C and 125°C. The percent gain errors are solved for by finding the percent error of the ideal slope and the measured slope for each of the four distinctive test conditions, resulting in four distinct percent gain error measurements. The drift (ppm/°C) with and without the RC present is then calculated by converting the percent gain errors to decimal format then following step 5 shown above. The introduced gain error drift is then solved for by subtracting the drift of the RC and no RC present.

Uncalibrated Correction

An uncalibrated correction targets to solve the input voltage before any losses occur due to the RC filter by working backwards from the ADC measured samples using a voltage divider.

1. Apply known test signal and measure equivalent code

V_{in}	Measured Code	Equivalent Measured Input
9.5V	30841	9.412

2. Calculate the input voltage before RC losses

$$V_{IN\_NoLoss} \quad V_{IN\_Equivalent} \cdot \frac{R_{EXT} + R_{IN}}{R_{IN}}$$

$$V_{IN\_NoLoss} \quad 9.412 \cdot \frac{1M\Omega + 10k\Omega}{1M\Omega}$$

$$V_{IN\_NoLoss} \quad 9.50612V$$

Uncalibrated Correction Measurements

Using a voltage correction can be beneficial, but not the most comprehensive. The correction factor can have a worst-case error of 0.2456% at room temperature due to change in internal impedance.

Room Temperature (25°C) Measurements				
V_{in}	Code	Reading	Correction	Error %
9.5	30841	9.412	9.506120	0.0644
8.5	27594	8.421	8.505210	0.0613
5	16232	4.954	5.003540	0.0708
0	1	0	0.000000	–
–5	–16230	–4.953	–5.002530	0.0506
–8.5	–27593	–8.421	–8.505210	0.0613
–9.5	–30839	–9.411	–9.505110	0.0538

2-Point Calibration Method

A two point calibration applies and samples two test signals at 0.5V from the full scale input range within the linear range of the ADC. These sample measurements are then used to calculate the slope and offset of the linear transfer function. Calibration will eliminate both the gain error introduced by the external resistor and the internal device gain error.

1. Apply test signal at 2.5% of input linear range

Vmin	Measured Code
–9.5V	–30839

2. Apply test signal at 97.5% of input linear range

Vmax	Measured Code
9.5V	30841

3. Calculate slope and offset calibration coefficients

$$m \quad \frac{Code_{max} - Code_{min}}{V_{max} - V_{min}}$$

$$m \quad \frac{30841 - (-30839)}{9.5 - (-9.5)} \quad 3246.3158$$

$$b = Code_{min} - m \cdot V_{min}$$

$$b = (-30839) - 3246.3 \cdot (-9.5\,V) = 1.0001$$

4. Apply calibration coefficient to all subsequent measurements

$$Vin_{Calibrate} \quad \frac{Code - b}{m}$$

$$Vin_{Calibrate} \quad \frac{30841 - 1.0001}{3246.3158} \quad 9.5000$$

2-Point Calibration Method Measurements

Calibration Coefficients

m = 3246.3158; *b* = 1.0001

At room temperature without calibration, a gain error is present. Once calibration is applied to the measured results from the ADC, the gain error is minimized to nearly zero.

Room Temperature (25°C) Measurements					
V_{IN}	Code	Uncalibrated V_{IN}	Calibrated V_{IN}	Voltage Error Without Calibration %	Voltage Error With Calibration %
9.5	30841	9.412	9.500000	–0.926316	–0.000001
8.5	27594	8.421	8.499789	–0.929412	–0.002480
5	16232	16232	4.999822	–0.920000	–0.003568
0	1	0	0.000000	–	–
–5	–16230	–4.953	–4.999822	–0.0940000	–0.003567
–8.5	–27593	–8.421	–8.500097	–0.929412	0.001144
–9.5	–30839	–9.411	–9.500000	–0.936842	0.000000

When exposed to high temperatures, the gain error increases, as expected. Once calibration is applied, the voltage error is decreased but not eliminated; the error still present is the drift error.

High Temperature (125°C) Measurements					
V_{IN}	Code	Uncalibrated V_{IN}	Calibrated V_{IN}	Relative Voltage Error Without Calibration %	Relative Voltage Error With Calibration %
9.5	30826	9.407	9.495379	–0.978947	–0.048639
8.5	27582	8.417	8.496093	–0.976471	–0.045968
5	16224	4.951	4.997357	–0.980000	–0.052854
0	0	0	–0.000308	0	–
–5	–16224	–4.951	–4.997973	–0.980000	–0.040531
–8.5	–27581	–8.417	–8.496401	–0.976471	–0.042344
–9.5	–30826	–9.407	–9.495995	–0.978947	–0.042153

Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS8588S	16-Bit, High-Speed 8-Channel Simultaneous-Sampling ADC With Bipolar Inputs on a Single Supply	SBAS642	Similar Devices

For direct support from TI Engineers use the E2E community:

http://e2e.ti.com/

Other Links

www.ti.com/adcs

Antialiasing Filter Circuit Design for Single-Ended ADC Input Using Fixed Cutoff Frequency

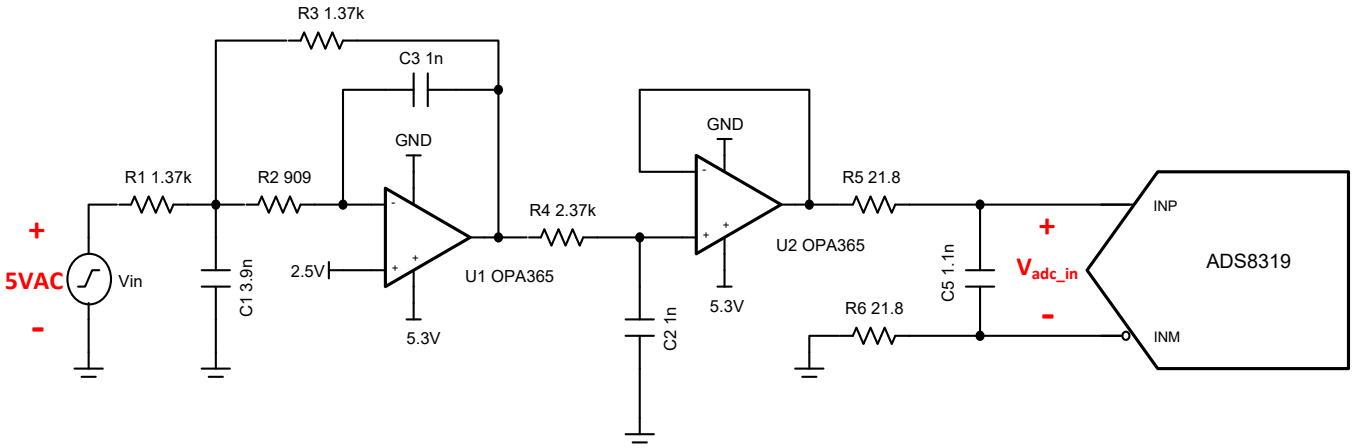
Manuel Chavez

Input	ADC Input	Digital Output ADS8319
V_{in} Min = 0.1V	V_{adc_in} = 4.9V	$FAE1_H$ or 64225_{10}
V_{in}Max = V_{REF} = 4.9V	V_{adc_in} = 0.1V	$051F_H$ or 1311_{10}

Power Supplies					
V_{cc}	V_{ee}	V_{cm}	V_{REF}	AVDD	DVDD
5.3V	GND (0V)	2.5V	5V	5V	5V

Design Description

This cookbook is intended to demonstrate a method of designing an antialiasing filter for a single-ended SAR ADC input using the Antialias Filter Designer on TI's *Analog Engineer's Calculator*. The objective of the tool is to find filter specifications that will attenuate alias signals to one-half LSB of a given ADC. This design approach uses a fixed cutoff frequency and the example circuit uses the ADS8319 ADC. This single-ended device circuit is practical for low-power applications such as *Data Acquisition*, *Lab Instrumentation*, *Oscilloscopes*, *Analog Input Module*, and battery-powered equipment.



Specifications

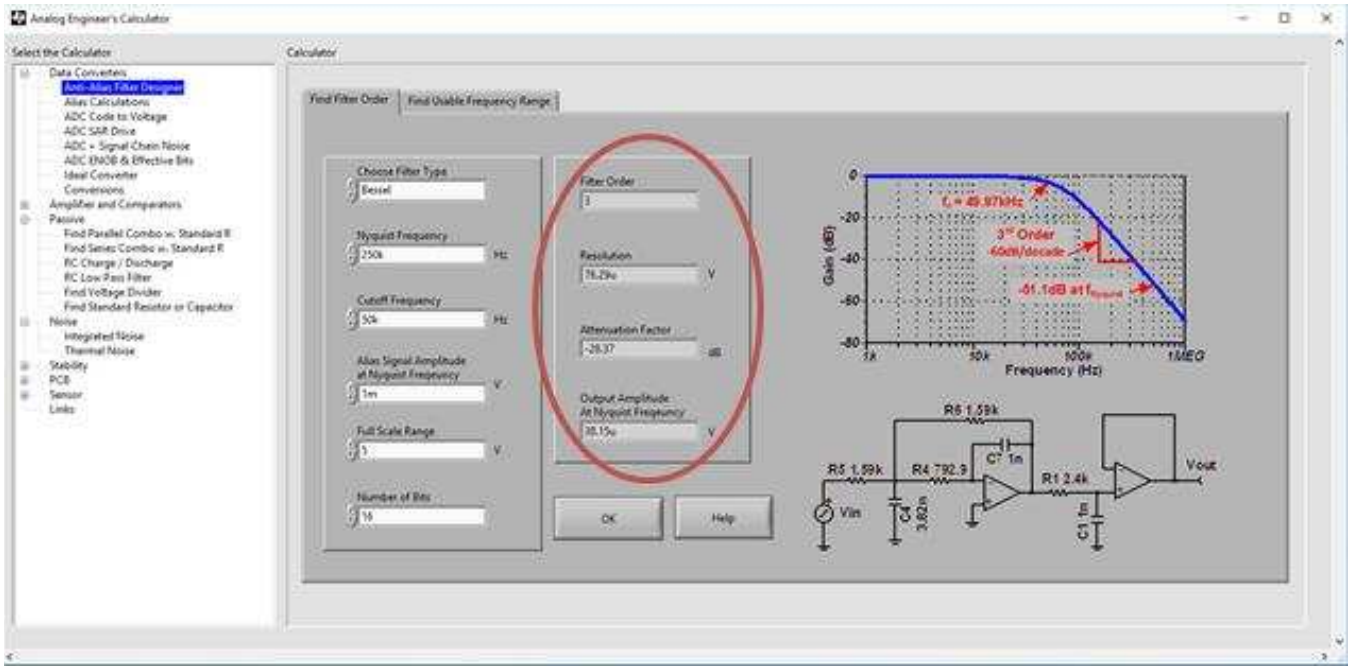
Specification	Calculated / Goal	Simulated
Attenuate 1mV alias signal at Nyquist to ½ LSB $V_{in\_Nyquist}$ = 1mV at 250kHz	$V_{out\_Nyquist}$ <= ½ LSB ½ LSB = 38.14µV at 250kHz	$V_{out\_Nyquist}$ = 21µV Attenuation = –33.43dB
Transient ADC Input Settling	< 0.5 LSB or 38.15µV	91.5nV
Noise	78.9µV	87.77µV
Bandwidth	50kHz	50.1kHz

Design Notes

1. *TI Precision Labs* introduces the concept of frequency domain aliasing and describes how aliases are error sources to avoid or minimize. The video on *Aliasing and Anti-aliasing Filters* covers how an antialiasing filter can be used to minimize these aliasing errors.
2. The active filter in this cookbook is designed using TI's *Analog Engineer's Calculator* and *TI FilterPro* (click to download). This software can be used to design active filter circuits for many applications.
3. Use 0.1%–1% tolerance resistors and 5% tolerance capacitors or better for good system accuracy.
4. RC charge bucket circuits are specially designed for each system; TI's Precision Labs video on *Refining Rfilt and Cfilt Values* explains how to optimize the RC charge bucket.
5. Circuit simulations are modeled with schematics and diagrams made using *TINA-TI* simulation software (click to download).
6. For detail on choosing the right driver op amp, building and simulating the ADC model, and finding the RC charge bucket values, see the TI Precision Labs video series *Introduction to SAR ADC Front-End Component Selection*.

Component Selection

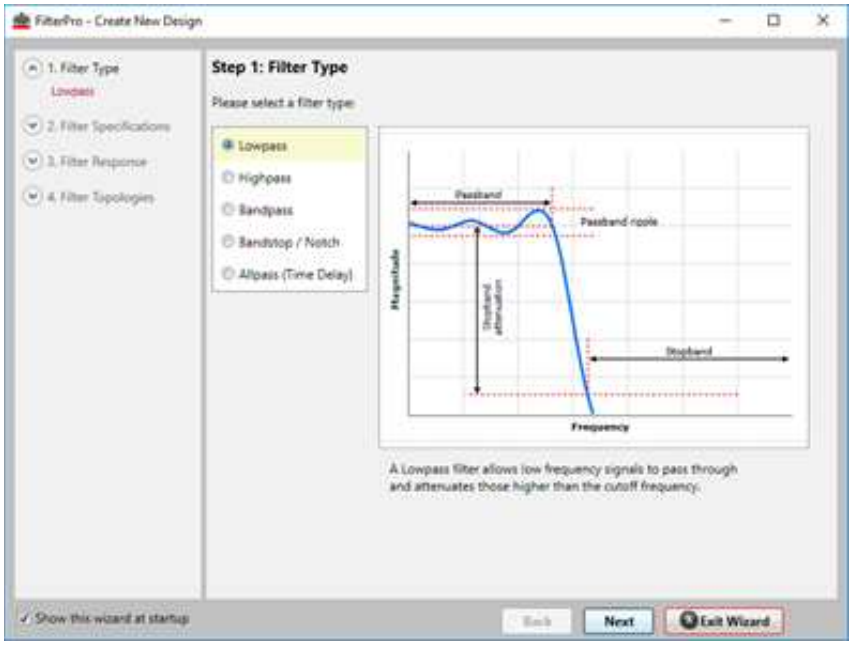
1. Once a single-ended ADC has been chosen, determine whether the antialias filter will be designed with a set cutoff frequency or set filter order. If the frequency is set, continue through the following steps. If the filter order is set, use the "Find Usable Frequency Range" tab in the Analog Engineer's Calculator. Both methods use tools from the *Analog Engineer's Calculator*.
2. Using the *Find Filter Order* tab of the *Anti-Alias Filter Designer*, choose between a Bessel and Butterworth filter under *Choose Filter Type*. Bessel is chosen in this case for maximum flatness in the pass band and linear phase response.
3. Fill in the *Nyquist Frequency* to be ½ of the sampling rate of the ADC. The ADS8319 has a sampling rate of 500ksps so the Nyquist frequency is 250kHz.
4. Determine the desired cutoff frequency of the filter to be designed and enter it in the *Cutoff Frequency* box; a general guideline is for the cutoff frequency to be one decade above the desired input frequency. In this case, the input frequency is 5kHz so the cutoff frequency is set to 50kHz.
5. For the *Alias Signal Amplitude at Nyquist Frequency* field, enter the largest expected alias signal amplitude that will be attenuated to ½ LSB at the Nyquist frequency. This number can range from microvolts up to the full scale voltage. In this low-noise system, a maximum alias signal amplitude of 1mVpp is expected.
6. The *Full Scale Range* of the ADC is typically equal to Vref and is set to 5V in this system. The bit resolution of the ADS8319 is 16 bits and is filled into *Number of Bits*.
7. After clicking *OK*, the results displayed on the right side of the calculator are used to design the necessary antialias filter.



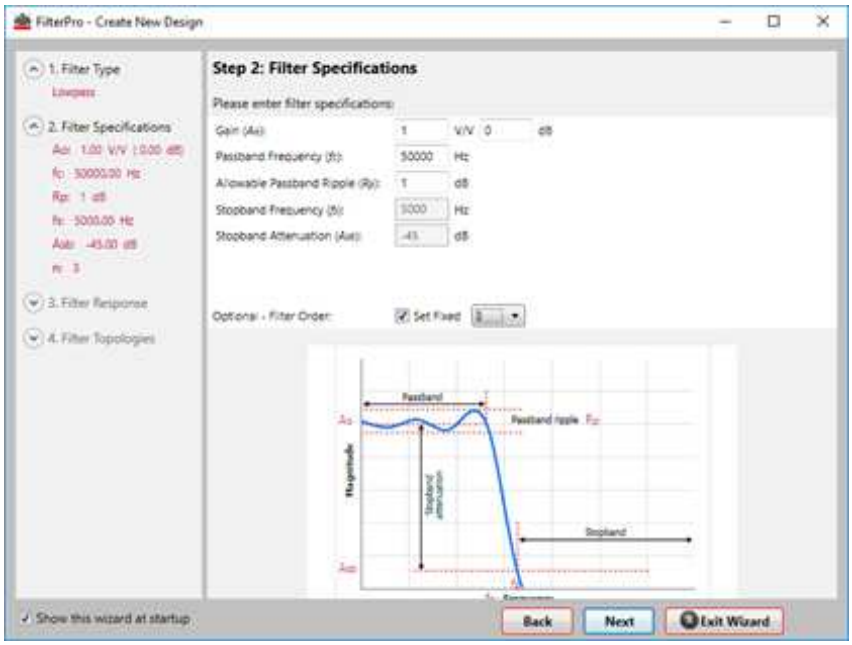
With the resulting filter specifications, the lowpass antialias filter can be designed by transcribing these numbers into TI FilterPro. The circuit specifications in this cookbook are $f_{nyquist}$ = 250k, f_c = 50k, V_{alias} = 1mV, FSR = 5V, and N bits = 16, so the Bessel example from Design Approach 1 is used continuing.

On startup, TI FilterPro asks for the filter specifications to design around. After the final screen, an active filter circuit is displayed, and this is the antialias filter of the system. Refer to the following screenshots for the steps using FilterPro.

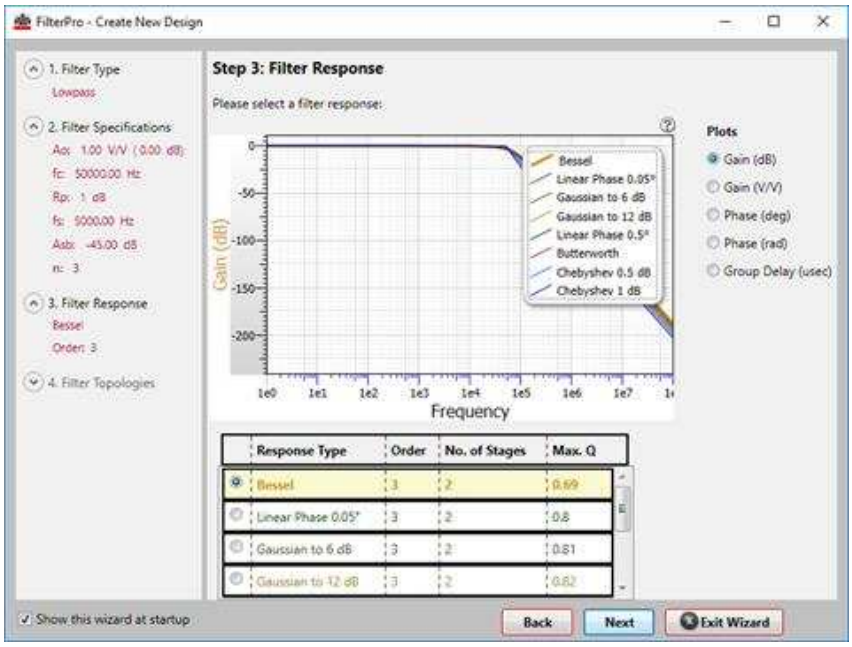
In step 1, *Lowpass* is selected since an antialias filter is a specific lowpass filter.



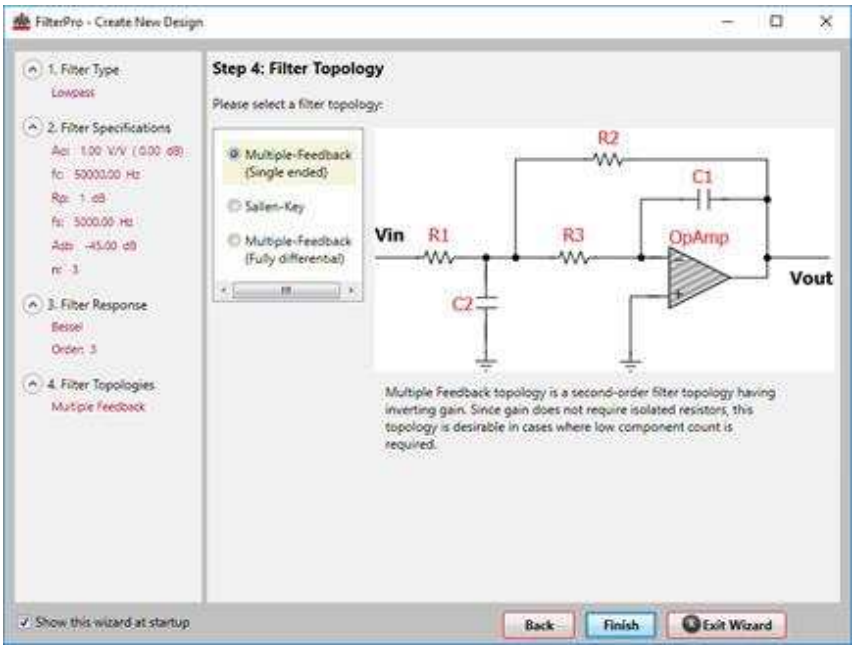
In step 2, the values for *Passband Frequency (f_c)* and filter order are filled in from the Analog Engineer's Calculator. The option to *Set Fixed* filter order must be selected to match calculated parameters.



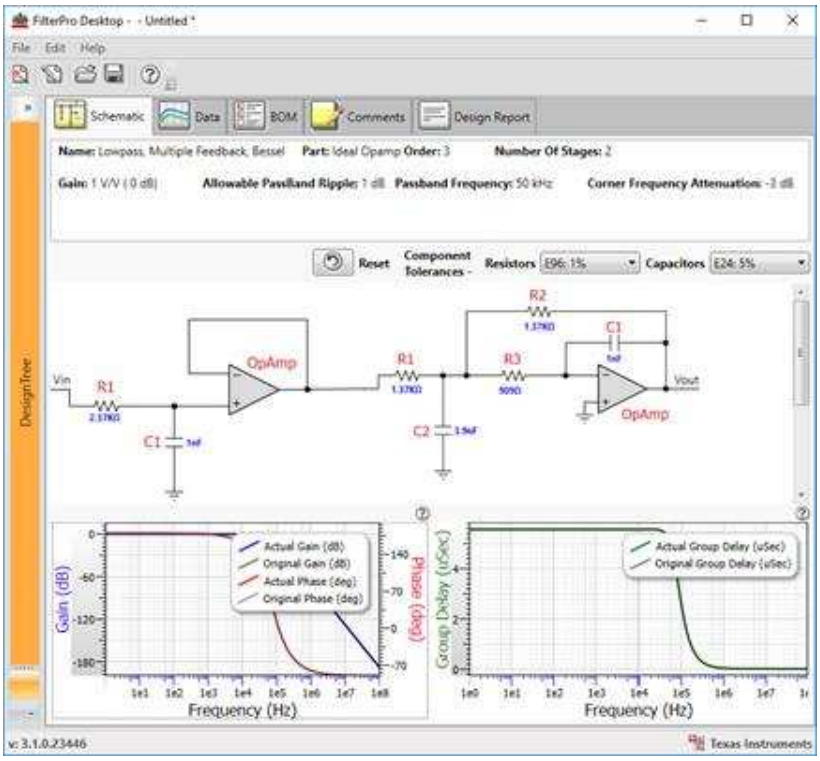
For step 3, select the filter type to match calculations; *Bessel* is chosen in this example for maximum flatness in the pass band and linear phase response.



Multiple feedback topology is chosen in step 4 because the filter attenuation will not be limited by the bandwidth of the op amp. This topology has the disadvantages of inverting a signal and offering low input impedance. *Sallen-Key* can also be selected since it is a non-inverting topology with high-input impedance, but at higher frequencies the attenuation of the filter will converge or even rise due to the bandwidth limitations of the op amp.



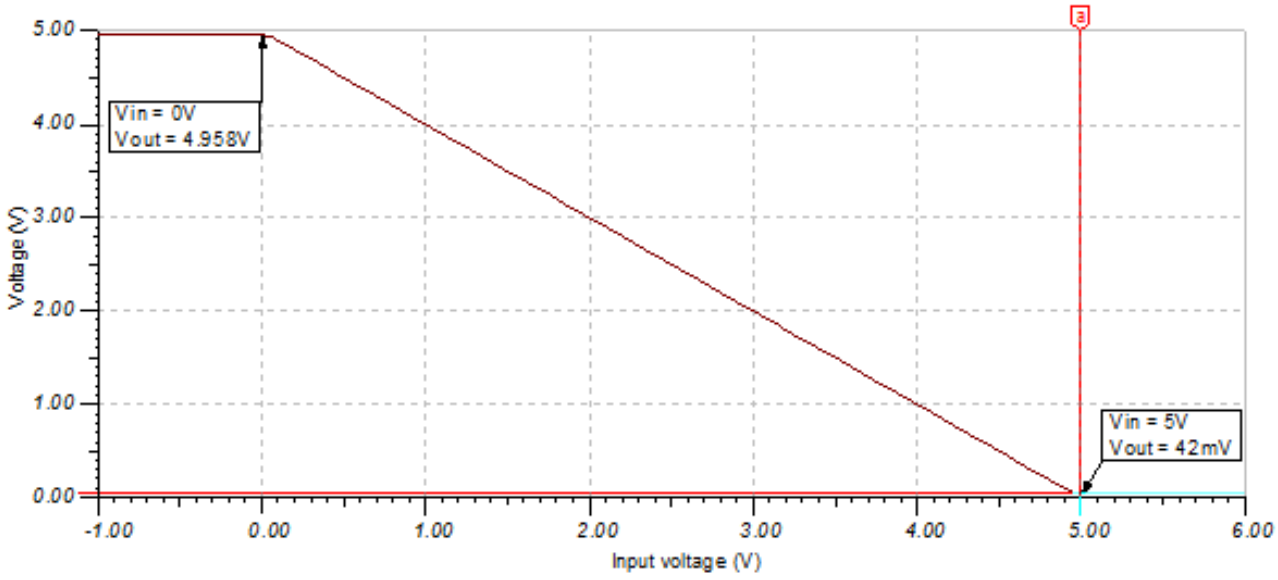
After clicking *Finish*, the filter schematic is displayed along with performance specifications of the resulting filter. Component tolerances can be adjusted using the right side drop-down menus; 1% resistors and 5% capacitors are chosen here as practical considerations. Component values can be modified by clicking on a number and entering new values.



The circuit previously pictured can be designed in TINA-TI for simulation. Performance characteristics are documented in the following sections.

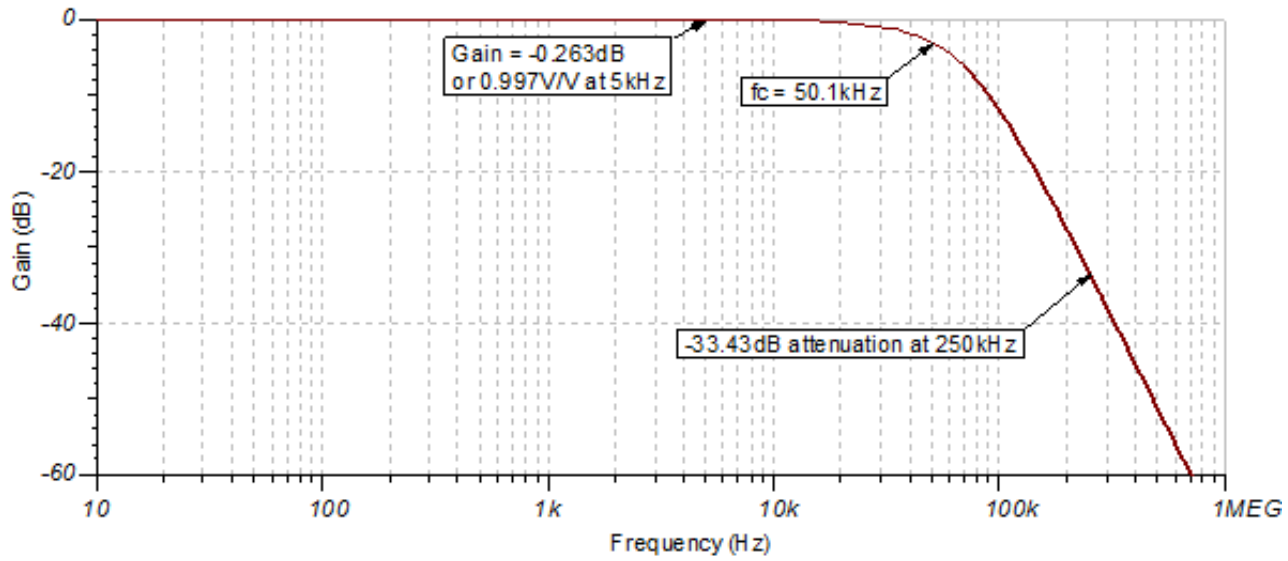
DC Transfer Characteristics

The following graph shows a linear output response for filter inputs from 0V to 5V. Since the filter amplifier is in inverting configuration, the output voltage is a function of $V_{out} = -V_{in} + 5V$.



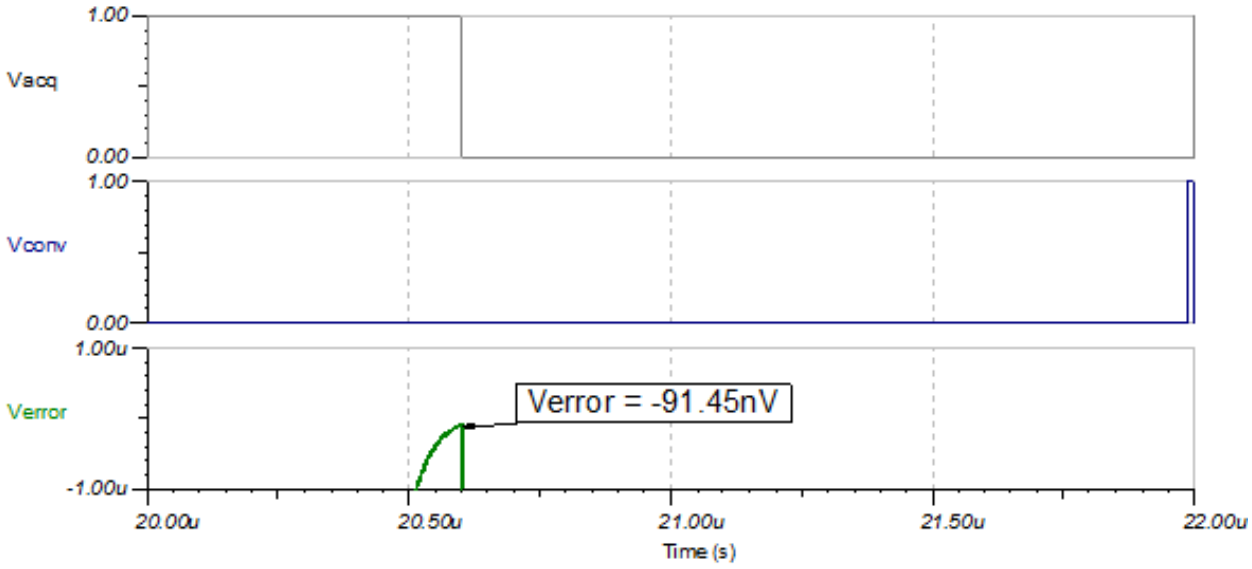
AC Transfer Characteristics

The bandwidth is simulated to be 50.1kHz, about 100Hz away from the desired value entered in the Analog Engineer's Calculator. At the Nyquist frequency, signals are attenuated by –33.43dB, which would lower the amplitude of the input alias signal to 21.3µV. See the TI Precision Labs *Op Amps: Bandwidth 1* for more details on this subject.



Transient ADC Input Settling Simulation

The following simulation shows the ADS8319 settling to a 5-Vpp AC signal at 5kHz through the data acquisition period. This type of simulation shows that the RC charge bucket components are properly selected. See the TI Precision Labs video on *Refine the Rfilt and Cfilt Values* for detailed theory on this subject.

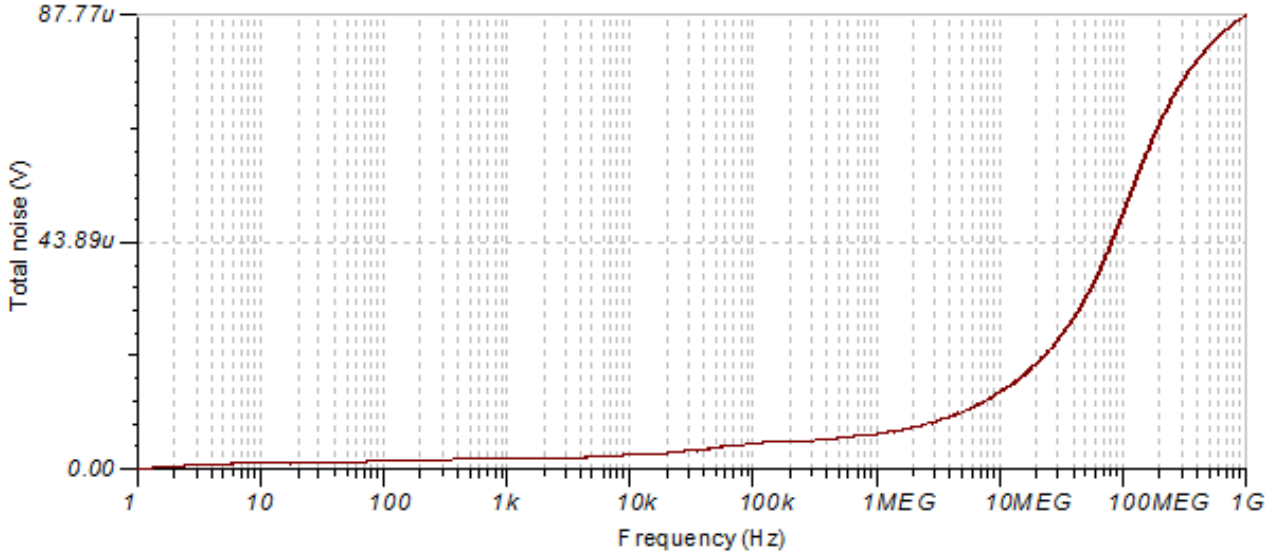


Noise Simulation

A simplified noise calculation is made here for a rough estimate. We neglect noise from the antialias filter in this calculation since it is attenuated for frequencies greater than 50kHz.

$$E_{nOPA365} = e_{nOPA365} \cdot G_{OPA}\sqrt{K_n \cdot f_c} = \left(7.2\,nV/\sqrt{Hz}\right) \cdot 1V/V\sqrt{1.57 \cdot 50MHz} = 63.8\mu V_{RMS}$$

The value for $e_{nOPA365}$ is taken from a data sheet noise curve. Note that calculated and simulated noise values match well. Some of the discrepancy between the simulated and calculated noise is due to inaccuracy from the bandwidth of the OPA365 model. See TI Precision Labs video on *Calculating the Total Noise for ADC Systems* for detailed theory on noise calculations.



Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS8319	16-bit, 500-kl, serial interface, micropower, miniature, SAR ADC	http://www.ti.com/product/ads8319	http://www.ti.com/adcs
OPA365	50-MHz, zero-crossover, low-distortion, high CMRR, RRI/O, single-supply operational amplifier	http://www.ti.com/product/opa365	http://www.ti.com/opamps

Link to Key Files

Source files for this design (http://www.ti.com/lit/zip/sbac197).

For direct support from TI Engineers use the E2E community:

e2e.ti.com

Other Links:

TI Analog Engineer's Calculator Download Link

TI FilterPro Desktop Download Link

TI Precision Labs series on *Introduction to SAR ADC Front-End Component Selection*

TI Precision Labs - ADCs

Digitally-Isolated ADS8689 Circuit Design

Reed Kaczmarek

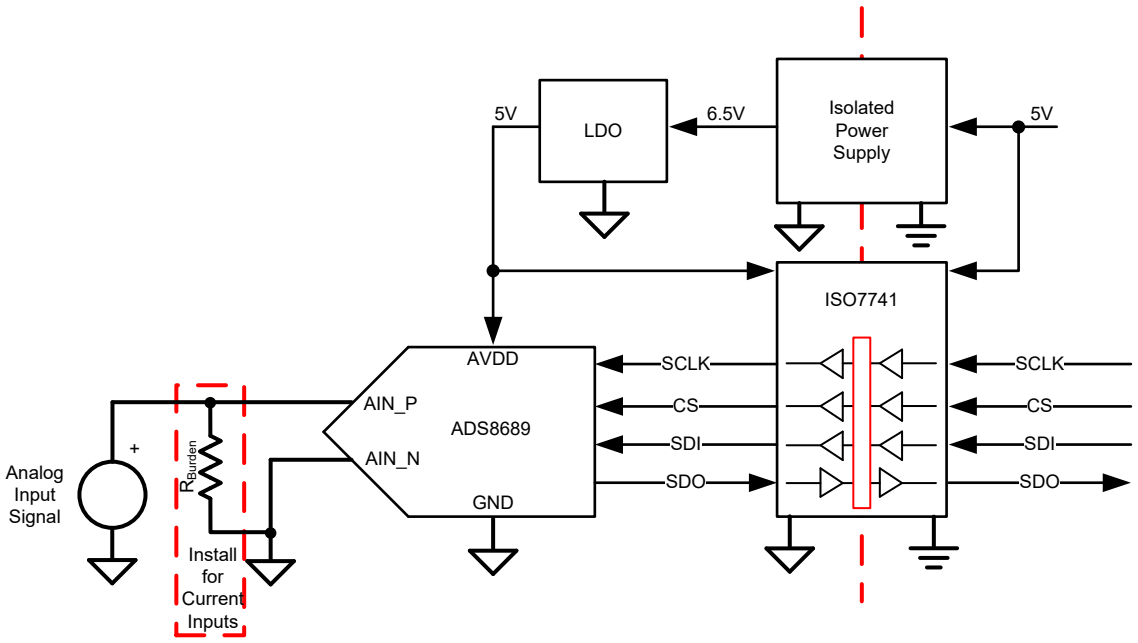
Input	ADC Input	Digital Output ADS7042
VinMin = –12.288V	AIN_P = –12.288V, AIN_N = 0V	8000_H or -32768_{10}
VinMax = 12.288V	AIN_P = 12.288V, AIN_N = 0V	$7FFF_H$ or 32767_{10}

Power Supplies		
AVDD	Vee	Vdd
5 V	6.5 V	5 V

Design Description

This design shows a digitally isolated high-voltage SAR ADC that is capable of full AC performance at maximum throughput. This design is intended for channel-to-channel isolated analog input modules as well as measuring a signal with a very large common mode. Programmable logic controller, analog input modules, and many 4- to 20-mA signal applications will benefit from this design. See *Isolated Power Supply Low-Noise, 5V, 100mA* for details on the isolated power supply design suitable for these applications. This cookbook includes links to design files.

This circuit implementation is applicable in applications such as *Analog Input Modules*, *Electrocardiogram (ECG)*, *Pulse Oximeter*, and *Bedside Patient Monitors*.



Specifications

Specification	Calculated	Measured
SCLK Frequency	6.66MHz	6.67MHz
Sampling Rate	100ksps	100ksps
Signal-to-Noise Ratio (SNR)	92dB	Min: 92.29dB Max: 92.46dB
Total Harmonic Distortion (THD)	–112dB	Min: –108.8dB Max: –111.38dB

Design Notes

1. Select a SAR ADC that will meet the input voltage range, sampling rate, and resolution for the system. This is covered in the *component selection* section.
2. Select a digital isolator that will allow for the required isolation specification as well as the correct number of channels and channel directions. This is covered in the *component selection* section.
3. Install the burden resistor for current inputs. This design will remove any common mode limitation of the inputs due to the channel-to-channel isolation. The burden resistor should be selected so that the maximum current input will stay within the full scale range of the SAR ADC.

Component Selection

1. Select a SAR ADC that meets the input voltage range, sampling rate, and resolution for the system:
   - Desired input range: ±12V
   - Desired effective number of bits (ENOB): 14 bits
   - Desired sampling rate: 100ksps
   - ADS8689 input range: ±12.228V
   - ADS8689 ENOB: 14.8 bits
   - ADS8689 maximum sampling rate: 100ksps

   NOTE: There is a wide selection of TI SAR ADCs that match the specifications in the previous list.

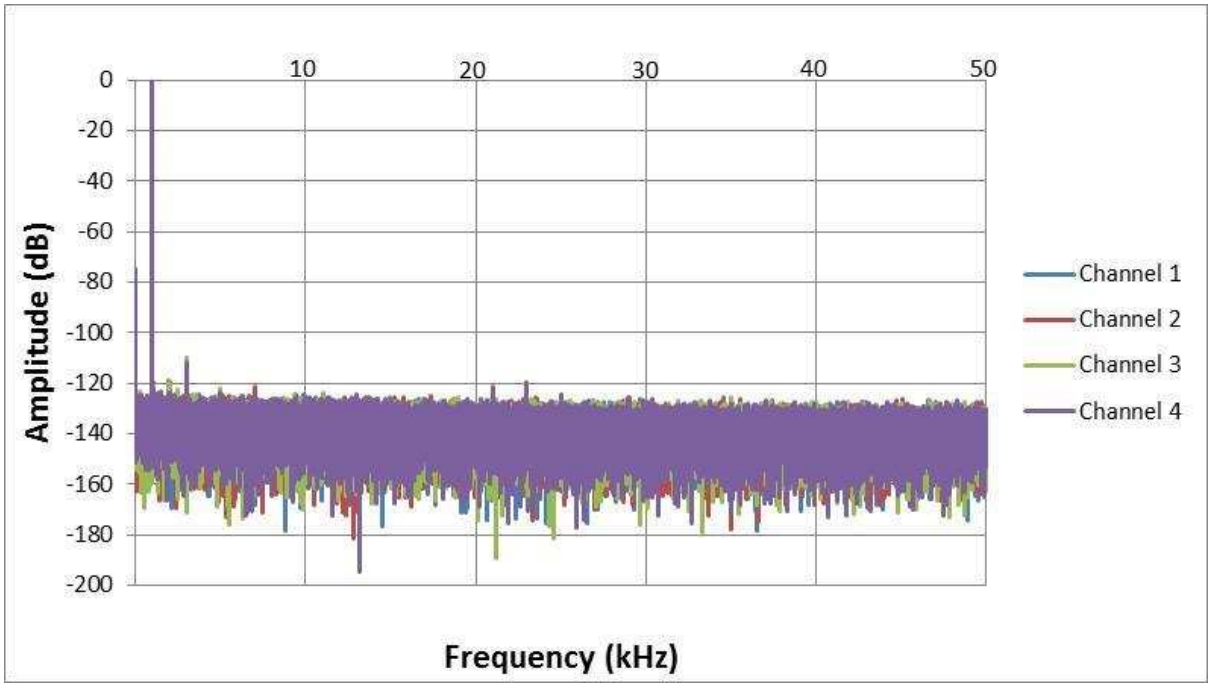
2. Select a digital isolator that will allow for the required isolation specification as well as the correct number of bidirectional channels:
   - TI offers digital isolators with isolation rating ranging from 2.5kV$_{RMS}$ to 5.7kV$_{RMS}$.
   - Choose isolation ratings based on the system requirements.
   - For a standard SPI interface, the digital isolator needs to be 4-channels with 3 channels in the same direction and 1 channel in the opposite direction.
   - The ISO774x is a digital isolator family for 4-channel devices with all combinations of channel directions and the ability to select a 2.5kV$_{RMS}$ or a 5.0kV$_{RMS}$ isolation rating.
3. Understand the expected delays to the digital signal from the digital isolator:
   - The ISO7741 has a typical propagation delay of 10.7ns with a maximum of 16ns.
   - Round trip isolation delay is 21.4ns typical or 32ns maximum.
   - SCLK is running at 6.66MHz resulting in a period of 150ns.
   - The typical roundtrip delay is 14% of the SCLK period.
   - The maximum roundtrip delay is 21% of the SCLK period.

   NOTE: The delay from the isolator results in a delay between the ideal SDO read relative to SCLK and the actual SDO read. This delay can be adjusted for by adding an SCLK return signal that travels through the digital isolator to all for the SDO to be read at exactly the correct time. Adding a return clock requires another channel of isolation.

Measured FFT

This performance was measured on a custom 4-channel, channel-to-channel isolated ADS8689 PCB. The input signal is a 24Vpp, 1-kHz sine wave. The AC performance indicates minimum SNR = 92.2dB and minimum THD = –108.8dB, which matches well with the specified performance of the ADC of SNR = 92dB and THD = –112dB.

Channel	SNR(dB)	THD (dB)
1	92.29	–109.95
2	92.38	–108.82
3	92.46	–109.53
4	92.42	–111.38



TVS Diode Performance Degradation

A 14-V bidirectional TVS diode was used in this design to protect the input of the SAR ADC. The TVS diode actually degrades total harmonic distortion (THD) due to the added capacitance. The THD was seen to be around 6dB worse with the TVS diode installed versus uninstalled.

Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS8689[1]	16 bit resolution, SPI, 100-ksps sample rate, single-ended input, and ±12.288-V input range.	http://www.ti.com/product/ADS8689	Similar Devices
ISO7741[2]	High-speed, robust-EMC reinforced quad-channel digital isolator	http://www.ti.com/product/iso7741	http://www.ti.com/iso

(1) The ADS8689 has in internal attenuator and programable gain amplifier that allows for a wide input voltage range.
(2) The ISO7741 is used to isolate the digital input signals.

Link to Key Files

Source files for Digitally-Isolated ADS8689 – http://www.ti.com/lit/zip/sbac179

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Other Links

www.ti.com/adcs

www.ti.com/opamp

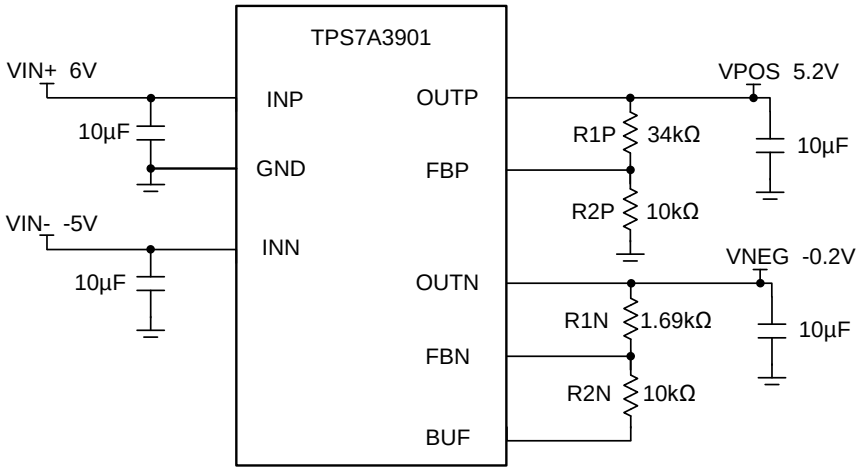
Powering a Dual-Supply Op Amp Circuit with One LDO

Reed Kaczmarek

LDO Input	LDO Output	Output Noise Level
Vin+ > 6V	5.2V	27µVRMS
Vin– < –5V	–200mV	22µVRMS

Design Description

This design shows a power supply that can be used to create a positive operational-amplifier (op amp) supply and a small negative op-amp supply. This small negative voltage is adjustable and is necessary in many operational amplifiers in order to ensure linearity down to ground. This design shows the TPS7A3901 as the power supply for creating the positive and negative voltage rails for operational amplifier circuits. This low dropout regulator (LDO) differs from most in its ability to regulate small negative voltages, as the following image shows. This is a generic circuit implementation that can be used in many *Industrial* applications.



Specifications

Measured Performance of ADS8900B With LDO

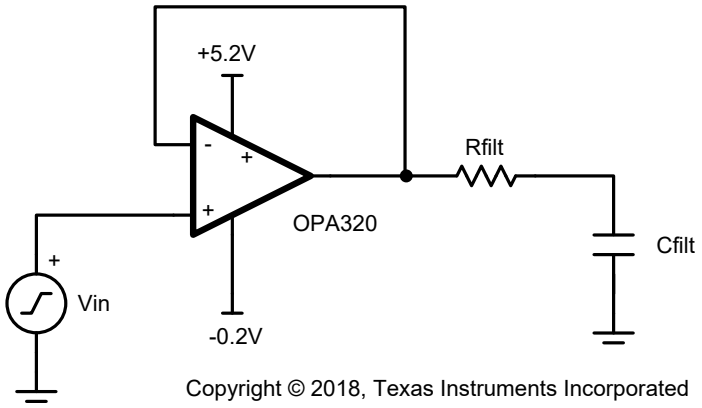
Parameter	Test Condition	Data Sheet Specification	Measured ADS8900B Performance
SNR	Vin_max = 5V, Vin_min = 0V	104.5dB	102.2dB
THD	Vin_max = 5V, Vin_min = 0V	–125dB	–123.5dB

Design Notes

1. Determine the linear range of the op amp based on common mode, output swing, and linear open-loop gain specification.
2. Set the adjustable LDO outputs to match the linear range of op amp.
3. Select X7R capacitors according to their temperature performance.
4. In cases where a negative supply is not available, an alternative solution is to use a *Low Noise Negative Bias Generator* (LM7705).

Component Selection

1. A common configuration shows in the following image using an OPA320 in a buffer configuration with a 0-V to 5-V desired linear signal swing. The power supplies are both 200mV away from the desired input and output swing. This topology ensures linear input and output swing for this amplifier.

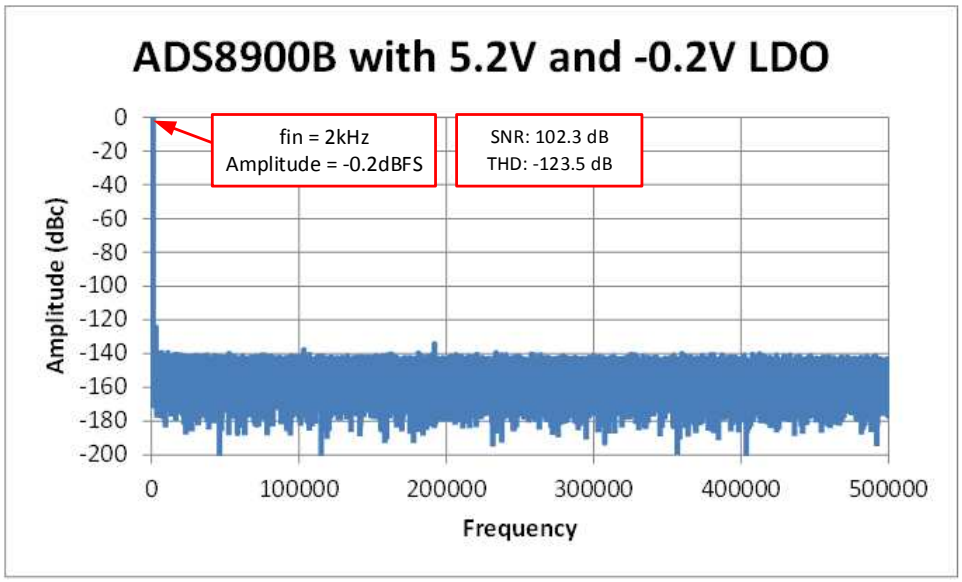


2. Select the components for the adjustable LDO outputs. Using the previous OPA320 example, the rails for the system will be –200mV and +5.2 V.

Desired Output	R1	R2
+5.2V	34kΩ	10kΩ
–200mV	1.69kΩ	10kΩ

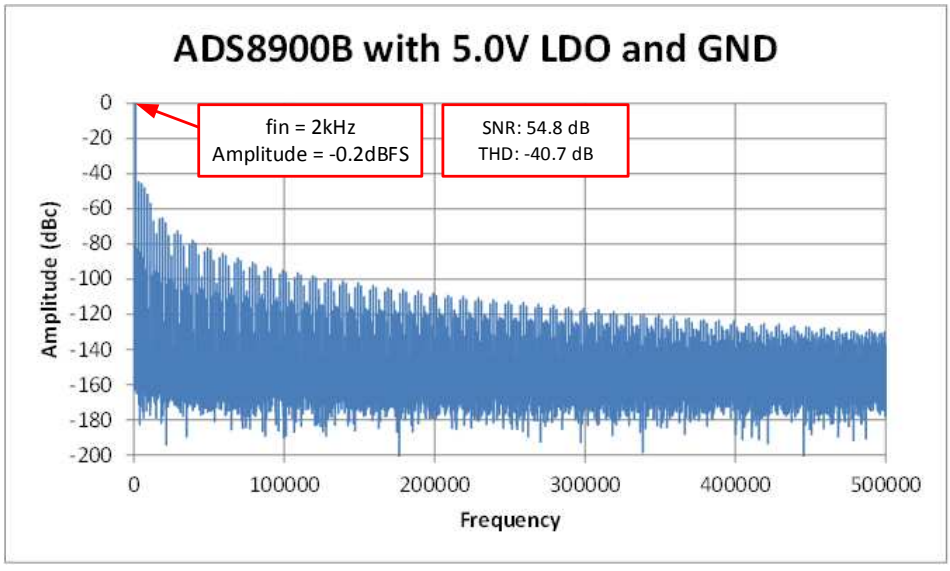
ADS8900B 20-Bit FFT Taken With LDO Adjusted to 5.2V and –0.2V

The FFT in the following was measured with an input signal very near full scale ±5V (–0.2dBFS). Note that the SNR and THD is very good compared to the case where the supply is adjusted to 5V and GND. Note the TPS7A3901 is a convenient way to generate a linear –0.2-V supply.



ADS8900B 20-Bit FFT Taken With LDO Adjusted to 5.0V and GND

The FFT shown in the following image was measured with an input signal very near full scale ±5V (–0.2dBFS). Note that the SNR and THD is poor compared to the case where the supply is adjusted to 5.2V and –0.2V.



Design Featured Devices

Device	Key Features	Link	Other Possible Devices
TPS7A3901	The TPS7A39 device is a dual, monolithic, high-PSRR, positive and negative low-dropout (LDO) voltage regulator capable of sourcing (and sinking) up to 150mA of current. It has a wide output voltage range of 1.2V to 30V for the positive output and –30V to 0V for the negative output. This device is ideally suited for generating a small negative supply voltage that is useful in cases where a single-supply amplifier needs a small negative supply so that the output can linearly swing to 0V.	http://www.ti.com/product/TPS7A39	Similar Devices
ADS8900B	Bipolar differential inputs, SAR ADC with internal reference buffer, SPI interface	Product Folder	Similar Devices
OPA320	Precision, Zero-Crossover, 20Mhz, RRIO, CMOS Operational Amplifier	Product Folder	Similar Devices

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Isolated Power Supply, Low-Noise Circuit: 5V, 100mA

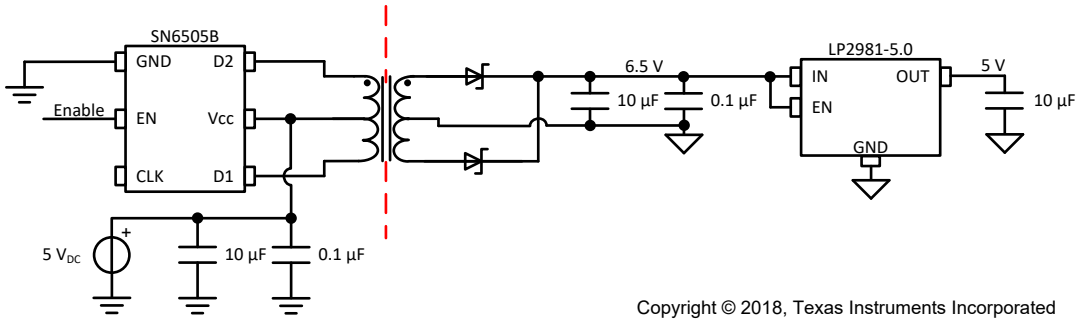
Reed Kaczmarek

Power Supplies		
AVDD	**Vee**	**Vdd**
5.0V	6.5V	5.0V

Design Description

This design shows an isolated power supply using a transformer driver and a low dropout regulator (LDO). This design is intended to be combined with a digitally-isolated SAR ADC, such as in *Digitally-Isolated ADS8689 Design*. *Industrial* applications that require an isolation interface are the primary application for this design in combination with a SAR ADC. The transformer driver and LDO can be selected differently based on the output current requirements and output voltage noise requirements. This power supply was built and tested on a PCB with the ADS8689 and later in this document the performance of the ADS8689 is shown to prove the effectiveness of the power supply.

This circuit implementation is applicable in applications such as *Analog Input Modules*, *Electrocardiogram (ECG)*, *Pulse Oximeters*, and *Bedside Patient Monitors*.



Specifications

Specification	Goal	Measured
LDO Output Current	< 100mA	16mA per channel
LDO Output Voltage Noise	< 1mV$_{RMS}$	N/A
ADS8689 Signal-to-Noise Ratio (SNR)	92dB	92.4dB
ADS8689 Total Harmonic Distortion (THD)	–112dB	111.3dB

Design Notes

1. Determine the required supply current that is needed on the secondary side of the transformer. This information is used for component selection.
2. Choosing the transformer and transformer driver are very important to creating a correct isolated power supply.
3. The CLK pin on the SN6505B can be connected to an external clock or left floating to use the internal 420-kHz clock.

Component Selection

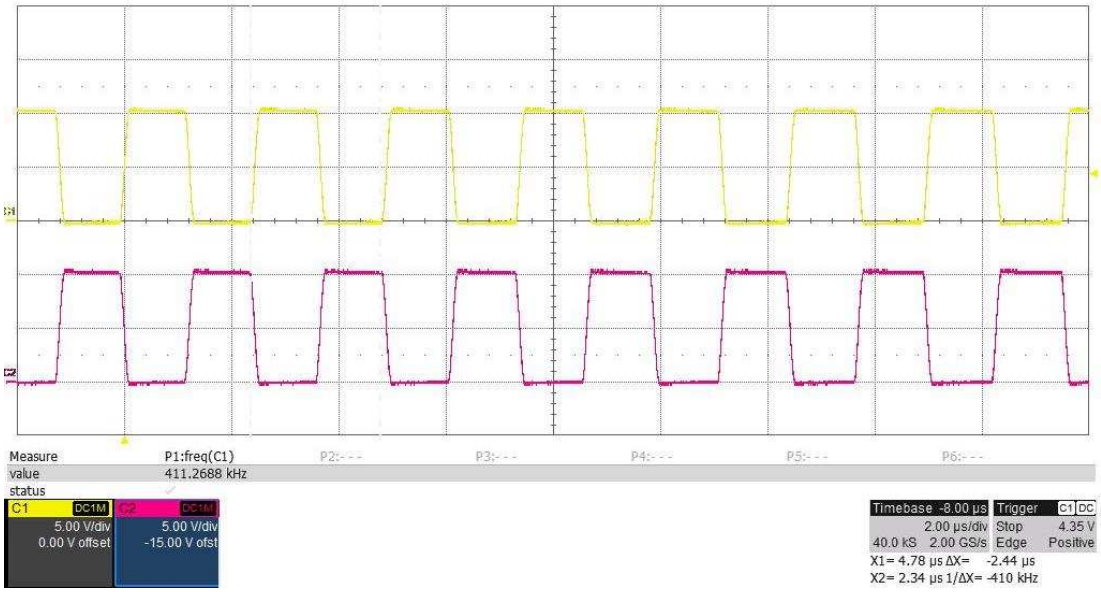
1. Select a transformer driver based on the required output current.
   - SN6505 will provide up to 1A of output current. The SN6505A has a 160-kHz internal clock and the SN6505B has a 420-kHz internal clock.
   - SN6501 will provide up to 350mA of output current.
2. Select a transformer with the desired turns ratio and current rating.
   - This design takes 5-V input and produces 6.5-V output. The turns ratio is determined as shown in the following:

$$\frac{n_p}{n_s} = \frac{V_{IN}}{V_{OUT}} = \frac{5V}{6.5V} = \frac{1}{1.3} \quad (1)$$

   - The 760390014 from Wurth Electronics was used in this design since it has a 1:1.3 turns ratio and a current rating that meets the 100-mA design specification.
3. Select a low dropout regulator (LDO) to use the transformer output and produce a low-noise supply voltage.
   a. The LDO should be selected to meet the output current requirement of the system and output voltage noise requirement of the system.
   b. The LP2981-5.0 is a fixed output voltage LDO that was selected for this design. This LDO is able to provide 100mA of output current. Also, the LDO output is accurate with only 160µV$_{RMS}$ of output voltage noise.
4. Select the rectifier diodes for the fast switching of the SN6505B.
   - The *SN6505x Low-Noise 1-A Transformer Drivers for Isolated Power Supplies* data sheet recommends using low-cost Schottky rectifier MBR0520L.
   - The forward voltage drop will take away from the output voltage of your isolated power supply.
   - The diodes must be rated for the expected current level for this supply.

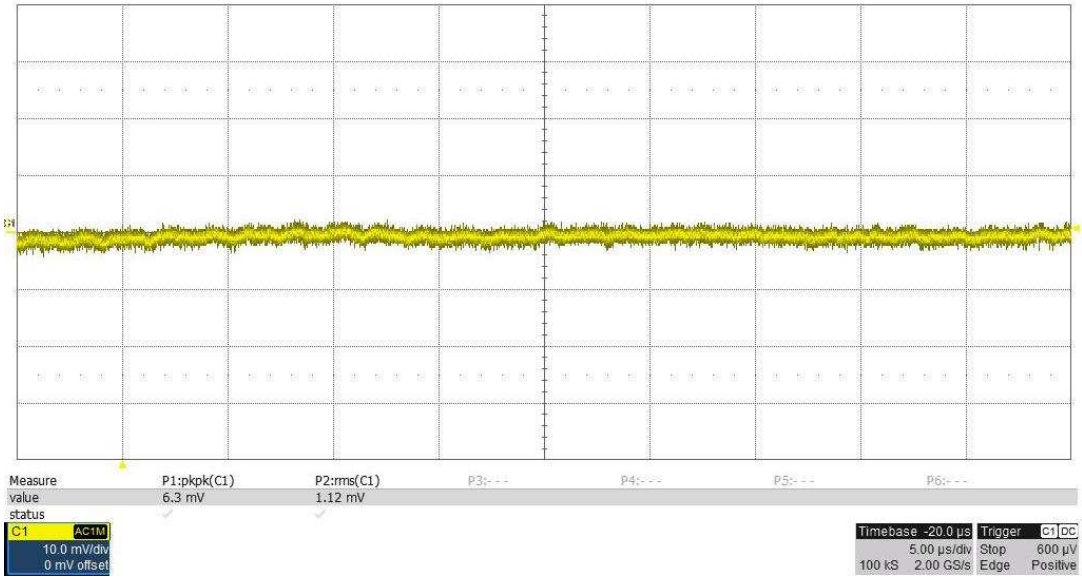
Measured Transformer Driver Outputs

The following image is an oscilloscope capture of the two transformer drive lines from the SN6505B. These are 0V to 5V pulses at a frequency of 411kHz.



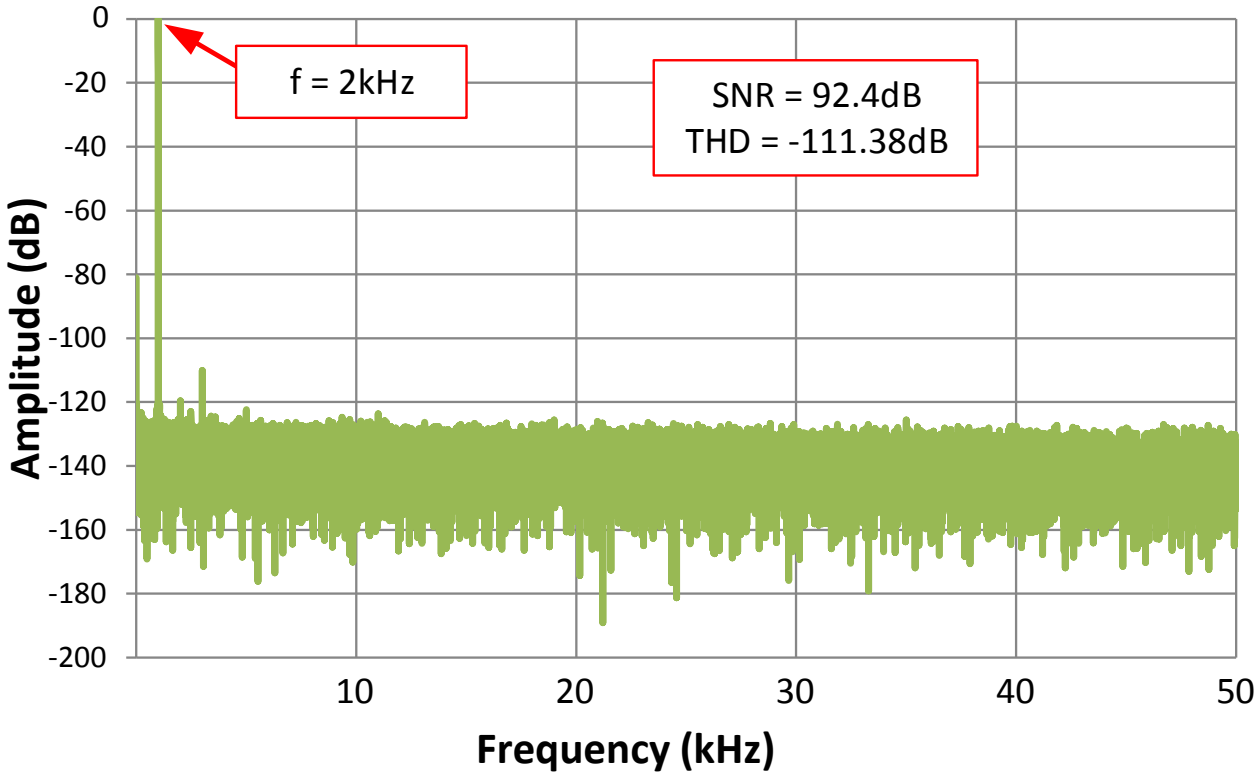
Measured SN6505B Stage Output Ripple

The following image is an oscilloscope capture of the output voltage following the rectifiers of the SN6505B power stage. This is the input to the LP2981-5.0 LDO. Result: 1.12mV$_{RMS}$.



Measured FFT

This power supply was implemented on a channel-to-channel isolated ADS8689 PCB. Measuring the AC performance of the ADS8689 proves the effectiveness of this isolated power supply. The AC performance indicates SNR = 92.4dB and THD = –111.3dB, which matches well with the specified performance of the ADC: SNR = 92dB and THD = –112dB).



Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS8689	12-bit resolution, SPI, 1-Msps sample rate, single-ended input, AVDD/Vref input range 1.6V to 3.6V.	http://www.ti.com/product/ADS8689	Similar Devices
SN6505B	Low-Noise 1-A, 420-kHz transformer driver	http://www.ti.com/product/SN6505B	Transformer Driver
LP2981	100mA ultra-low dropout regulator with shutdown	http://www.ti.com/product/LP2981	Linear Regulator (LDO) – Products

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