Application Report
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Use Conditions for 5-V Tolerant GPIOs on Tiva™ C Series TM4C123x Microcontrollers

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ABSTRACT

The Tiva C Series TM4C123x family of ARM® Cortex™–M4 microcontrollers features highly programmable, 5-V tolerant general-purpose input/outputs (GPIOs) with internal clamping and fail-safe electro static discharge (ESD) protection. The internal clamping and the fail-safe ESD protection require specific use conditions for external signal characteristics that must be followed at all times for proper operation of the device. Failure to follow these use conditions may result in improper operation or cause damage to the device. This application report describes GPIO characteristics, their limitations and use case conditions. This application report also suggests methods to protect the internal circuitry of the GPIO pins if they are subjected to signals that exceed maximum rating conditions as specified in the device-specific data sheet.

Contents

1 Introduction

TM4C123x microcontrollers have three types of I/Os with respect to the ESD protection and leakage current:

- Power I/Os (VDD, VDDA, VDDC, VBAT, GND, GNDA, GNDX)
- I/Os with fail-safe ESD protection (GPIOs, XOSCn pins, USBD+, USBD-). For exceptions, see the device-specific data sheets.
- I/Os with non-fail-safe ESD protection (VREFA+, VREFA-, any non-power, non-GPIO, non XOSCn pins)

This application report only discusses the GPIOs. The 5-V tolerant GPIOs in TM4C123x microcontrollers include internal clamping and fail-safe ESD protection. It is important to note that GPIOs configured as inputs are 5-V tolerant, not 5-V compliant meaning that 5 V is tolerated by internally clamping the input voltage to V_{DD}. Such clamping does not affect the voltage at the GPIO pin; it only affects the voltage swing in internal nodes.

Table 1 summarizes the clamping mechanisms for different modes in which GPIOs can be configured. More detail on these mechanisms is covered in Section 2.

Table 1. Clamping Mechanisms for Different Modes

GPIO Configuration	Clamping Mechanism	
Digital Function	Input Mode	Integrated clamping and protection circuit translates the voltage applied to a GPIO pin (V_{IN}) to an acceptable internal voltage level.
	Output Mode	The voltage output by a GPIO pin (V_{OUT}) is limited between 0 V and V_{DD}.
	Open-drain Mode	An external resistor connected between an external power supply and a GPIO allows the GPIO pin to drive larger signals. In this mode, the external supply must be limited to 5.5 V.
Analog Function	Input/ Output Mode	Clamping protects internal circuitry, allowing voltages greater than V_{DD} to be applied to GPIO pins, but analog specifications are not ensured if the voltage applied to the pin is not in the range 0 V to V_{DD}.

Figure 1 below shows a simplified representation of the 5V-tolerant GPIOs in TM4C123x microcontrollers.

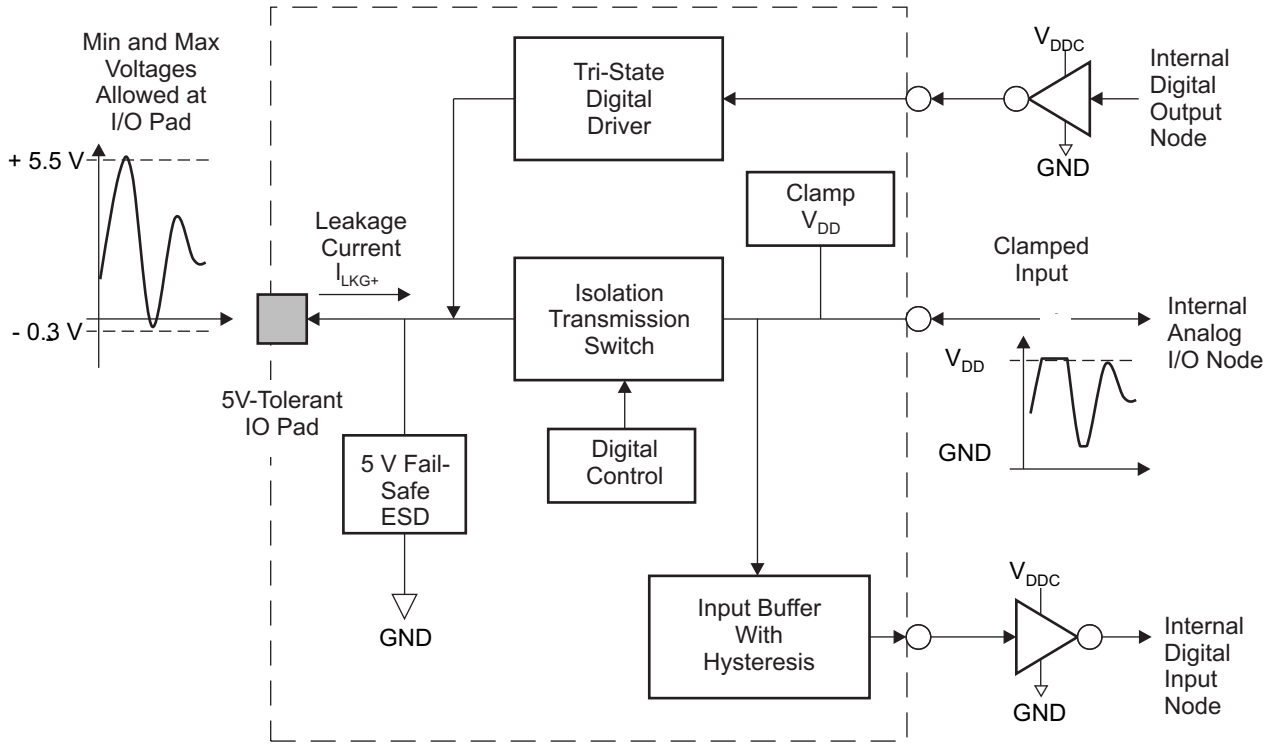

Figure 1. Block Diagram of 5V-Tolerant GPIOs

2 Use Conditions

The following section summarizes the use conditions for GPIOs on TM4C123x microcontrollers. Some of the use conditions are discussed in more detail in the subsequent sections of this application report.

1. GPIOs configured as inputs are 5-V tolerant, not 5-V compliant.
2. V_{IN}, the voltage applied to a GPIO pin, regardless of whether the microcontroller is powered or not, must be between -0.3 V and 5.5 V to ensure reliability. The microcontroller is not ensured to operate properly at the maximum ratings.
3. V_{IN} must be between 0 V and V_{DD} to ensure that analog specifications for the corresponding pin are met. For V_{IN} greater than V_{DD}, analog functionality suffers, and specifications are not met.
4. For V_{IN} ϵ (0 V, V_{DD}), the leakage current is less than 1 µA for most I/Os up to 85°C, and leakage current is less than 2 µA for ADC inputs and the ADC reference inputs.

5. For V_{IN} ϵ (-0.3 V, 0 V) and V_{IN} ϵ (V_{DD}, 5.5 V), the leakage is outside normal range, but is still well bounded.
   (a) For V_{IN} ϵ (-0.3 V, 0 V) and V_{IN} ϵ (V_{DD}, 5.5 V), the leakage is outside normal range, but is still well bounded.
   (b) For V_{IN} ϵ (V_{DD}, 5.5 V), the leakage current is less than 700 µA.
6. If there is a possibility that V_{IN} can be outside the absolute maximum ratings in the end-applications, I/Os must be protected with an external current-limiting series resistor.
   (a) For V_{IN} < -0.3 V, add: R_{INJ}-> (|V_{IN}| – 0.3 V)/ 0.5 mA.
   (b) For V_{IN} > 5.5 V, add: R_{IN} > (V_{IN} – 5.5 V)/ 20 µA.
   The equation above results in a value for R_{IN} that is highly impractical in most cases. It is recommended to keep V_{IN} < 5.5 V in all cases.
7. An unpowered device cannot be parasitically powered through the I/O pin, which has fail-safe protection. Maximum leakage current from a GPIO to any floating supply in absence of V_{DD}, $I_{LKGunpw}$, is less than 25 nA at V_{IN} = 5.5 V.
8. When a GPIO is configured as a digital output in open-drain mode, for a desired V_{OUT} output voltage, with V_{DDEXT} , external supply limited to 5.5 V, less than 5.5 V, the value of the external pull-up resistor can be calculated as follows:
   (a) R_{PU} < (V_{DDEXT} – V_{OUT})/I_{LEAKpd}; where I_{LEAKpd} ~ 30 µA

3 GPIOs in Input Mode

When a GPIO is used as an input, reliable operation can be ensured only if the voltage applied to the GPIO is inside the maximum rating conditions. Normal analog functionality is ensured only if the voltage applied to any GPIO configured for an analog function is inside the recommended operating conditions.

If the voltage applied to any GPIO is between the operating condition limits and the absolute maximum rating limits, reliability can be ensured, but specified analog functionality cannot.

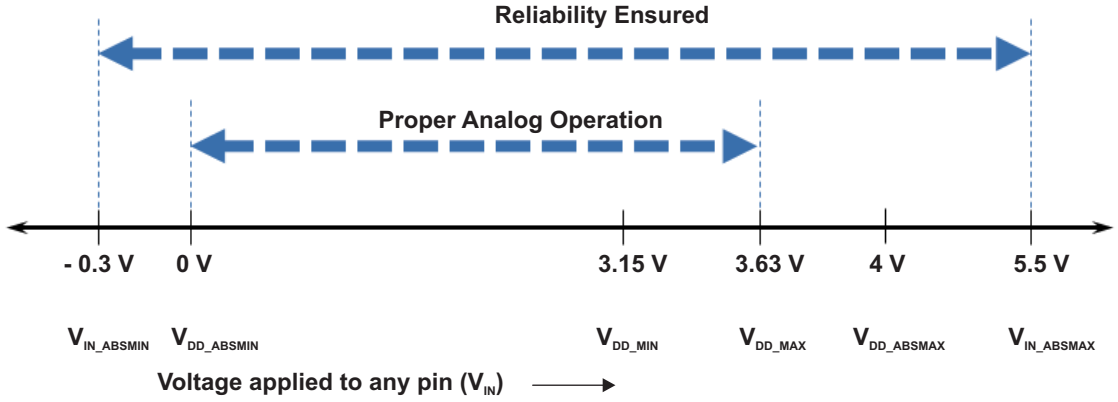

Figure 2. Regions of Reliability and Proper Analog Operation

V_{IN}	=	Input voltage applied to a GPIO, regardless of whether the microcontroller is powered.
V_{IN_ABSMIN}	=	Absolute minimum voltage that can be applied to any GPIO pin.
V_{IN_ABSMAX}	=	Absolute maximum voltage that can be applied to any GPIO pin.
V_{DD_ABSMIN}	=	Absolute minimum voltage that can be applied to VDD pin
V_{DD_ABSMAX}	=	Absolute maximum voltage that can be applied to VDD pin.
V_{DD_MIN}	=	Minimum supply voltage required for proper device operation.
V_{DD_MAX}	=	Maximum supply voltage required for proper device operation.

3.1 GPIO Protection and Leakage Current When the Device is Powered

3.1.1 Case I: V_{IN} < -0.3 V

Reliability is not ensured when a voltage outside absolute maximum ratings is applied to a GPIO pin. External components must be used to protect the device from damage.

Maximum negative injection current must be limited to 0.5 mA when a voltage less than -0.3 V is applied to a fail-safe GPIO pin. The ESD structure limits maximum negative voltage to approximately 0.6 V, but the current can increase without bounds and can potentially cause damage to the device.

If the system operating conditions involve applying a voltage less than -0.3 V to a GPIO pin, a series resistor (R_{INJ-}) must be connected between the GPIO pin and the voltage source. The value of the series resistor can be calculated using the following expression:

$R_{INJ-} > (|V_{IN\_WCMIN}| – 0.3\ V)/I_{MAXINJ-}$ (i)

Where,

V_{IN_WCMIN} = worst case minimum voltage expected under any conditions,

$I_{MAXINJ-}$ = injection current, 0.5 mA

3.1.2 Case II: $V_{IN} \in (-0.3\ V, 0\ V)$

The parasitic diode to GND does not conduct when a voltage between -0.3 V and 0 V is applied to a GPIO pin. The leakage current is internally limited to less than 10 µA under all PVT conditions.

3.1.3 Case III: $V_{IN} \in (0\ V, V_{DD})$

The leakage current into a GPIO is less than 1 µA for most GPIOs and less than 2 µA for the ADC pins when a voltage inside the recommended operating conditions, $V_{IN} \in (0\ V, V_{DD})$, is applied to a GPIO pin.

3.1.4 Case IV: $V_{IN} \in (V_{DD}, 5.5\ V)$

The leakage current is well bounded (but not as low) when a voltage higher than the recommended operating voltage condition, but lower than the absolute maximum rating, is applied to a GPIO pin. Inside this voltage range, leakage current actually increases when going from V_{DD} to 5.5 V, but it is still internally limited.

- When $V_{IN} \in (V_{DD}, 4\ V)$, nominal leakage current is approximately 60 µA. The maximum leakage current is less than ~700 µA. Inside this voltage range, leakage is actually larger than at higher voltages due to clamping circuits not being completely turned on.
- When $V_{IN} \in (4\ V, 5.5\ V)$, nominal leakage current is approximately 30 µA. The maximum leakage current is less than 60 µA.

Because GPIOs use fail-safe ESD circuitry, there is no diode between the GPIO pin and V_{DD}, and therefore no path from the GPIO pin to the V_{DD} supply. As a result, there is no forward-biased diode current when $V_{IN} > V_{DD} + 0.6\ V$ is applied as it would happen otherwise on GPIO with non-fail-safe ESDs.

Leakage is internally limited to less than 700 µA for any PVT condition for $V_{IN} \in (V_{DD}, 5.5\ V)$ and such an operating condition should not pose a reliability issue.

3.1.5 Case V: $V_{IN} > 5.5\ V$

In order to meet reliability requirements, a voltage greater than 5.5 V should not be applied to any GPIO. In fail-safe ESD structures, an internal diode is not connected between the GPIO pin and V_{DD} to limit positive voltage excursions. The fail-safe ESD structure is only triggered at voltages greater than 8 V.

It is important that even during initial transient conditions, the voltage at the GPIO pin must not go above 5.5 V to avoid potential damage to the GPIO circuitry.

In very special cases such as carefully controlled DC inputs, a series resistor (R_{IN}) can be connected to limit the voltage at the GPIO from going above 5.5 V. The value of the series resistor can be calculated using the following expression:

$R_{IN} > (V_{IN\_WCMAX} – 5.5\ V)/I_{LEAKmin+}$ (ii)

Where,

V_{IN_WCMAX} = worst case maximum voltage expected under any conditions,

$I_{LEAKMIN+}$ = 20 µA.

In most applications, the calculated value of R_{IN} turns out to be very large. Often, this value is so large that it is impractical to use an external series resistor with typical digital inputs because it can highly limit the speed of analog inputs. Connecting a series resistance is useful only in very special applications. The best practice, therefore, is to make sure that the voltage at the GPIO pin does not exceed above 5.5 V.

Example:

If V_{IN_WCMIN} = -1.0 V, V_{IN_WCMAX} = 7.0 V, $I_{MAXINJ-}$= 0.5 mA and $I_{LEAKMIN+}$= 20 µA, and using expressions (i) and (ii), the value of R_{INJ-} and R_{IN} can be calculated as:

R_{INJ-} = (1-0.3)/0.5 mA = 1.4 KΩ

R_{IN} = (7-5)/25 µA = 80 KΩ

Using R_{INJ-} = 1.4 KΩ limits the negative injection current to 0.5 mA, and using R_{IN} = 80 KΩ limits the positive voltage at the GPIO pin to less than 5.5 V. Connecting a 80 KΩ series resistance may be impractical in most applications.

NOTE:

- It is assumed in all cases, that the device has been powered on before any voltage has been applied to a GPIO pin.
- In the case of pins configured as analog inputs, a series resistance (R_S) is required for proper analog functionality. Connecting external current limiting resistors (R_{INJ-} or R_{IN}) will affect equivalent series resistance and therefore, analog operation. For the values of analog source resistance (R_S) requirements for proper ADC operation, see the *ADC Electrical Characteristics* in the device-specific data sheet.

The leakage current characteristics for cases II, III and IV are shown in Figure 3.

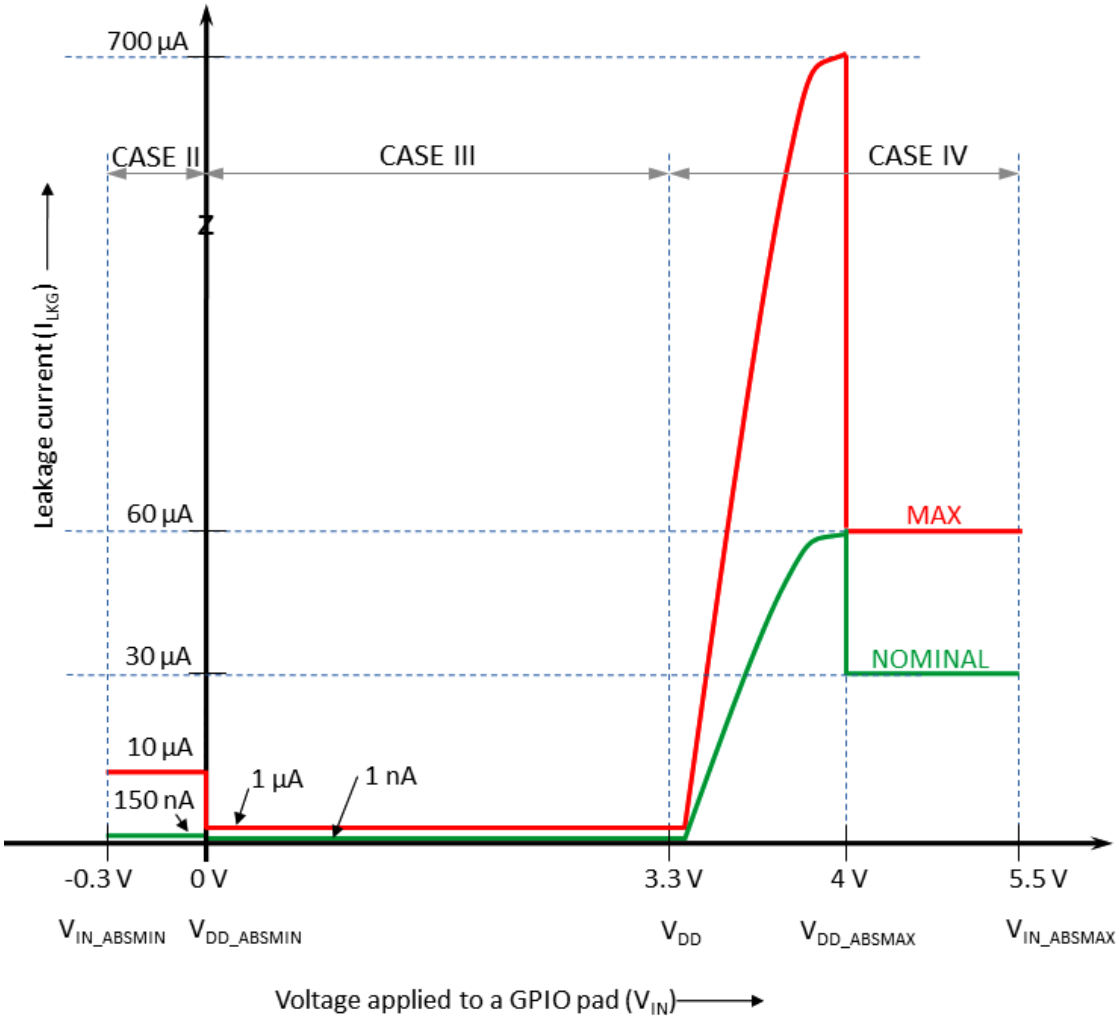

Figure 3. Relationship Between Leakage Current and Voltage Applied to a GPIO Pin at Nominal Temperature
(*approximate representation, graph not to scale***)**

3.2 Leakage Current When Device is Unpowered

When the device is not powered, or when the power pins are floating, the device cannot be powered through a signal pin because of the fail-safe ESD protection mechanism, as there is no path between the input/output pad and supply rails.

3.2.1 Case I: V_{IN} < -0.3 V

Maximum negative injection current must be limited to 0.5 mA when a voltage less than -0.3 V is applied to a fail-safe GPIO pin. As discussed in Section 3.1.1, Case I, a series resistor R_{INJ-} should be used to protect the GPIO pin. Note that applying V_{IN} < -0.3 V, violates the absolute maximum rating specification.

3.2.2 Case II: V_{IN} ϵ (-0.3 V, 0 V)

The leakage current is less than 10 µA for all PVT conditions when a voltage between -0.3 V and 0V is applied to a fail-safe GPIO.

3.2.3 Case III: V_{IN} > 3.3 V

An unpowered device cannot be parasitically powered through the I/O pin that has fail-safe protection. The maximum leakage current, $I_{LKGunpw}$, from a GPIO to V_{DD} or V_{DDA} supply rail in absence of V_{DD} is limited to less than 25 nA at V_{IN} = 5.5 V.

Note that applying V_{IN} > 3.53 V may cause reliability issues.

- In absence of V_{DD}, V_{IN} = 5.5 V should only be applied for a maximum of 10,000 hours at 27°C, over the lifetime of the product.
- In absence of V_{DD}, V_{IN} = 5.5 V should only be applied for a maximum of 5,000 hours at 85°C, over the lifetime of the product.
- In absence of V_{DD}, V_{IN} = 3.63 V can be applied for the entire lifetime of the product.

There is no limitation on how long V_{IN} = 5.5 V can be allowed while V_{DD} is present.

4 GPIO in Digital Output Mode

4.1 Normal Mode

The output voltage (V_{OUT}) is between 0 V and V_{DD} in normal mode.

$V_{OUT} \epsilon (0\ V, V_{DD})$

4.2 Open-Drain Mode

An external resistor is connected in series between the pin and an external power supply to drive larger output signals in open-drain mode. The external power supply (V_{DDEXT}) should be limited to 5.5 V.

Reliability issues result if voltages higher than 5.5 V are applied to a GPIO pin during any transient condition. Supply sequencing and transient voltages pose too much risk, so the safest solution is to limit the external supply to 5.5 V.

There is a weak internal pull-down connected to the GPIO pins. The external pull-up resistor must be sized correctly to achieve the expected swing at the output pin. The value of the external pull-up resistor (R_{PU}) can be calculated using the following expression knowing the value of the weak pull-down current (I_{LEAKpd}) in open-drain mode.

$$R_{PU} < (V_{DDEXT} - V_{OUT})/I_{LEAKpd} \quad \text{(iii)}$$

Where,

R_{PU} = External pull-up resistor

V_{DDEXT} = External supply limited to 5.5 V

V_{OUT} = Voltage at the GPIO pin

I_{LEAKpd} = Open-drain, output driver weak-pull down current source, 30 µA (nominal value), $I_{LEAKpd} \epsilon$ (15 µA, 60 µA) for all PVT conditions.

Figure 4 shows this configuration.

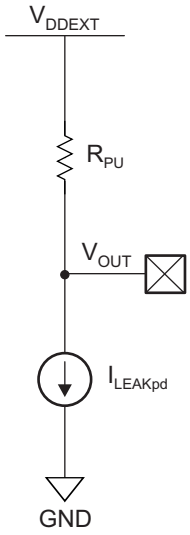

Figure 4. Connecting an External Pull-Up Resistor in Open-Drain Mode

Example:

If V_{DDEXT} = 5.5 V, V_{OUT} = 4.5 V, I_{LEAKpd} = 30 µA, using expression (iii), the value of R_{PU} can be calculated as:

R_{PU} = (5.5 V – 4.5 V)/30 µA = 33 KΩ

5 Conclusion

In this application report, 5-V tolerant GPIOs with internal clamping and fail-safe ESD protection in the Tiva C Series TM4C123x microcontrollers were discussed. Leakage characteristics, limitations and use case conditions for the GPIOs were also described. Methods were suggested to protect the GPIO's internal circuitry if GPIO pins are subjected to signals that exceed absolute maximum rating conditions as specified in the device-specific data sheet.

It is important to note that GPIOs configured as inputs are 5-V tolerant, not 5-V compliant, which means that 5-V inputs are tolerated by internally clamping the input voltage to V_{DD}. Such clamping does not affect the voltage at the input pin; it only affects the voltage swing in internal nodes. The internal clamping and the fail-safe ESD protection require specific use conditions for external signal characteristics that must be followed at all times for proper operation of the device. Failure to follow these use conditions may result in the damage to the device. Additionally, GPIOs can be connected to a 5-V external voltage source with an external pull-up resistor when they are configured as open drain outputs. The leakage current into the GPIO pin depends on the voltage at that pin, which in turn depends on the value of the external pull-up resistor. Therefore, the external pull-up resistor should be sized such that the leakage is around 30 µA and the voltage at the pin is as close to 5-V as possible.

NOTE: The electrical characteristics in this application report that are not specified in the device-specific data sheet are obtained from design simulation or limited bench testing. They have not been characterized or production tested.

6 References

- *Tiva™ C Series Data Sheet* (individual device-specific documents available through the product folders)
- *Tiva™ C Series Errata* (individual device-specific documents available through the product folders)
- *Tiva™ C Series ROM User's Guide* (individual device-specific documents available through the product folders)
- TivaWare™ Peripheral Driver Library for C Series

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