GPMC Sub-32-bit Read Issue

Problem Statement

- 8-bit sequential reads on an 8-bit NAND does not work on AM64 silicon
- Changing to 32-bit sequential reads works fine

```
>>>>>>> [    0.263677] read8 0x4f
>>>>>>> [    0.263683] read8+1 0x00
>>>>>>> [    0.263773] read8+2 0x00
>>>>>>> [    0.263781] read8+3 0x00
>>>>>>> [    0.263787] read8 0x00
>>>>>>> [    0.263793] read8+1 0x00
>>>>>>> [    0.263800] read8+2 0x00
>>>>>>> [    0.263806] read8+3 0x00
>>>>>>> [    0.263813] read8 0x4d
>>>>>>> [    0.263819] read8+1 0x4e
>>>>>>> [    0.263825] read8+2 0x20
>>>>>>> [    0.263832] read8+3 0x39
>>>>>>> [    0.263838] read8 0x46
>>>>>>> [    0.263845] read8+1 0x41
>>>>>>> [    0.263851] read8+2 0x48
>>>>>>> [    0.263857] read8+3 0x20
>>>>>>> [    0.263864] read8 0x2c
>>>>>>> [    0.263870] read8+1 0x00
>>>>>>> [    0.263877] read8+2 0x00
>>>>>>> [    0.263883] read8+3 0x00
>>>>>>> [    0.263889] read8 0x00
>>>>>>> [    0.263895] read8+1 0x01
>>>>>>> [    0.263902] read8+2 0x00
>>>>>>> [    0.263908] read8+3 0x00
>>>>>>> [    0.263915] read8 0x00
>>>>>>> [    0.263921] read8+1 0x23
>>>>>>> [    0.263927] read8+2 0x04
>>>>>>> [    0.263934] read8+3 0x00
```

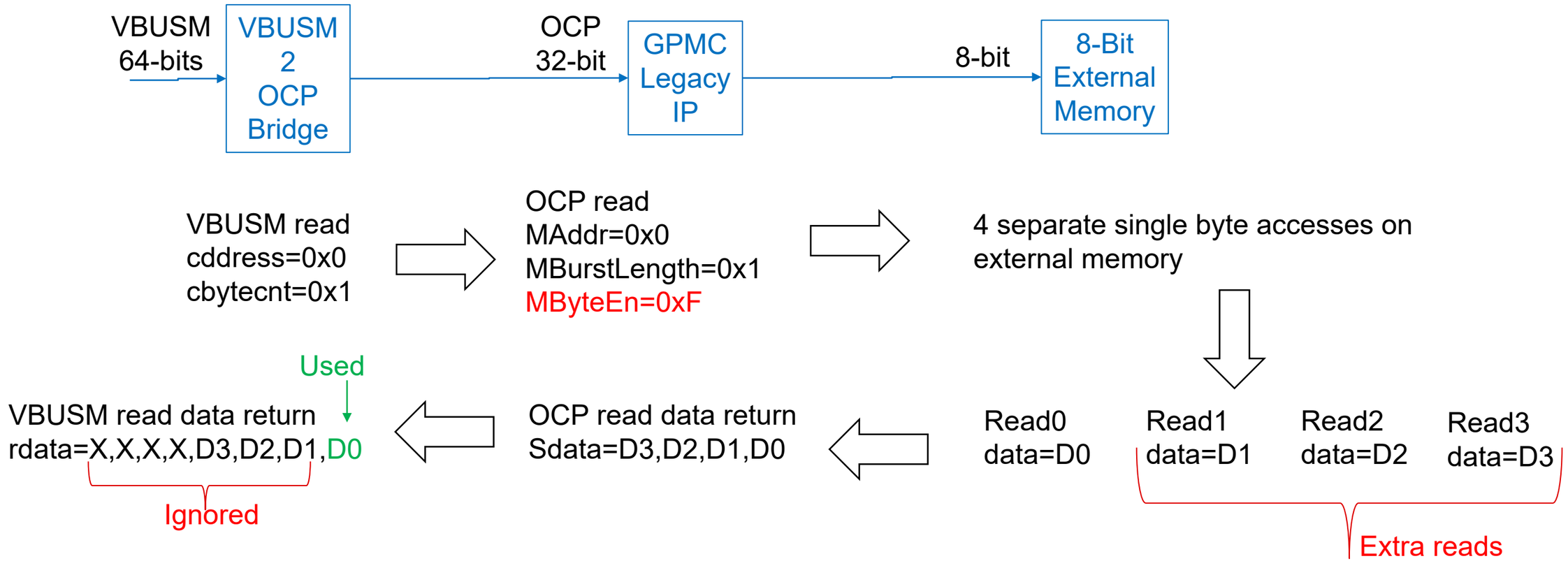
Incorrect Data

```
>>>>>>> [    0.263812] read32 0x49464e4f
>>>>>>> [    0.263819] read32 0x001a0002
>>>>>>> [    0.263825] read32 0x0000003f
>>>>>>> [    0.263832] read32 0x00000000
>>>>>>> [    0.263838] read32 0x00000000
>>>>>>> [    0.263845] read32 0x00000000
>>>>>>> [    0.263852] read32 0x00000000
>>>>>>> [    0.263858] read32 0x00000000
>>>>>>> [    0.263865] read32 0x5243494d
>>>>>>> [    0.263872] read32 0x20204e4f
>>>>>>> [    0.263878] read32 0x20202020
>>>>>>> [    0.263885] read32 0x3932544d
>>>>>>> [    0.263891] read32 0x30473846
>>>>>>> [    0.263898] read32 0x41444138
>>>>>>> [    0.263905] read32 0x34484146
>>>>>>> [    0.263911] read32 0x20202020
>>>>>>> [    0.263918] read32 0x0000002c
.......
```

Correct Data

VBUSM2OCP Bridge for GPMC

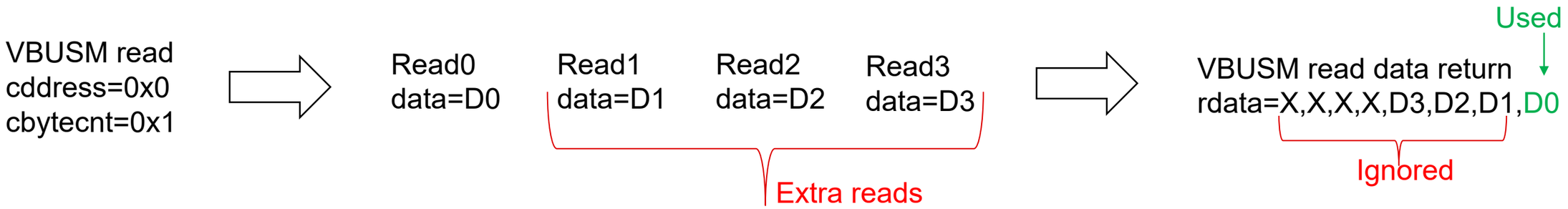
- Bridge translating sub-32-bit reads on VBUSM to 32-bit reads on OCP



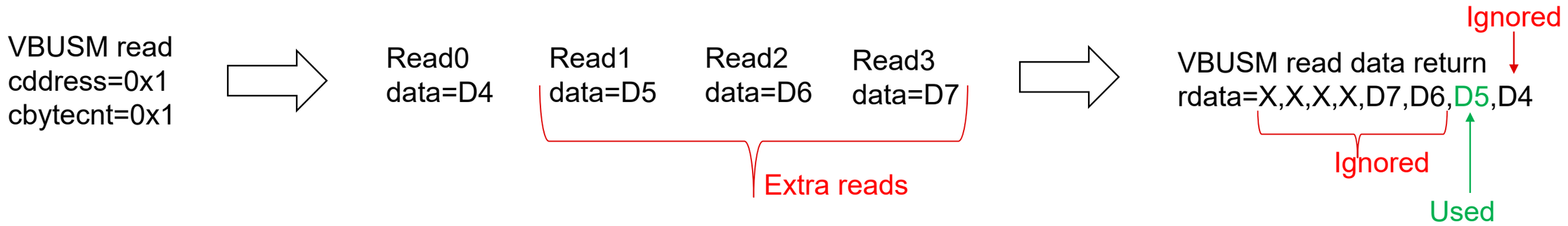
- No equivalent signal on VBUSM command to drive OCP MByteEn – need extra calculation
- Only D0 is used, all other data bytes are ignored at the VBUSM - no functional issue

What does this mean for NAND?

- NAND is accessed in 512 byte pages
- A single byte read will cause 4 reads on an 8-bit NAND device



- Internal NAND page counter increments by 4, any sequential byte read will read next data



What does it mean for other memories?

- Async/sync memories
  - No functional issue, but performance impact
    - Extra async accesses are performed on 8/16-bit external memory for sub-32-bit reads
    - For example, 4 async accesses are performed on an 8-bit external memory for a byte read

- FPGA/FIFO
  - GPMC is used to connect to FPGA in several systems
  - If an FPGA/FIFO is being read, data might be popped due to extra read accesses

Devices Impacted and Fix

- Devices impacted
  - AM64x_SR1.0, AM243x_SR1.0, AM263_SR1.x – Errata i2313
  - AM64x_SR2.0, AM243x_SR2.0 - Fixed

- Bridge fix
  - Fix has been identified and implemented
  - Involves addition of combinatorial gates
  - No addition of new flops

SW Workaround

- GPMC Legacy IP Behavior
  - OCP interface on the legacy GPMC IP only supports accesses with byte count equal to power-of-2 and starting address aligned to the requested byte count

- Potential SW workaround
  - Always use 32-bit or multiple of 32-bit reads to GPMC memory space when using NAND and/or FPGA FIFO implementation
  - Sub-32-bit reads (1 byte or 2 bytes) can be used for other async memories, but will have performance impact