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//

// i2c.h - Prototypes for the I2C Driver.

//

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//

// This is part of revision 2.1.3.156 of the Tiva Peripheral Driver Library.

//

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

**#ifndef** \_\_DRIVERLIB\_I2C\_H\_\_

**#define** \_\_DRIVERLIB\_I2C\_H\_\_

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//

// If building with a C++ compiler, make all of the definitions in this header

// have a C binding.

//

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

**#ifdef** \_\_cplusplus

**extern** "C"

{

**#endif**

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//

// Defines for the API.

//

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

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//

// Interrupt defines.

//

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

**#define** I2C\_INT\_MASTER 0x00000001

**#define** I2C\_INT\_SLAVE 0x00000002

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//

// I2C Master commands.

//

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

**#define** I2C\_MASTER\_CMD\_SINGLE\_SEND \

0x00000007

**#define** I2C\_MASTER\_CMD\_SINGLE\_RECEIVE \

0x00000007

**#define** I2C\_MASTER\_CMD\_BURST\_SEND\_START \

0x00000003

**#define** I2C\_MASTER\_CMD\_BURST\_SEND\_CONT \

0x00000001

**#define** I2C\_MASTER\_CMD\_BURST\_SEND\_FINISH \

0x00000005

**#define** I2C\_MASTER\_CMD\_BURST\_SEND\_STOP \

0x00000004

**#define** I2C\_MASTER\_CMD\_BURST\_SEND\_ERROR\_STOP \

0x00000004

**#define** I2C\_MASTER\_CMD\_BURST\_RECEIVE\_START \

0x0000000b

**#define** I2C\_MASTER\_CMD\_BURST\_RECEIVE\_CONT \

0x00000009

**#define** I2C\_MASTER\_CMD\_BURST\_RECEIVE\_FINISH \

0x00000005

**#define** I2C\_MASTER\_CMD\_BURST\_RECEIVE\_ERROR\_STOP \

0x00000004

**#define** I2C\_MASTER\_CMD\_QUICK\_COMMAND \

0x00000027

**#define** I2C\_MASTER\_CMD\_HS\_MASTER\_CODE\_SEND \

0x00000013

**#define** I2C\_MASTER\_CMD\_FIFO\_SINGLE\_SEND \

0x00000046

**#define** I2C\_MASTER\_CMD\_FIFO\_SINGLE\_RECEIVE \

0x00000046

**#define** I2C\_MASTER\_CMD\_FIFO\_BURST\_SEND\_START \

0x00000042

**#define** I2C\_MASTER\_CMD\_FIFO\_BURST\_SEND\_CONT \

0x00000040

**#define** I2C\_MASTER\_CMD\_FIFO\_BURST\_SEND\_FINISH \

0x00000044

**#define** I2C\_MASTER\_CMD\_FIFO\_BURST\_SEND\_ERROR\_STOP \

0x00000004

**#define** I2C\_MASTER\_CMD\_FIFO\_BURST\_RECEIVE\_START \

0x0000004a

**#define** I2C\_MASTER\_CMD\_FIFO\_BURST\_RECEIVE\_CONT \

0x00000048

**#define** I2C\_MASTER\_CMD\_FIFO\_BURST\_RECEIVE\_FINISH \

0x00000044

**#define** I2C\_MASTER\_CMD\_FIFO\_BURST\_RECEIVE\_ERROR\_STOP \

0x00000004

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//

// I2C Master glitch filter configuration.

//

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

**#define** I2C\_MASTER\_GLITCH\_FILTER\_DISABLED \

0

**#define** I2C\_MASTER\_GLITCH\_FILTER\_1 \

0x00010000

**#define** I2C\_MASTER\_GLITCH\_FILTER\_2 \

0x00020000

**#define** I2C\_MASTER\_GLITCH\_FILTER\_3 \

0x00030000

**#define** I2C\_MASTER\_GLITCH\_FILTER\_4 \

0x00040000

**#define** I2C\_MASTER\_GLITCH\_FILTER\_8 \

0x00050000

**#define** I2C\_MASTER\_GLITCH\_FILTER\_16 \

0x00060000

**#define** I2C\_MASTER\_GLITCH\_FILTER\_32 \

0x00070000

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//

// I2C Master error status.

//

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

**#define** I2C\_MASTER\_ERR\_NONE 0

**#define** I2C\_MASTER\_ERR\_ADDR\_ACK 0x00000004

**#define** I2C\_MASTER\_ERR\_DATA\_ACK 0x00000008

**#define** I2C\_MASTER\_ERR\_ARB\_LOST 0x00000010

**#define** I2C\_MASTER\_ERR\_CLK\_TOUT 0x00000080

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//

// I2C Slave action requests

//

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

**#define** I2C\_SLAVE\_ACT\_NONE 0

**#define** I2C\_SLAVE\_ACT\_RREQ 0x00000001 // Master has sent data

**#define** I2C\_SLAVE\_ACT\_TREQ 0x00000002 // Master has requested data

**#define** I2C\_SLAVE\_ACT\_RREQ\_FBR 0x00000005 // Master has sent first byte

**#define** I2C\_SLAVE\_ACT\_OWN2SEL 0x00000008 // Master requested secondary slave

**#define** I2C\_SLAVE\_ACT\_QCMD 0x00000010 // Master has sent a Quick Command

**#define** I2C\_SLAVE\_ACT\_QCMD\_DATA 0x00000020 // Master Quick Command value

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//

// Miscellaneous I2C driver definitions.

//

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

**#define** I2C\_MASTER\_MAX\_RETRIES 1000 // Number of retries

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//

// I2C Master interrupts.

//

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

**#define** I2C\_MASTER\_INT\_RX\_FIFO\_FULL \

0x00000800 // RX FIFO Full Interrupt

**#define** I2C\_MASTER\_INT\_TX\_FIFO\_EMPTY \

0x00000400 // TX FIFO Empty Interrupt

**#define** I2C\_MASTER\_INT\_RX\_FIFO\_REQ \

0x00000200 // RX FIFO Request Interrupt

**#define** I2C\_MASTER\_INT\_TX\_FIFO\_REQ \

0x00000100 // TX FIFO Request Interrupt

**#define** I2C\_MASTER\_INT\_ARB\_LOST \

0x00000080 // Arb Lost Interrupt

**#define** I2C\_MASTER\_INT\_STOP 0x00000040 // Stop Condition Interrupt

**#define** I2C\_MASTER\_INT\_START 0x00000020 // Start Condition Interrupt

**#define** I2C\_MASTER\_INT\_NACK 0x00000010 // Addr/Data NACK Interrupt

**#define** I2C\_MASTER\_INT\_TX\_DMA\_DONE \

0x00000008 // TX DMA Complete Interrupt

**#define** I2C\_MASTER\_INT\_RX\_DMA\_DONE \

0x00000004 // RX DMA Complete Interrupt

**#define** I2C\_MASTER\_INT\_TIMEOUT 0x00000002 // Clock Timeout Interrupt

**#define** I2C\_MASTER\_INT\_DATA 0x00000001 // Data Interrupt

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//

// I2C Slave interrupts.

//

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

**#define** I2C\_SLAVE\_INT\_RX\_FIFO\_FULL \

0x00000100 // RX FIFO Full Interrupt

**#define** I2C\_SLAVE\_INT\_TX\_FIFO\_EMPTY \

0x00000080 // TX FIFO Empty Interrupt

**#define** I2C\_SLAVE\_INT\_RX\_FIFO\_REQ \

0x00000040 // RX FIFO Request Interrupt

**#define** I2C\_SLAVE\_INT\_TX\_FIFO\_REQ \

0x00000020 // TX FIFO Request Interrupt

**#define** I2C\_SLAVE\_INT\_TX\_DMA\_DONE \

0x00000010 // TX DMA Complete Interrupt

**#define** I2C\_SLAVE\_INT\_RX\_DMA\_DONE \

0x00000008 // RX DMA Complete Interrupt

**#define** I2C\_SLAVE\_INT\_STOP 0x00000004 // Stop Condition Interrupt

**#define** I2C\_SLAVE\_INT\_START 0x00000002 // Start Condition Interrupt

**#define** I2C\_SLAVE\_INT\_DATA 0x00000001 // Data Interrupt

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//

// I2C Slave FIFO configuration macros.

//

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

**#define** I2C\_SLAVE\_TX\_FIFO\_ENABLE \

0x00000002

**#define** I2C\_SLAVE\_RX\_FIFO\_ENABLE \

0x00000004

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//

// I2C FIFO configuration macros.

//

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

**#define** I2C\_FIFO\_CFG\_TX\_MASTER 0x00000000

**#define** I2C\_FIFO\_CFG\_TX\_SLAVE 0x00008000

**#define** I2C\_FIFO\_CFG\_RX\_MASTER 0x00000000

**#define** I2C\_FIFO\_CFG\_RX\_SLAVE 0x80000000

**#define** I2C\_FIFO\_CFG\_TX\_MASTER\_DMA \

0x00002000

**#define** I2C\_FIFO\_CFG\_TX\_SLAVE\_DMA \

0x0000a000

**#define** I2C\_FIFO\_CFG\_RX\_MASTER\_DMA \

0x20000000

**#define** I2C\_FIFO\_CFG\_RX\_SLAVE\_DMA \

0xa0000000

**#define** I2C\_FIFO\_CFG\_TX\_NO\_TRIG 0x00000000

**#define** I2C\_FIFO\_CFG\_TX\_TRIG\_1 0x00000001

**#define** I2C\_FIFO\_CFG\_TX\_TRIG\_2 0x00000002

**#define** I2C\_FIFO\_CFG\_TX\_TRIG\_3 0x00000003

**#define** I2C\_FIFO\_CFG\_TX\_TRIG\_4 0x00000004

**#define** I2C\_FIFO\_CFG\_TX\_TRIG\_5 0x00000005

**#define** I2C\_FIFO\_CFG\_TX\_TRIG\_6 0x00000006

**#define** I2C\_FIFO\_CFG\_TX\_TRIG\_7 0x00000007

**#define** I2C\_FIFO\_CFG\_TX\_TRIG\_8 0x00000008

**#define** I2C\_FIFO\_CFG\_RX\_NO\_TRIG 0x00000000

**#define** I2C\_FIFO\_CFG\_RX\_TRIG\_1 0x00010000

**#define** I2C\_FIFO\_CFG\_RX\_TRIG\_2 0x00020000

**#define** I2C\_FIFO\_CFG\_RX\_TRIG\_3 0x00030000

**#define** I2C\_FIFO\_CFG\_RX\_TRIG\_4 0x00040000

**#define** I2C\_FIFO\_CFG\_RX\_TRIG\_5 0x00050000

**#define** I2C\_FIFO\_CFG\_RX\_TRIG\_6 0x00060000

**#define** I2C\_FIFO\_CFG\_RX\_TRIG\_7 0x00070000

**#define** I2C\_FIFO\_CFG\_RX\_TRIG\_8 0x00080000

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//

// I2C FIFO status.

//

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

**#define** I2C\_FIFO\_RX\_BELOW\_TRIG\_LEVEL \

0x00040000

**#define** I2C\_FIFO\_RX\_FULL 0x00020000

**#define** I2C\_FIFO\_RX\_EMPTY 0x00010000

**#define** I2C\_FIFO\_TX\_BELOW\_TRIG\_LEVEL \

0x00000004

**#define** I2C\_FIFO\_TX\_FULL 0x00000002

**#define** I2C\_FIFO\_TX\_EMPTY 0x00000001

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//

// Prototypes for the APIs.

//

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

**extern** **void** **I2CIntRegister**(uint32\_t ui32Base, **void**(\*pfnHandler)(**void**));

**extern** **void** **I2CIntUnregister**(uint32\_t ui32Base);

**extern** **void** **I2CTxFIFOConfigSet**(uint32\_t ui32Base, uint32\_t ui32Config);

**extern** **void** **I2CTxFIFOFlush**(uint32\_t ui32Base);

**extern** **void** **I2CRxFIFOConfigSet**(uint32\_t ui32Base, uint32\_t ui32Config);

**extern** **void** **I2CRxFIFOFlush**(uint32\_t ui32Base);

**extern** uint32\_t **I2CFIFOStatus**(uint32\_t ui32Base);

**extern** **void** **I2CFIFODataPut**(uint32\_t ui32Base, uint8\_t ui8Data);

**extern** uint32\_t **I2CFIFODataPutNonBlocking**(uint32\_t ui32Base,

uint8\_t ui8Data);

**extern** uint32\_t **I2CFIFODataGet**(uint32\_t ui32Base);

**extern** uint32\_t **I2CFIFODataGetNonBlocking**(uint32\_t ui32Base,

uint8\_t \*pui8Data);

**extern** **void** **I2CMasterBurstLengthSet**(uint32\_t ui32Base,

uint8\_t ui8Length);

**extern** uint32\_t **I2CMasterBurstCountGet**(uint32\_t ui32Base);

**extern** **void** **I2CMasterGlitchFilterConfigSet**(uint32\_t ui32Base,

uint32\_t ui32Config);

**extern** **void** **I2CSlaveFIFOEnable**(uint32\_t ui32Base, uint32\_t ui32Config);

**extern** **void** **I2CSlaveFIFODisable**(uint32\_t ui32Base);

**extern** **bool** **I2CMasterBusBusy**(uint32\_t ui32Base);

**extern** **bool** **I2CMasterBusy**(uint32\_t ui32Base);

**extern** **void** **I2CMasterControl**(uint32\_t ui32Base, uint32\_t ui32Cmd);

**extern** uint32\_t **I2CMasterDataGet**(uint32\_t ui32Base);

**extern** **void** **I2CMasterDataPut**(uint32\_t ui32Base, uint8\_t ui8Data);

**extern** **void** **I2CMasterDisable**(uint32\_t ui32Base);

**extern** **void** **I2CMasterEnable**(uint32\_t ui32Base);

**extern** uint32\_t **I2CMasterErr**(uint32\_t ui32Base);

**extern** **void** **I2CMasterInitExpClk**(uint32\_t ui32Base, uint32\_t ui32I2CClk,

**bool** bFast);

**extern** **void** **I2CMasterIntClear**(uint32\_t ui32Base);

**extern** **void** **I2CMasterIntDisable**(uint32\_t ui32Base);

**extern** **void** **I2CMasterIntEnable**(uint32\_t ui32Base);

**extern** **bool** **I2CMasterIntStatus**(uint32\_t ui32Base, **bool** bMasked);

**extern** **void** **I2CMasterIntEnableEx**(uint32\_t ui32Base,

uint32\_t ui32IntFlags);

**extern** **void** **I2CMasterIntDisableEx**(uint32\_t ui32Base,

uint32\_t ui32IntFlags);

**extern** uint32\_t **I2CMasterIntStatusEx**(uint32\_t ui32Base,

**bool** bMasked);

**extern** **void** **I2CMasterIntClearEx**(uint32\_t ui32Base,

uint32\_t ui32IntFlags);

**extern** **void** **I2CMasterTimeoutSet**(uint32\_t ui32Base, uint32\_t ui32Value);

**extern** **void** **I2CSlaveACKOverride**(uint32\_t ui32Base, **bool** bEnable);

**extern** **void** **I2CSlaveACKValueSet**(uint32\_t ui32Base, **bool** bACK);

**extern** uint32\_t **I2CMasterLineStateGet**(uint32\_t ui32Base);

**extern** **void** **I2CMasterSlaveAddrSet**(uint32\_t ui32Base,

uint8\_t ui8SlaveAddr,

**bool** bReceive);

**extern** uint32\_t **I2CSlaveDataGet**(uint32\_t ui32Base);

**extern** **void** **I2CSlaveDataPut**(uint32\_t ui32Base, uint8\_t ui8Data);

**extern** **void** **I2CSlaveDisable**(uint32\_t ui32Base);

**extern** **void** **I2CSlaveEnable**(uint32\_t ui32Base);

**extern** **void** **I2CSlaveInit**(uint32\_t ui32Base, uint8\_t ui8SlaveAddr);

**extern** **void** **I2CSlaveAddressSet**(uint32\_t ui32Base, uint8\_t ui8AddrNum,

uint8\_t ui8SlaveAddr);

**extern** **void** **I2CSlaveIntClear**(uint32\_t ui32Base);

**extern** **void** **I2CSlaveIntDisable**(uint32\_t ui32Base);

**extern** **void** **I2CSlaveIntEnable**(uint32\_t ui32Base);

**extern** **void** **I2CSlaveIntClearEx**(uint32\_t ui32Base, uint32\_t ui32IntFlags);

**extern** **void** **I2CSlaveIntDisableEx**(uint32\_t ui32Base,

uint32\_t ui32IntFlags);

**extern** **void** **I2CSlaveIntEnableEx**(uint32\_t ui32Base, uint32\_t ui32IntFlags);

**extern** **bool** **I2CSlaveIntStatus**(uint32\_t ui32Base, **bool** bMasked);

**extern** uint32\_t **I2CSlaveIntStatusEx**(uint32\_t ui32Base,

**bool** bMasked);

**extern** uint32\_t **I2CSlaveStatus**(uint32\_t ui32Base);

**extern** **void** **I2CLoopbackEnable**(uint32\_t ui32Base);

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//

// Mark the end of the C bindings section for C++ compilers.

//

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

**#ifdef** \_\_cplusplus

}

**#endif**

**#endif** // \_\_DRIVERLIB\_I2C\_H\_\_