TFP410 DEBUGGING STEPS

Q1. What happens if TFP410 is powered on and there is no output?

A1. Ensure that the monitor/Receiver is connected to the TFP410. Remember that DVI must be terminated through 50 ohms to 3.3V, since DVI is a current drive output. This termination is normally in the receiver chip. When measuring with load resistors, the termination voltage AVcc must be provided by an external supply.

The following figure shows the termination voltage for the load resistors like the DVI Spec. The effective measurement point shown for the output traces that follow is shown on the figure also.

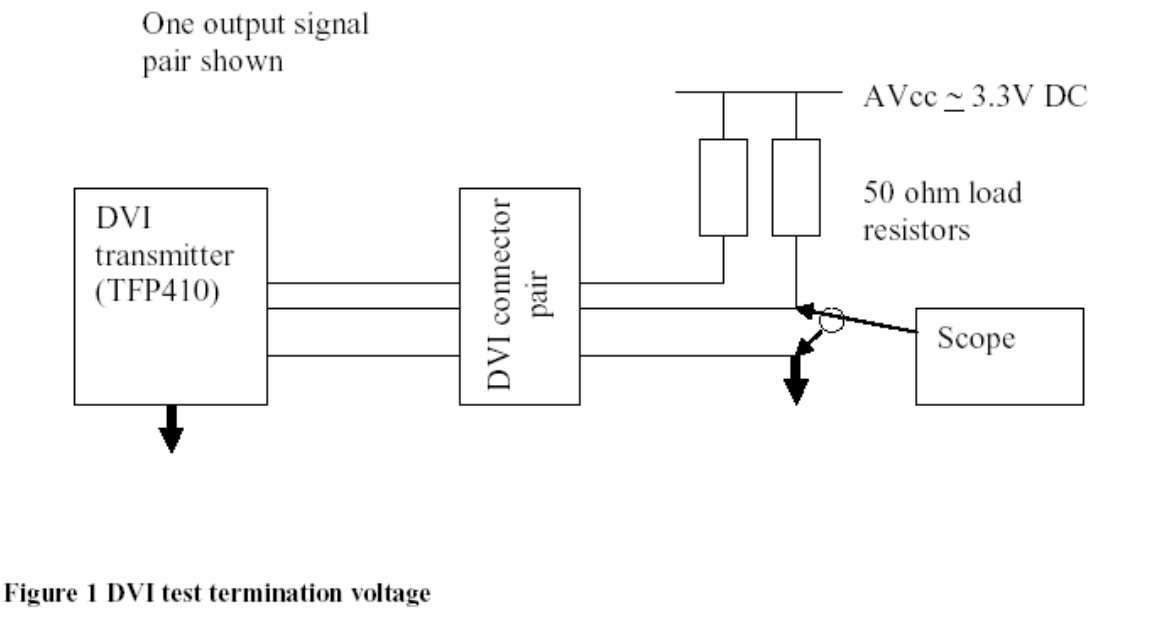

Figure 1 DVI test termination voltage

Q2. What happens if the TFP410 is powered on and the monitor is connected but there is no output?

A2 Power down (active low). In the power down state, only the digital I/O buffers and I2C interface remain active.

When I2C is disabled (ISEL = low), a high level selects the normal operating mode. A low level selects the power down mode.

When I2C is enabled (ISEL = high), the power-down state is selected through I2C. In this configuration, the PD pin should be tied to GND.

Note**:** The default register value for PD is low, so the device is in power down mode when I2C is first enabled or after an I2C RESET.

Q3. When the TFP410 is in the I2C mode, there is no output from the TFP410?

A3 The default register value for PD is low, so the device is in power down mode when I2C is first enabled or after an I2C RESET. Kindly write a value of 35 (or 37 depending

upon application) to register 8. This will make the TFP410 to go in normal operating mode.

Q4 How do I debug the signals/ Where should I start looking at to debug TFP410?
A4 With a differential probe (example: Tektronix P7330) and a high bandwidth oscilloscope (example Tektronix CSA7404), probe at the TMDS pairs out of the TFP410. First signal to look at can be the differential clock that is pin number 21 and 22. If the RTFADJ (resistor connected to pin 19 ~ = 510 ohms) then a ~1V differential peak to peak signal can be expected at the TMDS clock with a frequency same as the input clock that is pin 57.

Q5 What are the typical current readings when the TFP410 is in active mode?
A5 The current drawn by the TFP410 at UXGA resolution that is ~162MHz clock resolution is ~200mA. The current drawn depends on the resolution at which the TFP410 is operating.

Q6 Why is the amplitude of the DVI signals coming out of the TFP410 is very small?
A6. Ensure that the RTFADJ resistor connected to the TFADJ pin that is pin number 19 is ~510ohms. This is a Full-scale adjust pin. This pin controls the amplitude of the DVI output voltage swing, determined by the value of the pull-up resistor RTFADJ connected to TVDD.

Q7 What are the graphics controller interface formats that the TFP410 support?
A7. TFP410 supports 12 bit dual edge, 24 bit single edge input format. Kindly note that the TFP410 does not support 24bit Dual edge format. For more information kindly refer to page 11 of the TFP410 datasheet: Table 1. Universal Graphics Controller Interface Options.