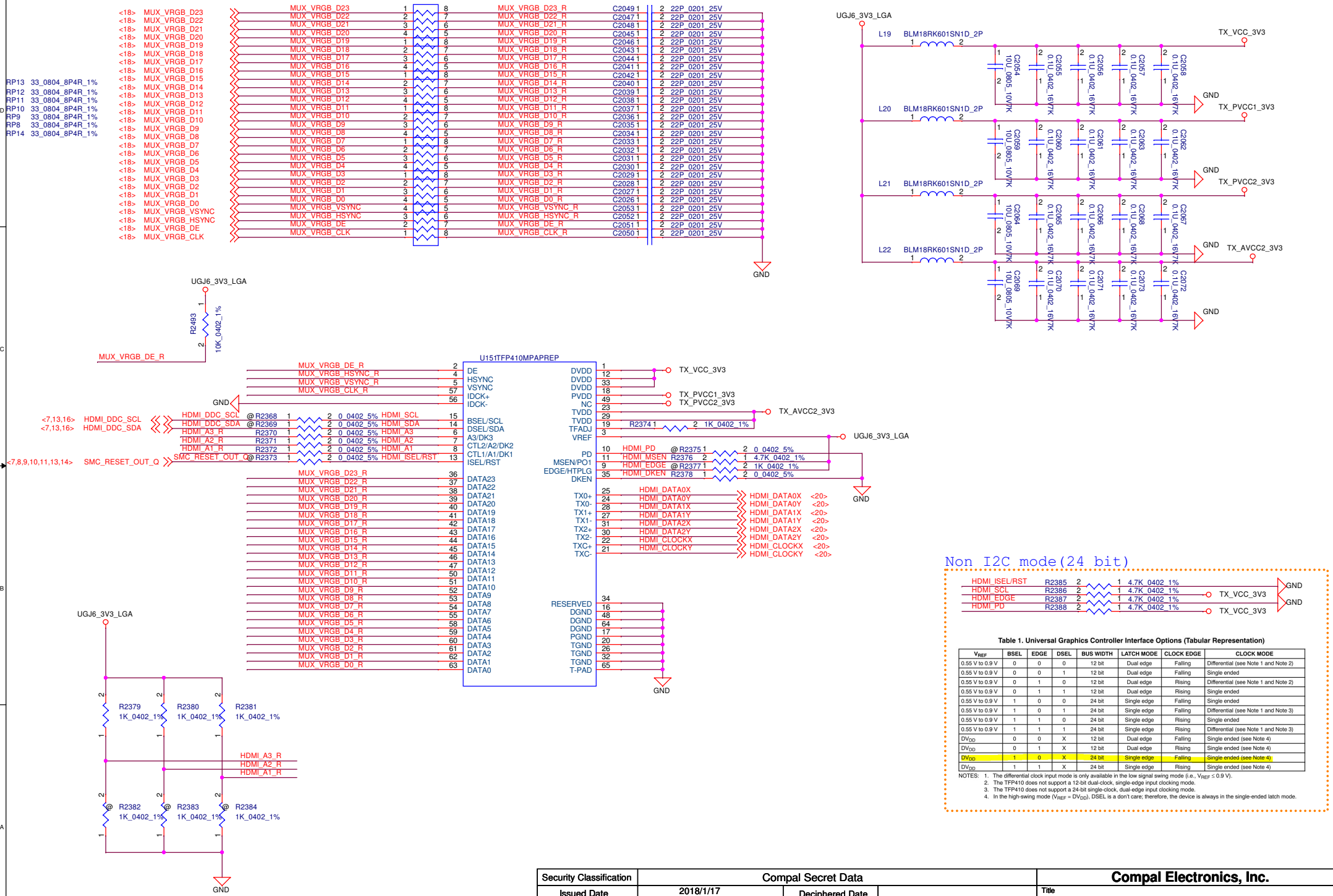

Table 1. Universal Graphics Controller Interface Options (Tabular Representation)

V_{REF}	BSEL	EDGE	DSEL	BUS WIDTH	LATCH MODE	CLOCK EDGE	CLOCK MODE
0.55 V to 0.9 V	0	0	0	12 bit	Dual edge	Falling	Differential (see Note 1 and Note 2)
0.55 V to 0.9 V	0	0	1	12 bit	Dual edge	Falling	Single ended
0.55 V to 0.9 V	0	1	0	12 bit	Dual edge	Rising	Differential (see Note 1 and Note 2)
0.55 V to 0.9 V	0	1	1	12 bit	Dual edge	Rising	Single ended
0.55 V to 0.9 V	1	0	0	24 bit	Single edge	Falling	Single ended
0.55 V to 0.9 V	1	0	1	24 bit	Single edge	Falling	Differential (see Note 1 and Note 3)
0.55 V to 0.9 V	1	1	0	24 bit	Single edge	Rising	Single ended
0.55 V to 0.9 V	1	1	1	24 bit	Single edge	Rising	Differential (see Note 1 and Note 3)
DV_{DD}	0	0	X	12 bit	Dual edge	Falling	Single ended (see Note 4)
DV_{DD}	0	1	X	12 bit	Dual edge	Rising	Single ended (see Note 4)
DV_{DD}	1	0	X	24 bit	Single edge	Falling	Single ended (see Note 4)
DV_{DD}	1	1	X	24 bit	Single edge	Rising	Single ended (see Note 4)

NOTES:
1. The differential clock input mode is only available in the low signal swing mode (i.e., $V_{REF} \leq 0.9$ V).
2. The TFP410 does not support a 12-bit dual-clock, single-edge input clocking mode.
3. The TFP410 does not support a 24-bit single-clock, dual-edge input clocking mode.
4. In the high-swing mode ($V_{REF} = DV_{DD}$), DSEL is a don't care; therefore, the device is always in the single-ended latch mode.

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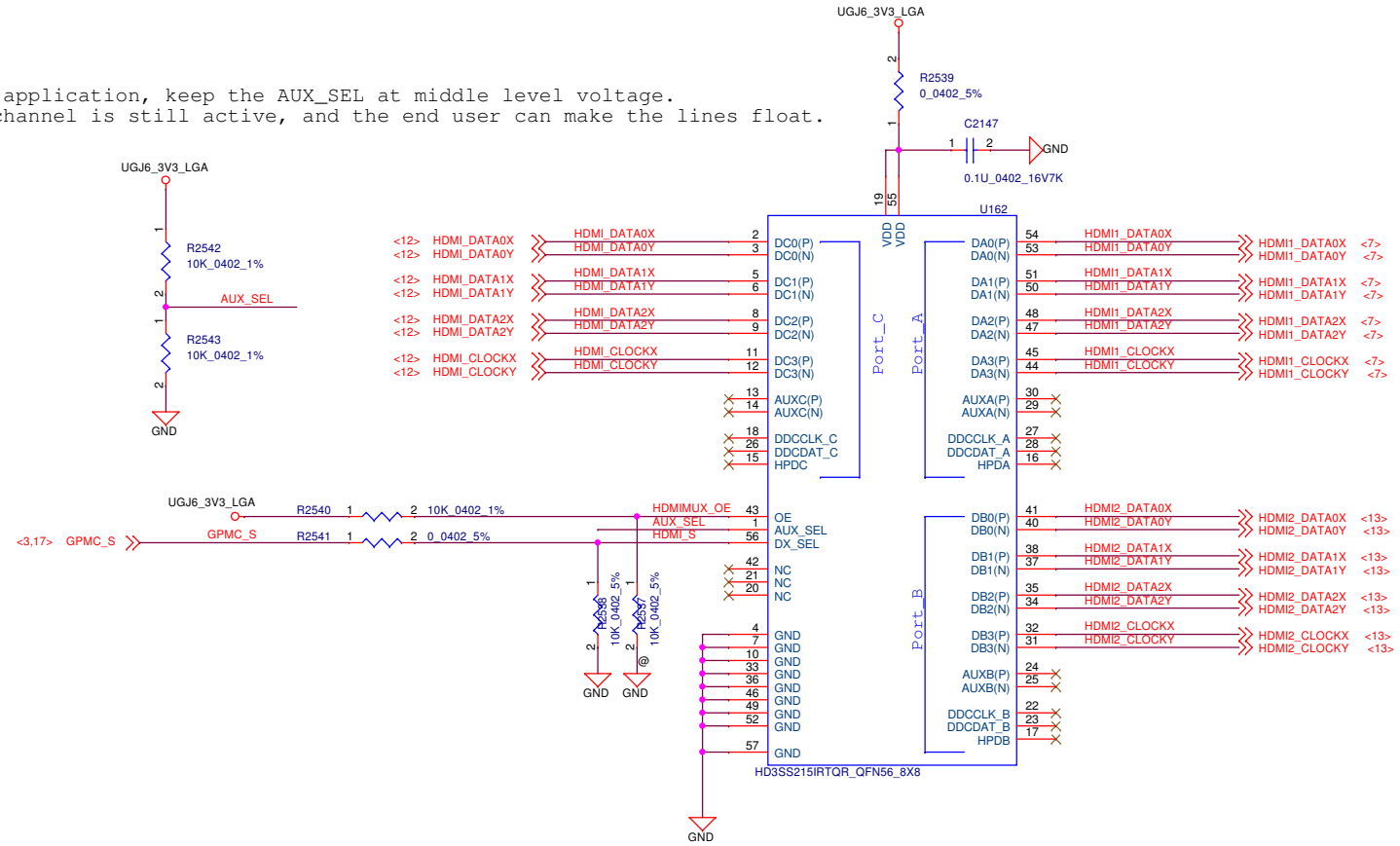
For HDMI application, keep the AUX_SEL at middle level voltage.
The AUX channel is still active, and the end user can make the lines float.



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