DSI Setup and Debugging Guide

Contents

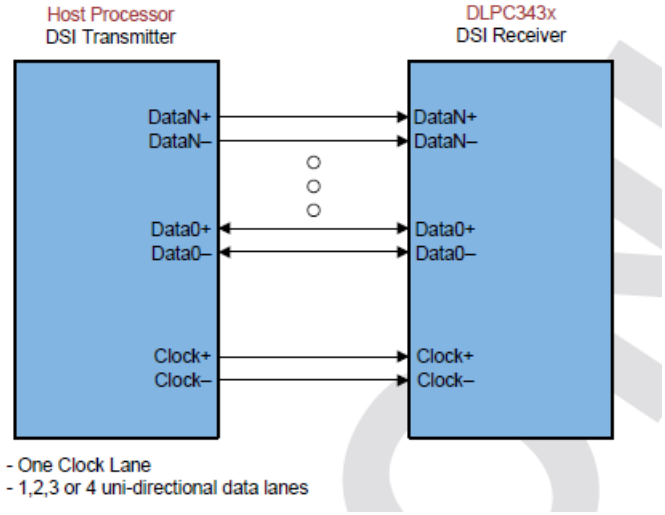
Note: The information in this document is not a substitute for the specifications listed in the corresponding device datasheets. In the event of a discrepancy, the datasheet supersedes this document.

DSI Overview

DSI (Display Serial Interface) is a source synchronous, high speed, low power, differential video interface. The DLPC3430 and DLPC3433 (both a part of the DLPC34xx family) support the DSI Type-3 LVDS video interface with up to 4-lanes. DSI is a useful alternative to a parallel interface if a reduction in data lanes is desired. This can be useful to save space in a PCB (printed circuit board) layout, or it can be useful if a desired front end processor has a reduced pin count that only supports DSI video.

The DLPC34xx DSI implementation supports the following features

- Implements DSI v1.02.00 (see exceptions in DSI Setup and DSI Timings)
- D-PHY standard MIPI specification version 1.0
- Display resolutions of 320x200 to 1280x1800
- Video mode support (no command mode support)
- Supports multiple packets per transmission
- Supports trigger messages in the forward direction
- One to four lanes of video support
- CRC (cyclic redundancy check) and ECC (error correction code) for header supported
- Checksum for long packets with error reporting (but no ECC)
- Supports burst mode, non-burst mode with sync pulses and with sync event

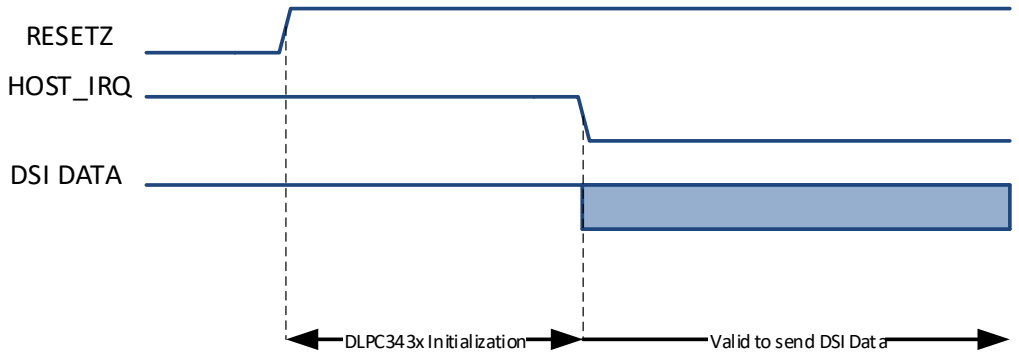


DLPC34xx Setup

- Set number of lanes DSI will use with GPIO_01 and GPIO_02. The GPIO pins are sampled during boot up and should be pulled-up or pulled-down appropriately
  - Note that these GPIO pins are used as part of SPI bus 1. The pull-up or pull-down resistors should be appropriately sized to not interfere with the SPI bus. The voltage is sampled during controller startup and is not sampled again during normal operation (thus one cannot dynamically change lanes)

GPIO_02	GPIO_01	Number of DSI Data Lanes
DSI-Lane-Config_1	DSI-Lane-Config_0	
0	0	1
0	1	2
1	0	3
1	1	4

- Startup the DLPC343x
- Execute the following commands. This can be done through an autoinit batch file but you can also directly send the I2C command
  - *Set DSI HS Clock input (0xBD):* Specify the high speed DSI clock
  - *Write Input Source Select (0x05)*: Set to external video
  - *Write External Video Source Format Select (0x07)*: Auto detect DSI format
  - Example batch file
    - # Write: DsiHsClockInput
      W 36 bd c8 00
      # Write: InputSourceSelect, 0 = External Video Port
      W 36 05 00
      # Write: ExternalVideoSourceFormat 0x00 = DSI Auto
      W 36 07 00
  - Send the DSI signal. It is important this signal is not sent before the DLPC343x is initialized (i.e. the DSI lines should remain idle until HOST_IRQ goes low). See the below diagram



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DSI Setup

- HS and LP Setup
    - Blanking Setup
        - HSync Blanking : Use HS Blanking
        - HBPorch Blanking: Use HS Blanking
        - HFPorch Blanking: Use HS Blanking
        - VSynce: Use LP11
        - Vertical Blanking: Use LP11
        - Turn clock off during LP Blanking: Disabled
    - Ensure low-power mode between pixels doesn't occur
- Command mode should not be enabled (i.e. MIPI Display Command Set[SM], DCS[SM], should not be used)
- EOT (End of Transfer) command must be enabled
- BTA (Bus Turn-Around) mode must be disabled
- The DSI HS signal should be ~200mV

DSI Timings

- Ensure THS_PREPARE + THS_ZERO add to at least 465ns if the clock is 95MHz to 235MHz and ensure they add to at least 565ns if the clock is 80MHz to 94MHz.
- In addition to all the general parallel interface requirements in the DLPC34xx datasheet and standard DSI specification requirements, the following requirements from the datasheet should be followed

6.15 DSI Host Timing Requirements

This section describes timing requirements for specific host minimum values that are higher than those specified in the MIPI standards. It is critical for proper operation that the host meet these minimum timing requirements for specified MIPI parameters.

			MIN	MAX	UNIT
Supported Frequency Lane	Clock Lane		80	235	MHz
	Data Lane	effective data rate	160	470	Mbps
	Number of Data Lanes	selectable	1	4	Lanes
$T_{HS-PREPARE}$+ $T_{HS-ZERO}$	During a LP to HS transition, the time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence	80 MHz to 94 MHz HS Clock	565		ns
		95 MHz to 235 MHz HS Clock(1)	465(2)		ns
$T_{HS-SETTLE}$	Time interval during which the HS reciever shall ignore any data lane HS transitions, starting from the beginning of $T_{HS-PREPARE}$. The HS receiver shall ignore any data lane transitions before the minimum value, and shall respond to any data lane transitions after the maximum value	80 MHz to 94 MHz HS Clock		565(3)	ns
		95 MHz to 235 MHz HS Clock		465(3)	ns

(1) Example: At 172 MHz and $T_{HS-PREPARE}$ = 51.46ns -> 51.46ns + $T_{HS-ZERO}$ >= 465ns. Therefore $T_{HS-ZERO}$ >= 413.54ns.
(2) Minimum values are higher than those required by the MIPI standard. $T_{HS-PREPARE}$ must be within the MIPI specified range.
(3) Maximum values are higher than those required by the MIPI standard.

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Other

- Ensure there are no DSI clock or data signals before the DLPC343x is initialized (i.e. these DSI lines should be idle). Only after the DLPC33x is initialized should these signals be sent
- The DSI lines are sensitive to temperature. High temperature may cause the image to freeze. Ensure there are no temperature gradients between the different DSI signals and ensure the PCB remains cool
- The propagation delay between the P and N signals should be matched within 8ps
- DSI signals are very sensitive to EMI (electromagnetic interference) which may cause the image to freeze or be lost. It is recommended to physically separate or shield the signals from known EMI sources
    - Note: It has been observed that using a heat gun to test a PCB under temperature produces enough EMI to cause DSI to fail. If testing a board under temperature it is important to use a heat source that doesn't produce excessive EMI

Qualcomm Specifics

- Set the DLPC343x clock rate to half of Qualcomm's clock frequency. Qualcomm and TI have different clock definitions. For example, if Qualcomm says 200MHz, the DLPC343x should be set to 100MHz
- Force DSI clock to HS mode in the Qualcomm processor (- qcom,mdss-dsi-force-clock-lane-hs: Boolean to force dsi clock lanes to HS mode always.)
- Enable End of Packet (EOT)
- Ensure proper lane state during LP blanking period (- qcom,mdss-dsi-bllp-eof-power-mode and - qcom,mdss-dsi-bllp-power-mode)
- There is a specific DSI Excel file the Qualcomm gives to their customers. Use this to verify timings will work with the Qualcomm processor.