

NOTES, UNLESS OTHERWISE SPECIFIED:

1. The netname "P1P1V" represents connection to the +1.1V FPGA power plane
2. The netname "P1P1V\_FIL" represents connection to the +1.1V filtered FPGA power plane
3. The netname "P1P1V\_M" represents connection to the +1.1V Primary Controller power plane
4. The netname "P1P1V\_S" represents connection to the +1.1V Secondary Controller power plane
5. The netname "P1P15V" represents connection to the +1.15V FPGA power plane
6. The netname "P1P15V\_FIL" represents connection to the +1.15V filtered FPGA power plane
7. The netname "P1P15V\_M" represents connection to the +1.15V Primary Controller power plane
8. The netname "P1P15V\_S" represents connection to the +1.15V Secondary Controller power plane
9. The netname "P1P8V\_M" represents connection to the +1.8V Primary Controller power plane
10. The netname "P1P8V\_S" represents connection to the +1.8V Secondary Controller power plane
11. The netname "A1P8V\_M" represents connection to the +1.8V Primary Controller power plane for the PLLs
12. The netname "A1P8V\_S" represents connection to the +1.8V Secondary Controller power plane for the PLLs
13. The netname "P2P5V" represents connection to the +2.5V FPGA power plane
14. The netname "P2P5V\_FIL" represents connection to the +2.5V filtered FPGA power plane
15. The netname "P2P5V\_M" represents connection to the +2.5V Primary Controller power plane
16. The netname "P2P5V\_S" represents connection to the +2.5V Secondary Controller power plane
17. The netname "P3P3V" represents connection to the +3.3V FPGA power plane
18. The netname "P3P3V\_M" represents connection to the +3.3V Primary Controller power plane
19. The netname "P3P3V\_S" represents connection to the +3.3V Secondary Controller power plane
20. The netname "P5V\_M" represents connection to the +5V Primary Controller power plane
21. The netname "P5V\_S" represents connection to the +5V Secondary Controller power plane
22. The netname "P12V" represents the connection to the +12.0V power plane.
23. The netname "GND" represents connection to the ground plane
24. A "Z" suffix on a signal name indicates an active low signal
25. All components with designators "U\*", "Q\*", "D\*" are electrostatic discharge sensitive.
26. All components with designators above 500 are mounted on the bottom side of the board.
27. All resistor values are in ohms.

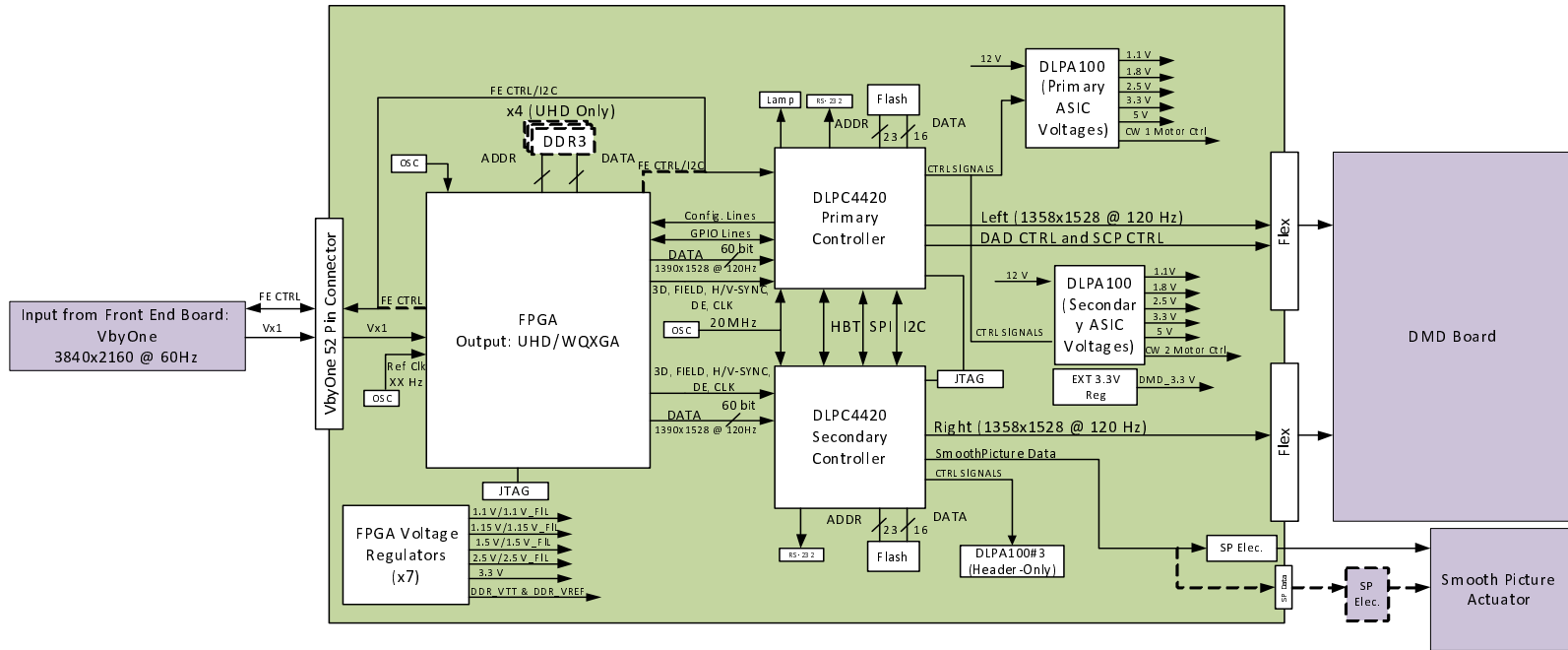


INDEX

- Sheet 1: Cover
- Sheet 2: Block Diagram
- Sheet 3: FPGA Front End I/F
- Sheet 4: FPGA DDR3 I/F
- Sheet 5: DDR3 Memory 1&2
- Sheet 6: DDR3 Memory 3&4
- Sheet 7: FPGA Video Out I/F
- Sheet 8: FPGA Programming/Test MUX
- Sheet 9: FPGA Power
- Sheet 10: FPGA Regulators
- Sheet 11: FPGA Regulators
- Sheet 12: FPGA Ground
- Sheet 13: ASIC Video Input I/F
- Sheet 14: Primary DMD Flex I/F
- Sheet 15: Secondary DMD Flex I/F
- Sheet 16: Input Power and PMD1000 I/F
- Sheet 17: Primary DLPAL100 Power Supplies
- Sheet 18: Secondary DLPAL100 Power Supplies
- Sheet 19: ColorWheel Drive
- Sheet 20: Fans, CW Index, Peripheral Connectors
- Sheet 21: Primary ASIC GPIO, I2C, and Lamp Ballast
- Sheet 22: GPIO Expander, Keypad Interface and IR
- Sheet 23: Primary ASIC TP, ARM JTAG, RESET
- Sheet 24: Secondary ASIC TP, ARM JTAG
- Sheet 25: Primary RS-232, SPI, and USB
- Sheet 26: Primary ASIC Flash I/F
- Sheet 27: Secondary ASIC Flash I/F
- Sheet 28: ASIC SSI I/F
- Sheet 29: SSI Driver I/F
- Sheet 30: Secondary ASIC GPIO & Smooth Picture I/F
- Sheet 31: Smooth Picture Electronics
- Sheet 32: Primary Power and Bypass Caps
- Sheet 33: Secondary Power and Bypass Caps
- Sheet 34: Output FMC Connector
- Sheet 35: Revision History
- Sheet 36: Important Notice

|             |         |      |               |      |           |   |                      |          |
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|             |         | ENGR |               |      |           |   |                      |          |
|             |         | SYST |               |      |           | TITLE<br><b>DLPC4420A Controller Board</b>  |                      |          |
|             |         | PRJ  |               |      |           |   |                      |          |
|             |         | QA   |               |      |           |   |                      |          |
| NEXT ASSY   | USED ON |      |               |      |           | <b>A3</b>   | DRAWING NO<br>DLP072 | REV<br>H |
| APPLICATION |         | SW   |               |      |           | SCALE   | SHEET 1 of 36        |          |

# Block Diagram



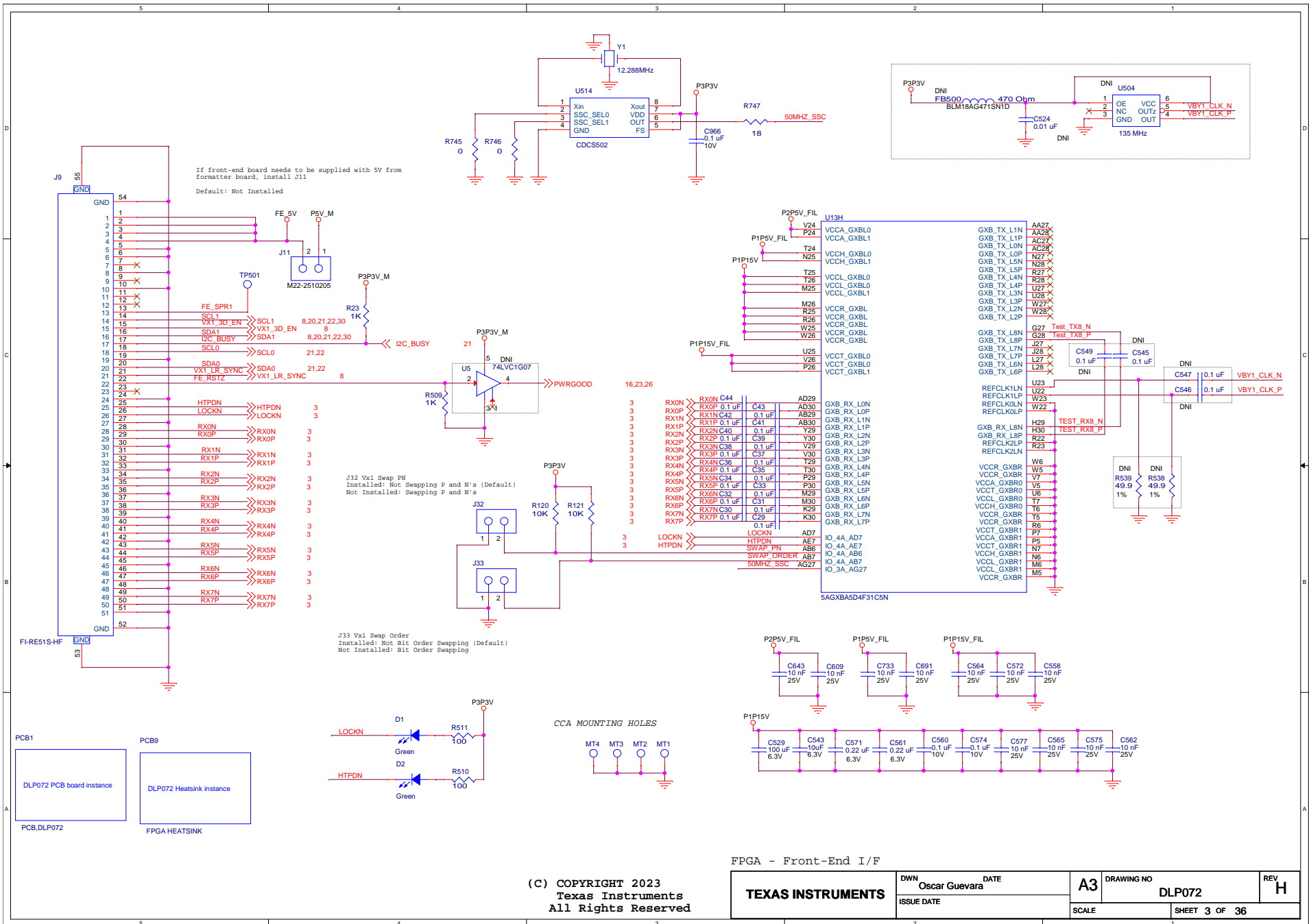
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SCALE SHEET 2 OF 36



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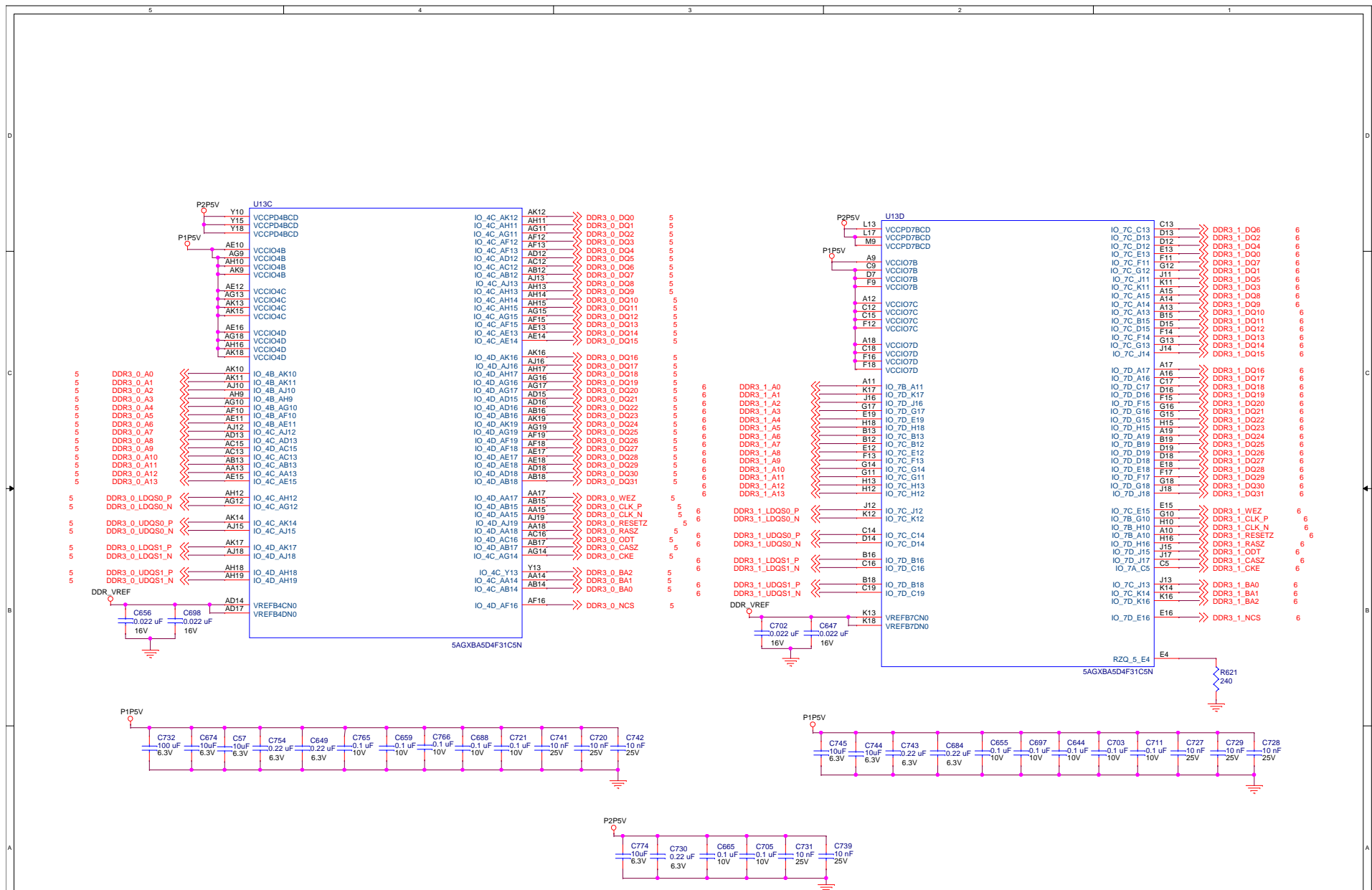
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DLP072

REV H

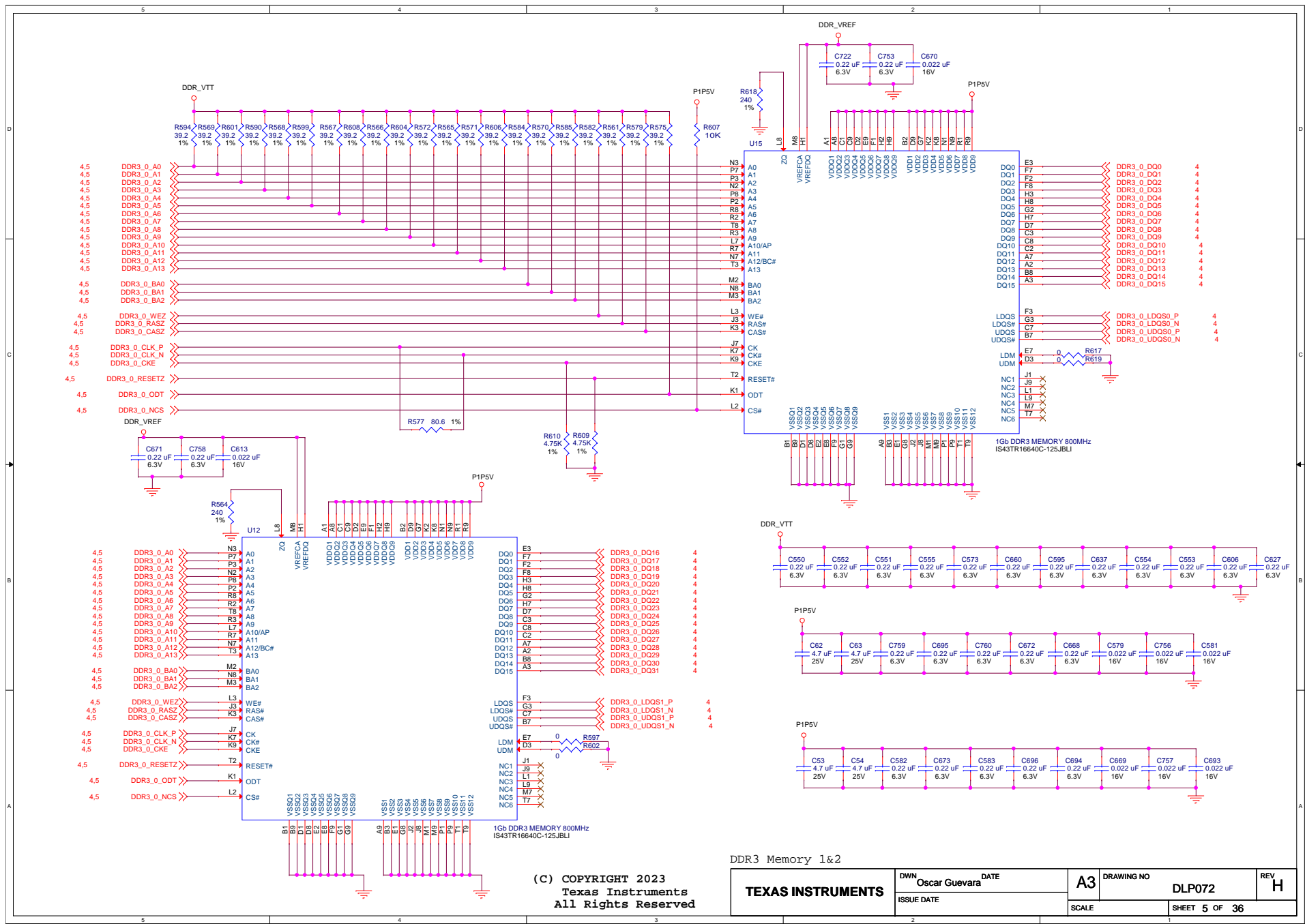
SCALE SHEET 3 OF 36



FPGA - DDR3 Interface

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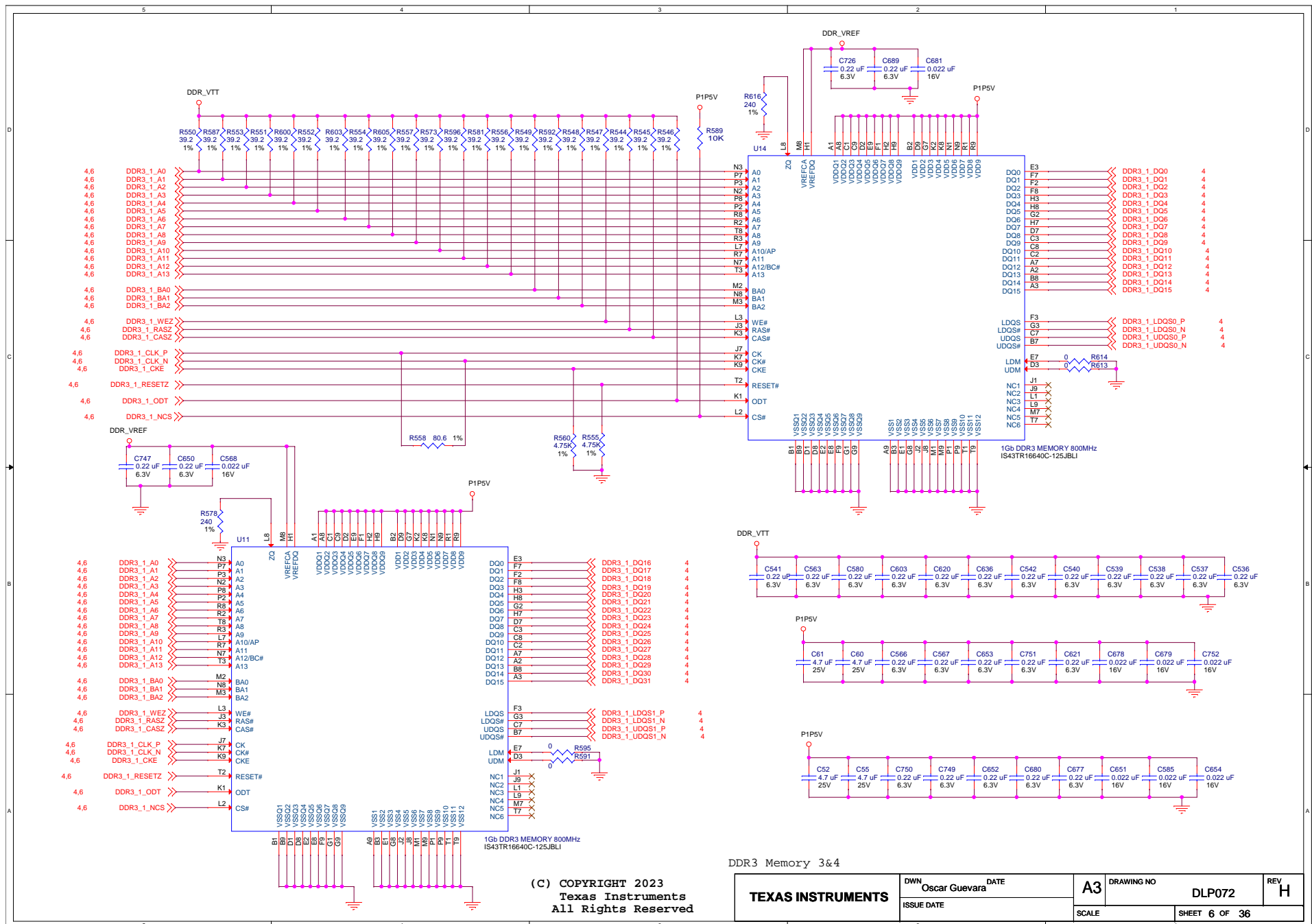
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|  | SCALE | DLP072        | H   |
|  |       | SHEET 4 OF 36 |     |



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DDR3 Memory 1&2

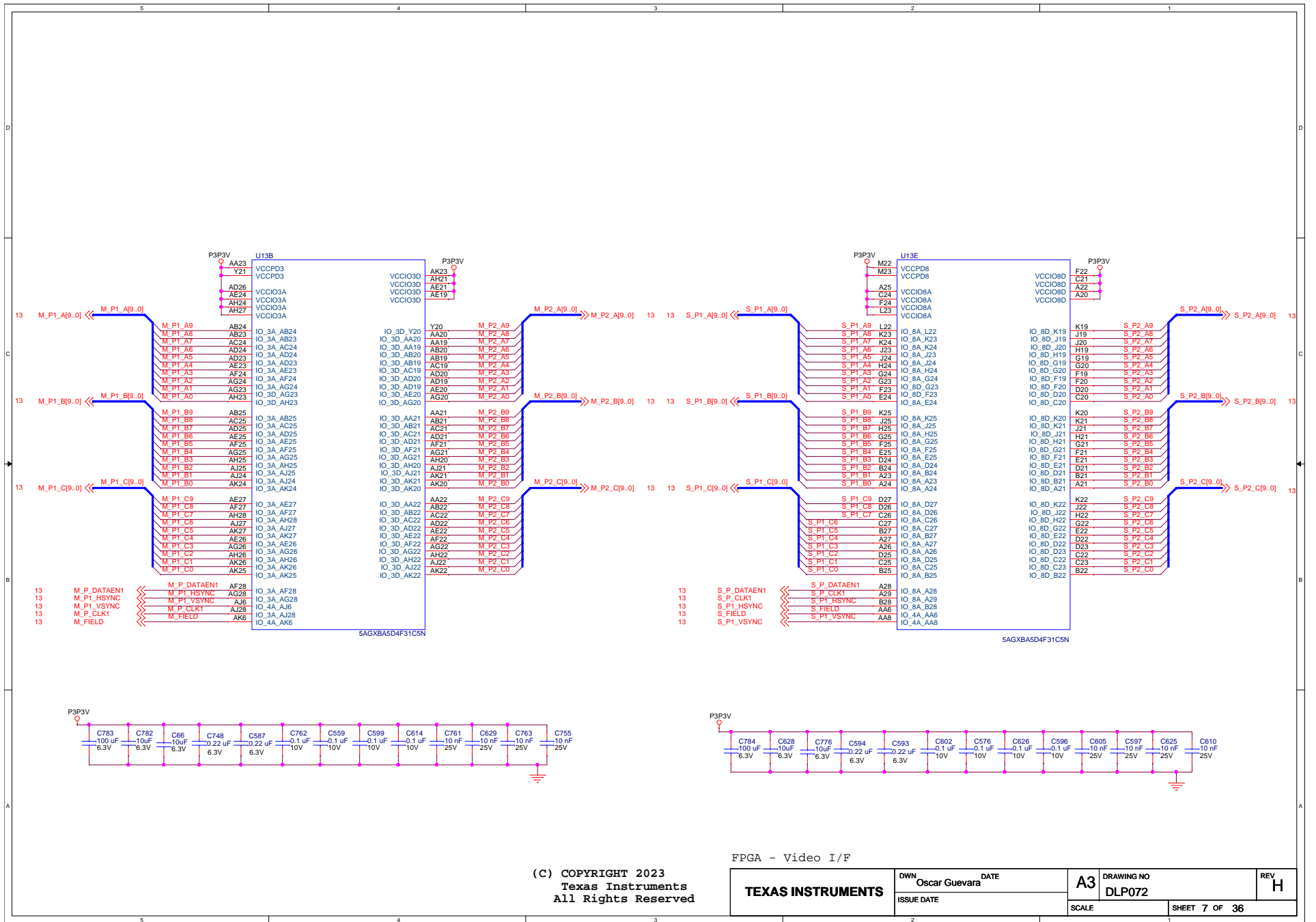
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|  | DATE |   |               |                 |



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DDR3 Memory 3&4

|   |               |                 |
|---|---------------|-----------------|
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|   | SCALE         | SHEET 6 OF 36   |



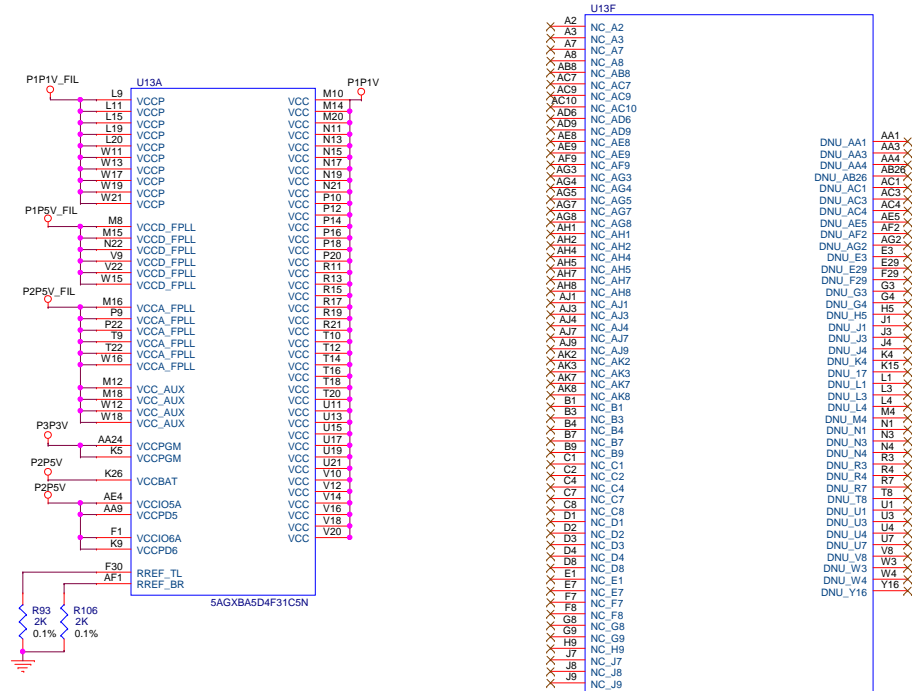
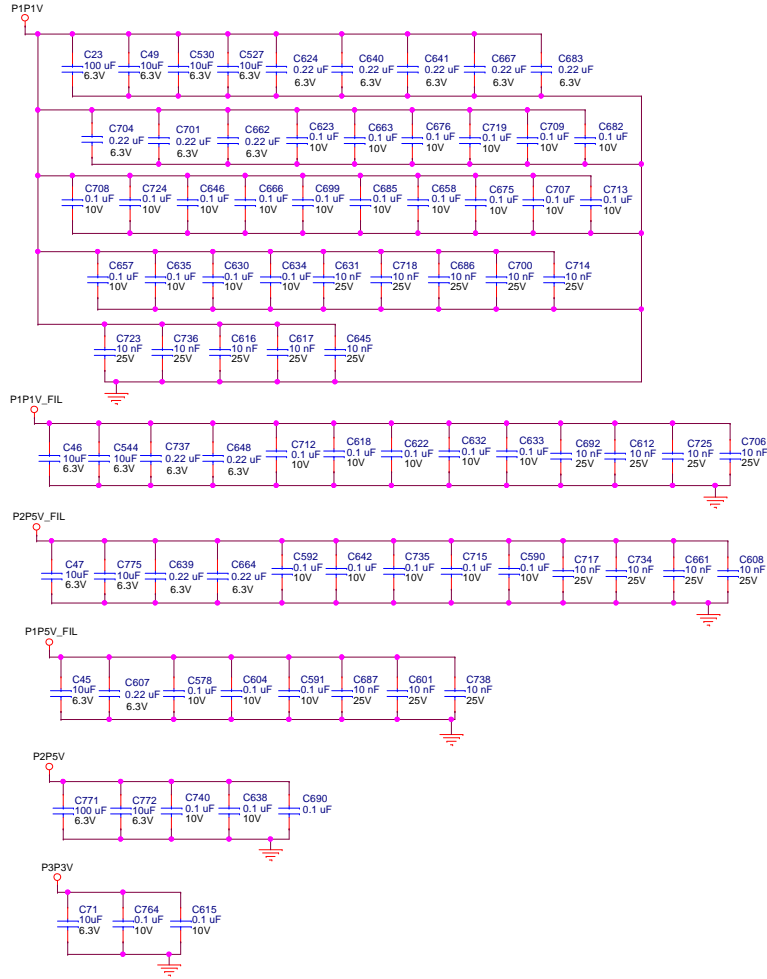
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FPGA - Video I/F

|  |       |                                |                 |
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|  | SCALE | SHEET 7 OF 36                  |                 |







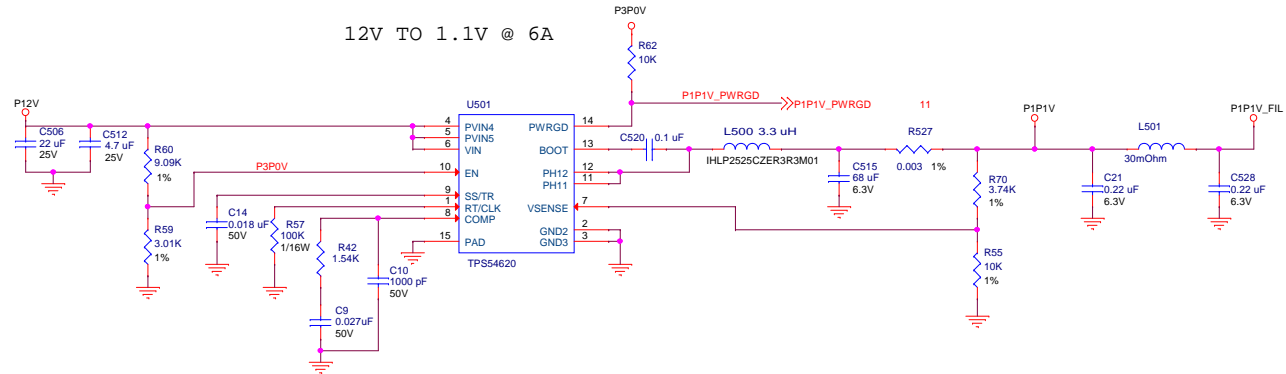
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FPGA - Power

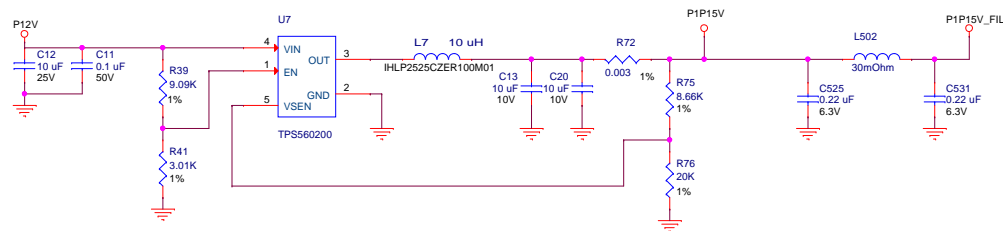
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|  | SCALE                     | DLP072               | SHEET 9 OF 36 |



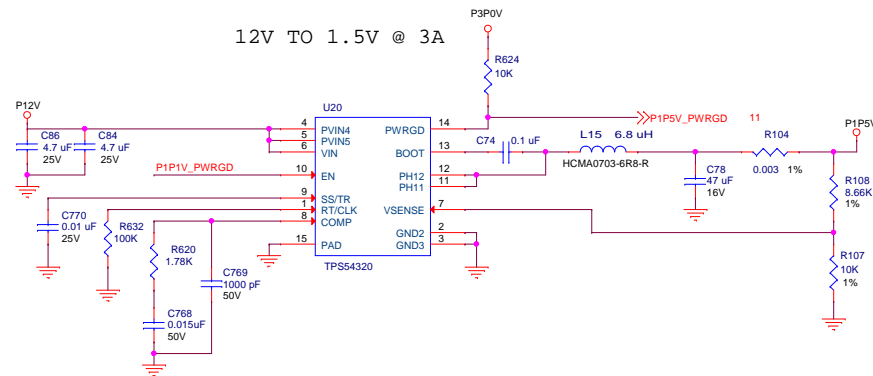
### 12V TO 1.1V @ 6A



### 12V TO 1.15V @ 500mA



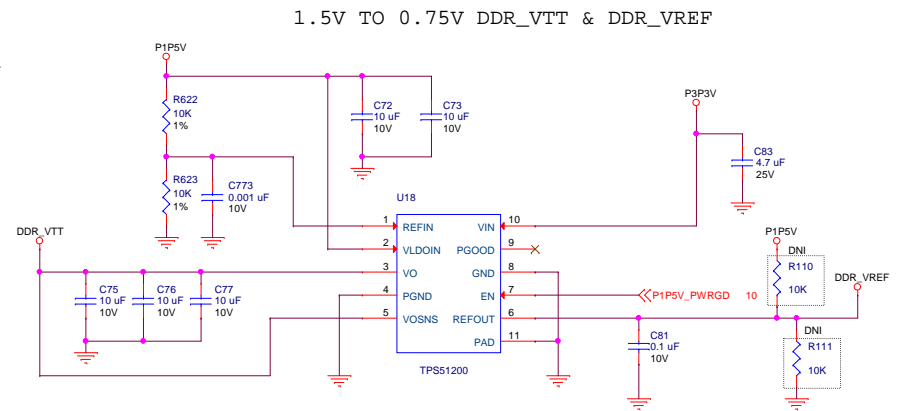
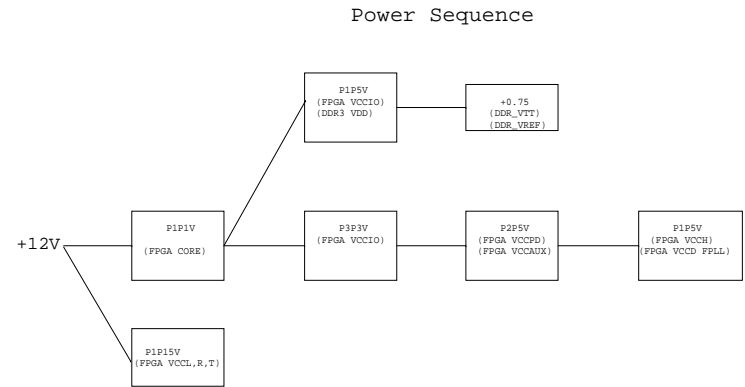
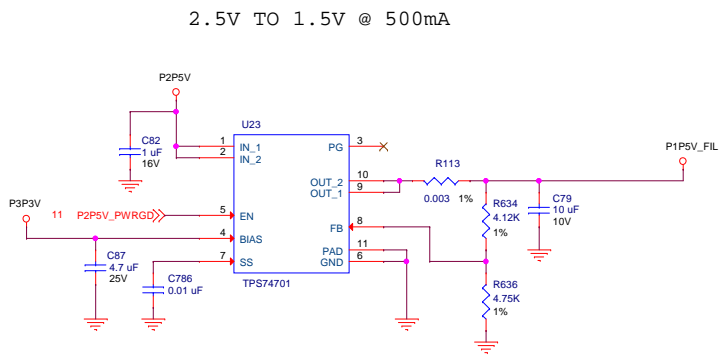
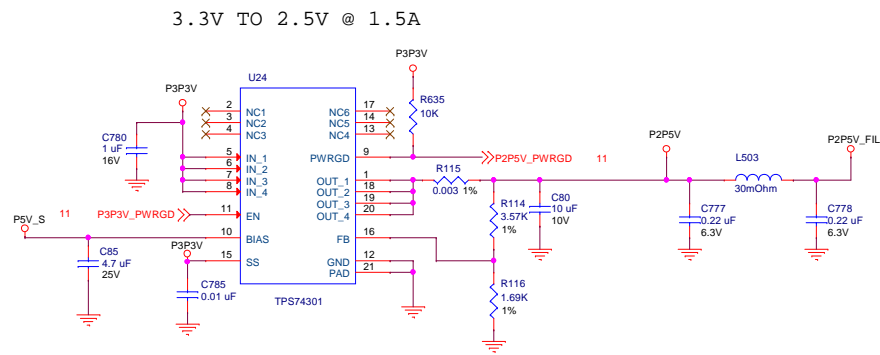
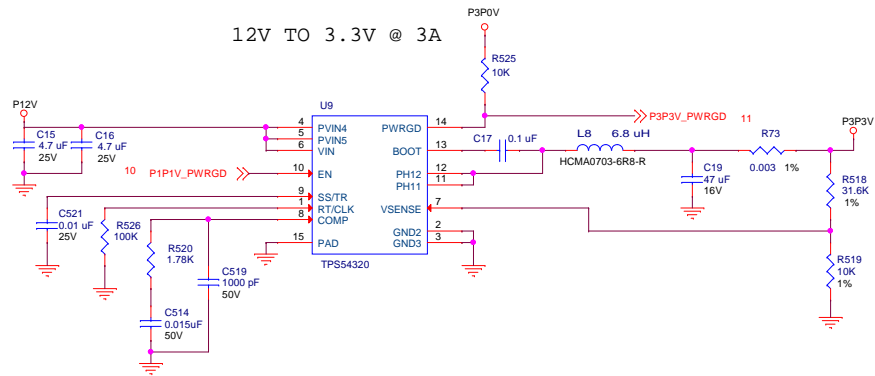
### 12V TO 1.5V @ 3A



FPGA - Regulators

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| SCALE             |                   |      | SHEET 10 OF 36 |            |     |



DDR TERMINATION VOLTAGE

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FPGA - Regulators

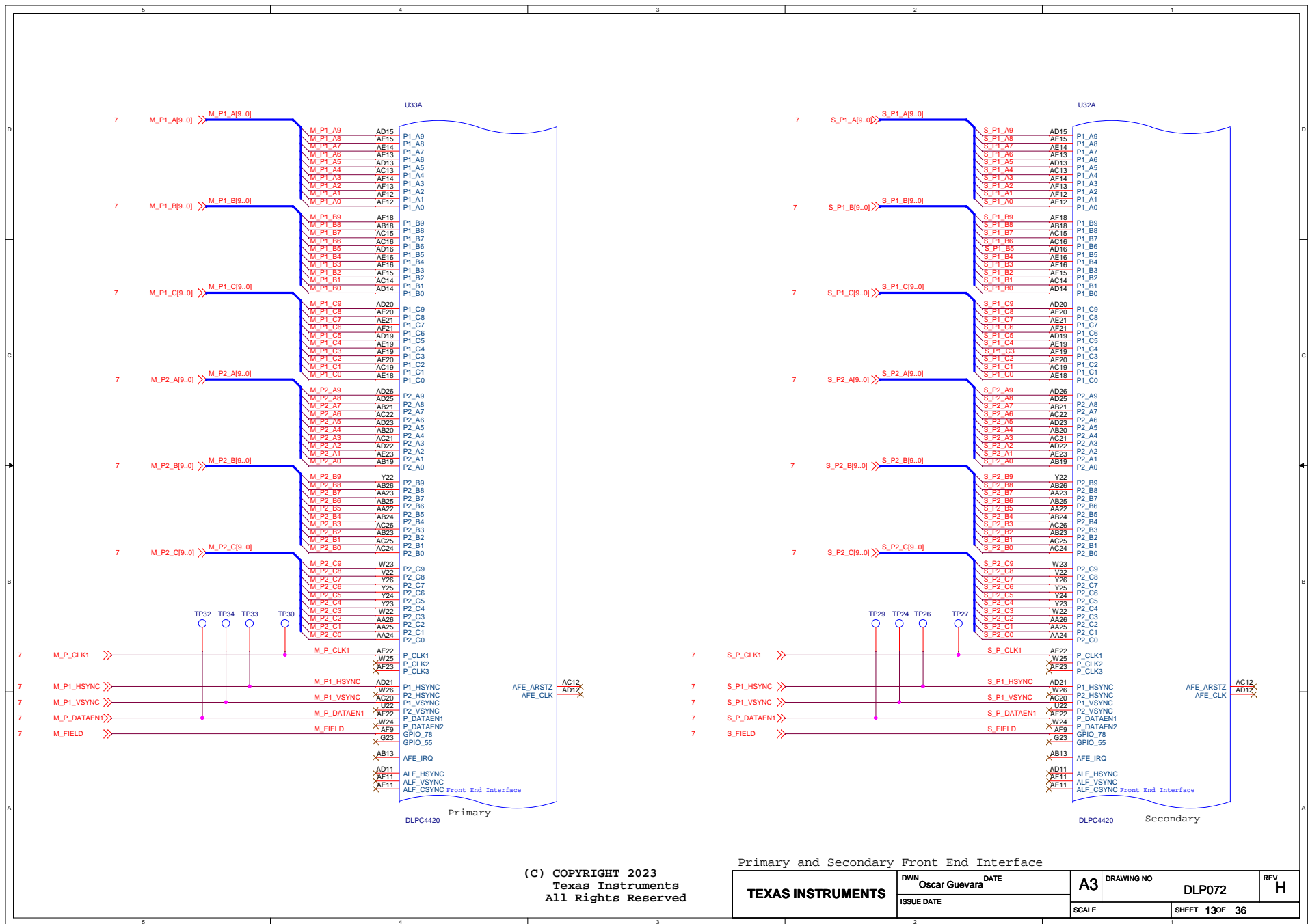
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|   | SCALE |                                | SHEET 110F 36   |



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FPGA - GND

|                          |                   |      |           |                             |                 |
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|                          | ISSUE DATE        |      |           |                             |                 |

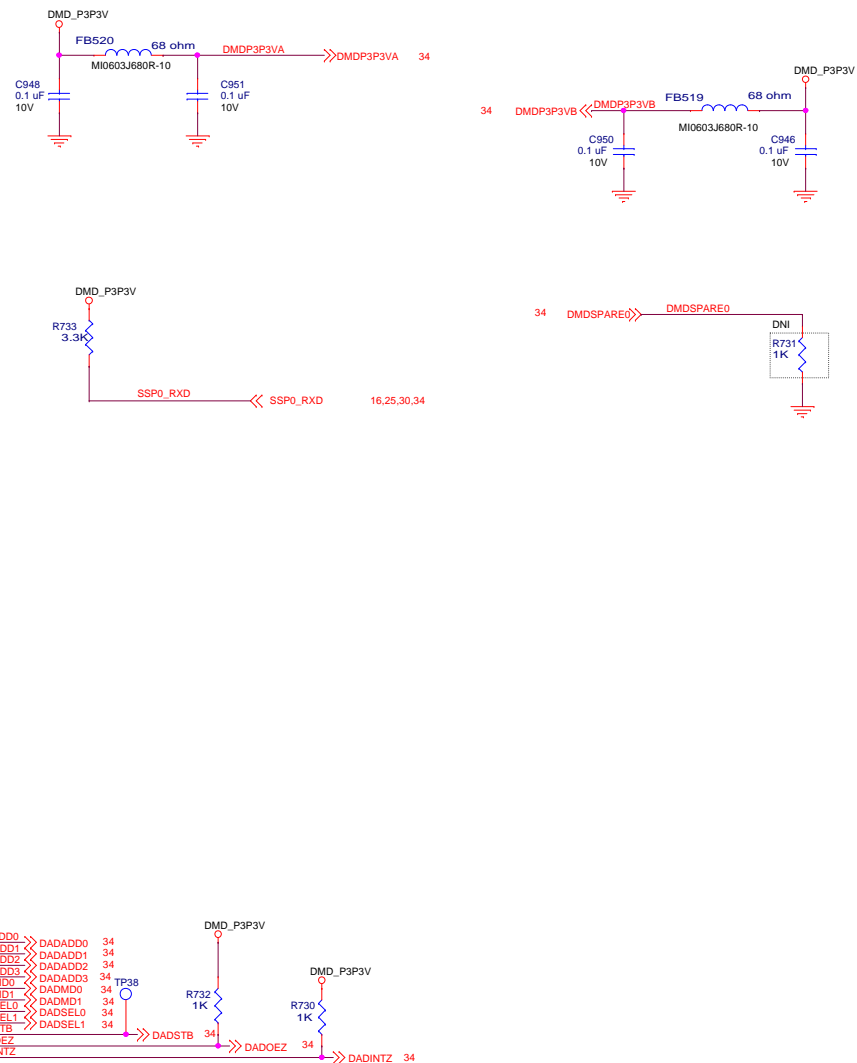
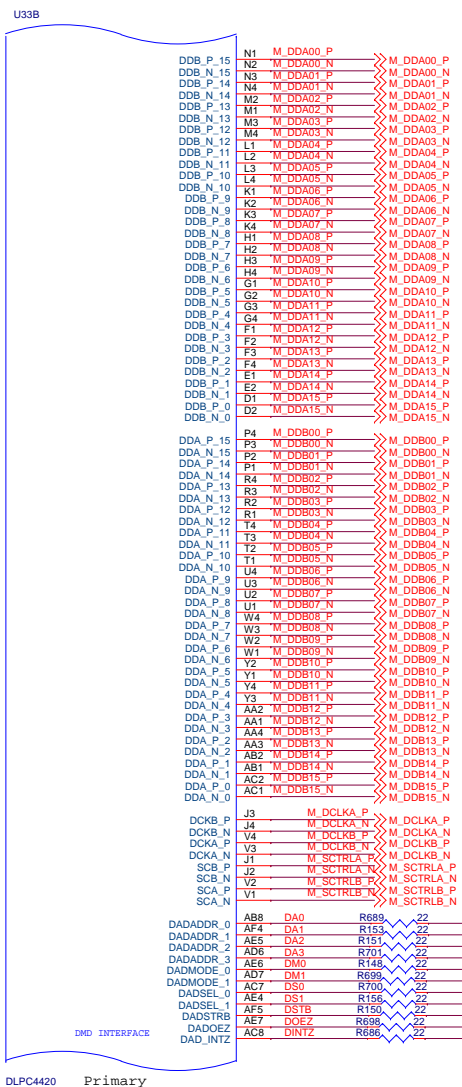


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Primary and Secondary Front End Interface

|   |       |                                       |                 |
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|   | SCALE |                                       | SHEET 13 OF 36  |

DMD Interface is BUS & BIT Swappable



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Primary Controller DMD Flex Interface

|                   |                   |      |       |            |        |     |   |
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|                   | ISSUE DATE        |      | SCALE | SHEET      | 140F   | 36  |   |

U32B

|           |     |            |     |            |    |
|-----------|-----|------------|-----|------------|----|
| DDB_P_15  | N1  | S_DDA00_P  | >>> | S_DDA00_P  | 34 |
| DDB_N_15  | N2  | S_DDA00_N  | >>> | S_DDA00_N  | 34 |
| DDB_P_14  | N3  | S_DDA01_P  | >>> | S_DDA01_P  | 34 |
| DDB_N_14  | N4  | S_DDA01_N  | >>> | S_DDA01_N  | 34 |
| DDB_P_13  | M1  | S_DDA02_N  | >>> | S_DDA02_P  | 34 |
| DDB_N_13  | M3  | S_DDA03_P  | >>> | S_DDA02_N  | 34 |
| DDB_P_12  | M4  | S_DDA03_N  | >>> | S_DDA03_P  | 34 |
| DDB_N_12  | L1  | S_DDA04_P  | >>> | S_DDA03_N  | 34 |
| DDB_P_11  | L2  | S_DDA04_N  | >>> | S_DDA04_P  | 34 |
| DDB_N_11  | L3  | S_DDA05_P  | >>> | S_DDA04_N  | 34 |
| DDB_P_10  | L4  | S_DDA05_N  | >>> | S_DDA05_P  | 34 |
| DDB_N_10  | K1  | S_DDA06_P  | >>> | S_DDA05_N  | 34 |
| DDB_P_9   | K2  | S_DDA06_N  | >>> | S_DDA06_P  | 34 |
| DDB_N_9   | K3  | S_DDA07_P  | >>> | S_DDA06_N  | 34 |
| DDB_P_8   | K4  | S_DDA07_N  | >>> | S_DDA07_P  | 34 |
| DDB_N_8   | H1  | S_DDA08_P  | >>> | S_DDA07_N  | 34 |
| DDB_P_7   | H2  | S_DDA08_N  | >>> | S_DDA08_P  | 34 |
| DDB_N_7   | H3  | S_DDA09_P  | >>> | S_DDA08_N  | 34 |
| DDB_P_6   | H4  | S_DDA09_N  | >>> | S_DDA09_P  | 34 |
| DDB_N_6   | G1  | S_DDA10_P  | >>> | S_DDA09_N  | 34 |
| DDB_P_5   | G2  | S_DDA10_N  | >>> | S_DDA10_P  | 34 |
| DDB_N_5   | G3  | S_DDA11_P  | >>> | S_DDA10_N  | 34 |
| DDB_P_4   | G4  | S_DDA11_N  | >>> | S_DDA11_P  | 34 |
| DDB_N_4   | F1  | S_DDA12_P  | >>> | S_DDA11_N  | 34 |
| DDB_P_3   | F2  | S_DDA12_N  | >>> | S_DDA12_P  | 34 |
| DDB_N_3   | F3  | S_DDA13_P  | >>> | S_DDA12_N  | 34 |
| DDB_P_2   | F4  | S_DDA13_N  | >>> | S_DDA13_P  | 34 |
| DDB_N_2   | E1  | S_DDA14_P  | >>> | S_DDA13_N  | 34 |
| DDB_P_1   | E2  | S_DDA14_N  | >>> | S_DDA14_P  | 34 |
| DDB_N_1   | D1  | S_DDA15_P  | >>> | S_DDA14_N  | 34 |
| DDB_P_0   | D2  | S_DDA15_N  | >>> | S_DDA15_P  | 34 |
| DDB_N_0   |     |            |     |            |    |
| DDA_P_15  | P4  | S_DDB00_P  | >>> | S_DDB00_P  | 34 |
| DDA_N_15  | P3  | S_DDB00_N  | >>> | S_DDB00_N  | 34 |
| DDA_P_14  | P1  | S_DDB01_P  | >>> | S_DDB01_P  | 34 |
| DDA_N_14  | R4  | S_DDB02_P  | >>> | S_DDB01_N  | 34 |
| DDA_P_13  | R3  | S_DDB02_N  | >>> | S_DDB02_P  | 34 |
| DDA_N_13  | R2  | S_DDB03_P  | >>> | S_DDB02_N  | 34 |
| DDA_P_12  | R1  | S_DDB03_N  | >>> | S_DDB03_P  | 34 |
| DDA_N_12  | T4  | S_DDB04_P  | >>> | S_DDB03_N  | 34 |
| DDA_P_11  | T3  | S_DDB04_N  | >>> | S_DDB04_P  | 34 |
| DDA_N_11  | T2  | S_DDB05_P  | >>> | S_DDB04_N  | 34 |
| DDA_P_10  | T1  | S_DDB05_N  | >>> | S_DDB05_P  | 34 |
| DDA_N_10  | U4  | S_DDB06_P  | >>> | S_DDB05_N  | 34 |
| DDA_P_9   | U3  | S_DDB06_N  | >>> | S_DDB06_P  | 34 |
| DDA_N_9   | U2  | S_DDB07_P  | >>> | S_DDB06_N  | 34 |
| DDA_P_8   | U1  | S_DDB07_N  | >>> | S_DDB07_P  | 34 |
| DDA_N_8   | W4  | S_DDB08_P  | >>> | S_DDB07_N  | 34 |
| DDA_P_7   | W3  | S_DDB08_N  | >>> | S_DDB08_P  | 34 |
| DDA_N_7   | W2  | S_DDB09_P  | >>> | S_DDB08_N  | 34 |
| DDA_P_6   | W1  | S_DDB09_N  | >>> | S_DDB09_P  | 34 |
| DDA_N_6   | Y2  | S_DDB10_P  | >>> | S_DDB09_N  | 34 |
| DDA_P_5   | Y1  | S_DDB10_N  | >>> | S_DDB10_P  | 34 |
| DDA_N_5   | Y4  | S_DDB11_P  | >>> | S_DDB10_N  | 34 |
| DDA_P_4   | Y3  | S_DDB11_N  | >>> | S_DDB11_P  | 34 |
| DDA_N_4   | AA2 | S_DDB12_P  | >>> | S_DDB11_N  | 34 |
| DDA_P_3   | AA1 | S_DDB12_N  | >>> | S_DDB12_P  | 34 |
| DDA_N_3   | AA4 | S_DDB13_P  | >>> | S_DDB12_N  | 34 |
| DDA_P_2   | AA3 | S_DDB13_N  | >>> | S_DDB13_P  | 34 |
| DDA_N_2   | AB2 | S_DDB14_P  | >>> | S_DDB13_N  | 34 |
| DDA_P_1   | AB1 | S_DDB14_N  | >>> | S_DDB14_P  | 34 |
| DDA_N_1   | AC2 | S_DDB15_P  | >>> | S_DDB14_N  | 34 |
| DDA_P_0   | AC1 | S_DDB15_N  | >>> | S_DDB15_P  | 34 |
| DDA_N_0   |     |            |     |            |    |
| DCKB_P    | J3  | S_DCLKA_P  | >>> | S_DCLKA_P  | 34 |
| DCKB_N    | J4  | S_DCLKA_N  | >>> | S_DCLKA_N  | 34 |
| DCKA_P    | V3  | S_DCLKB_N  | >>> | S_DCLKB_P  | 34 |
| DCKA_N    | J1  | S_SCTRLA_P | >>> | S_DCLKB_N  | 34 |
| SCB_P     | J2  | S_SCTRLA_N | >>> | S_SCTRLA_P | 34 |
| SCB_N     | V2  | S_SCTRLB_P | >>> | S_SCTRLA_N | 34 |
| SCA_P     | V1  | S_SCTRLB_N | >>> | S_SCTRLB_P | 34 |
| SCA_N     |     |            |     | S_SCTRLB_N | 34 |
| DADADDR_0 | AF4 | X          |     |            |    |
| DADADDR_1 | AE5 | X          |     |            |    |
| DADADDR_2 | AD6 | X          |     |            |    |
| DADADDR_3 | AE6 | X          |     |            |    |
| DADM0DE_0 | AD7 | X          |     |            |    |
| DADM0DE_1 | AC7 | X          |     |            |    |
| DADSEL_0  | AE4 | X          |     |            |    |
| DADSEL_1  | AE5 | X          |     |            |    |
| DADSTRB   | AE7 | X          |     |            |    |
| DAD0EZ    | AE8 | X          |     |            |    |
| DAD_INTZ  | AC8 | X          |     |            |    |

DMD INTERFACE

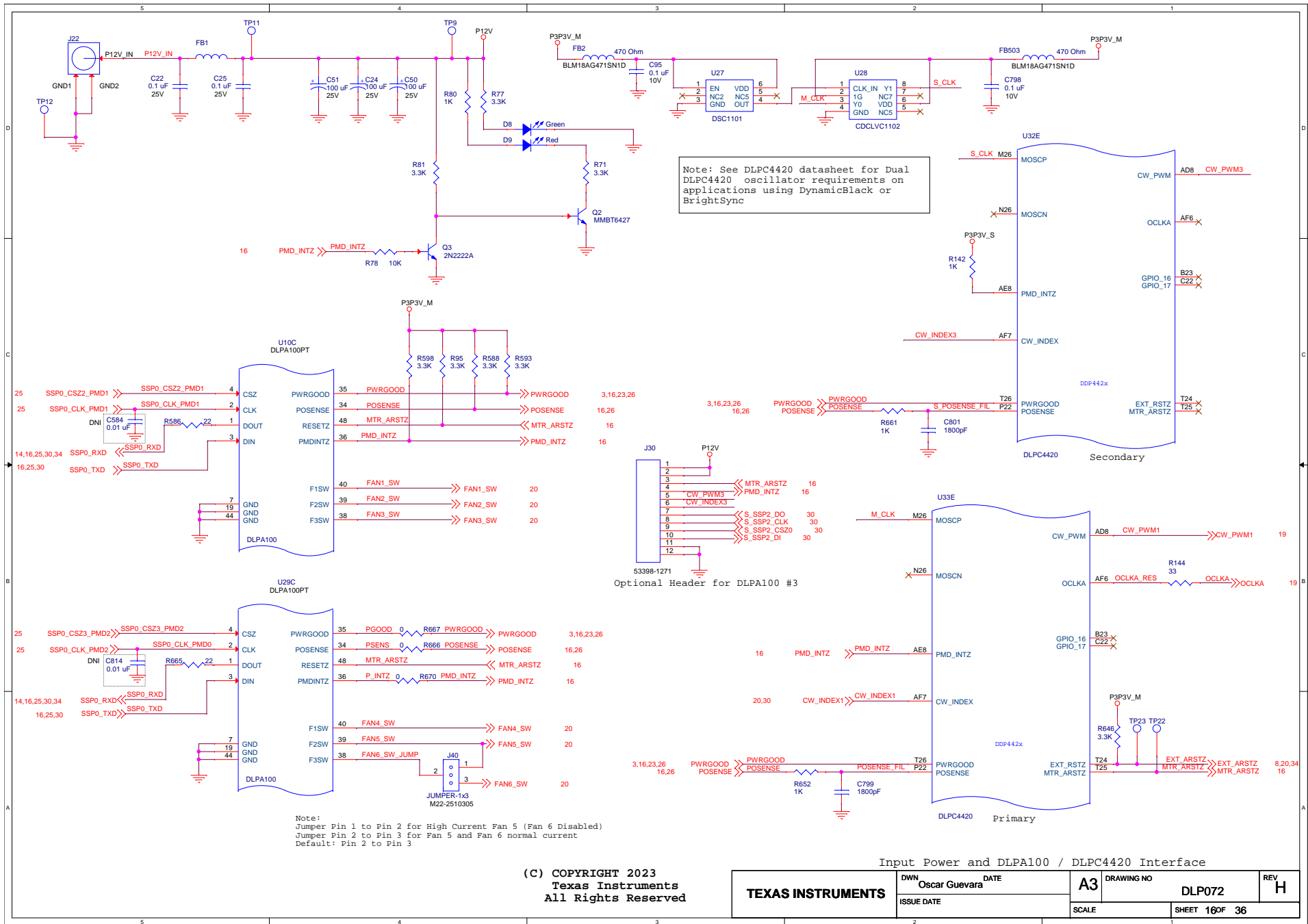
DLPC4420 Secondary



Secondary Controller DMD Flex Interface

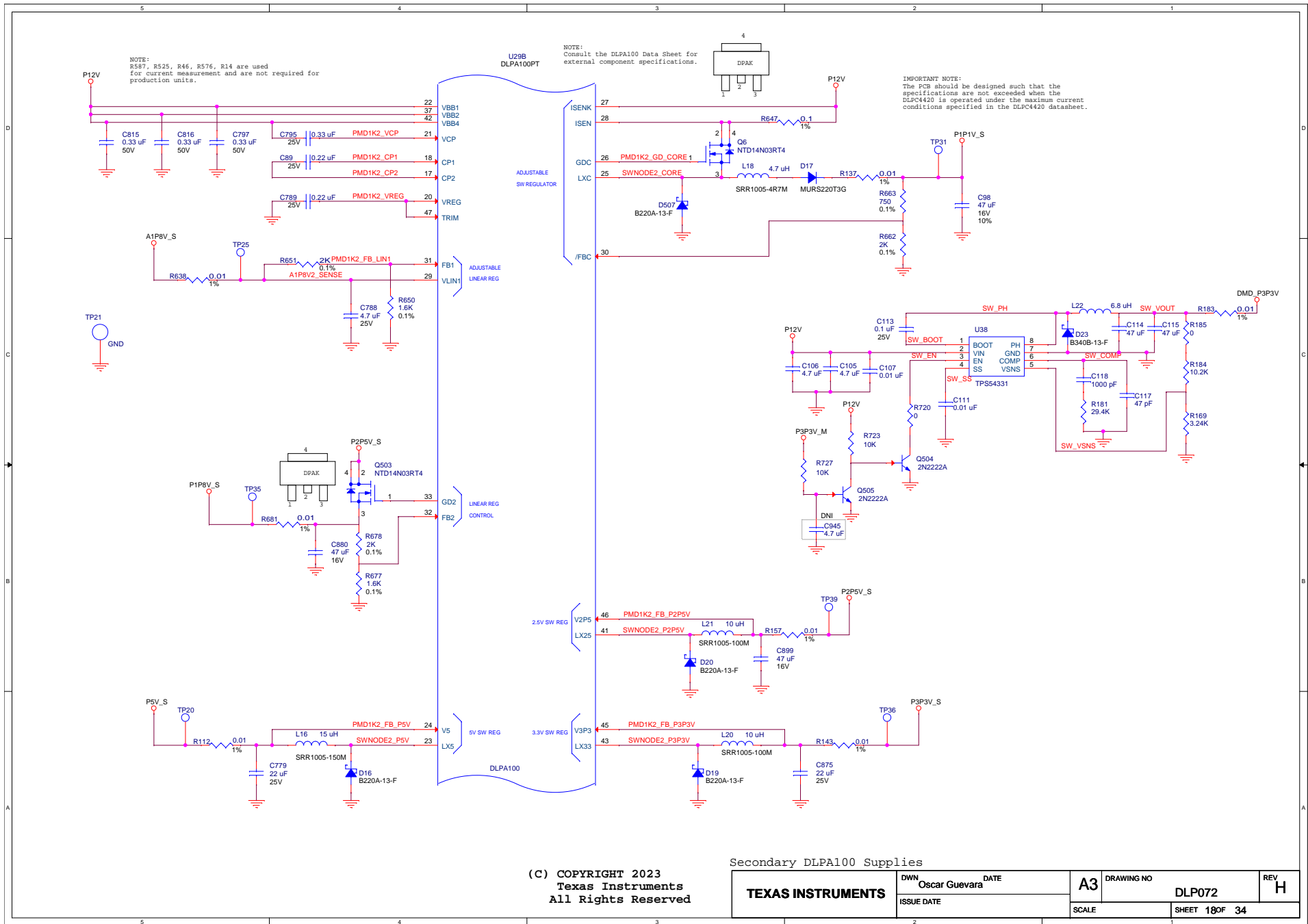
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|                   | ISSUE DATE        |      |               | DLP072     |       |
| SCALE             |                   |      | SHEET 15OF 36 |            |       |

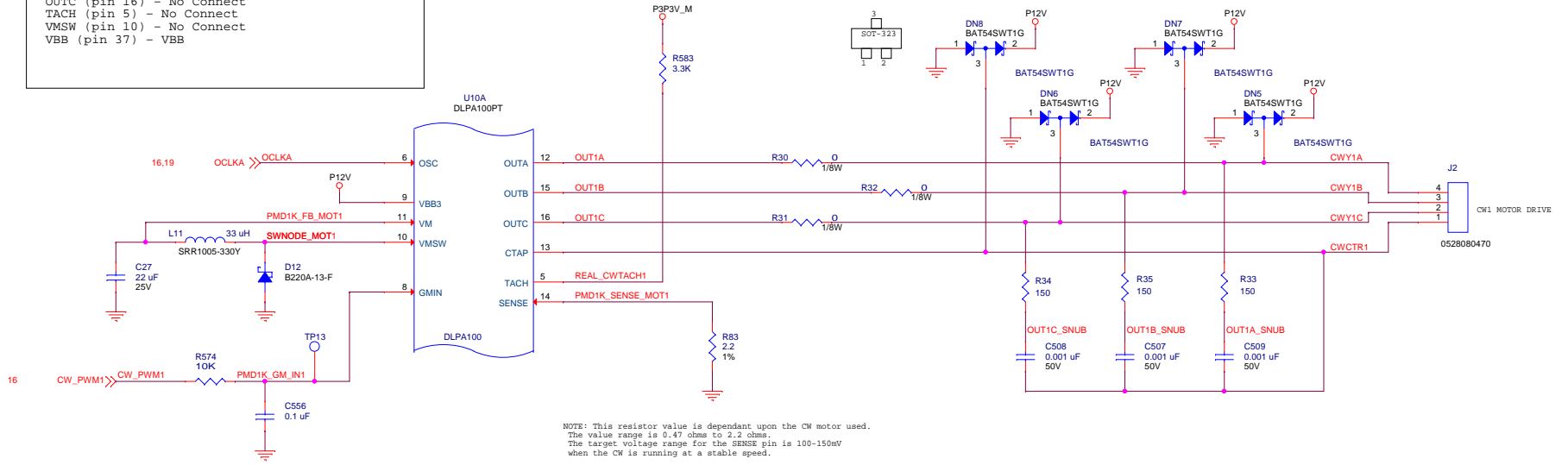




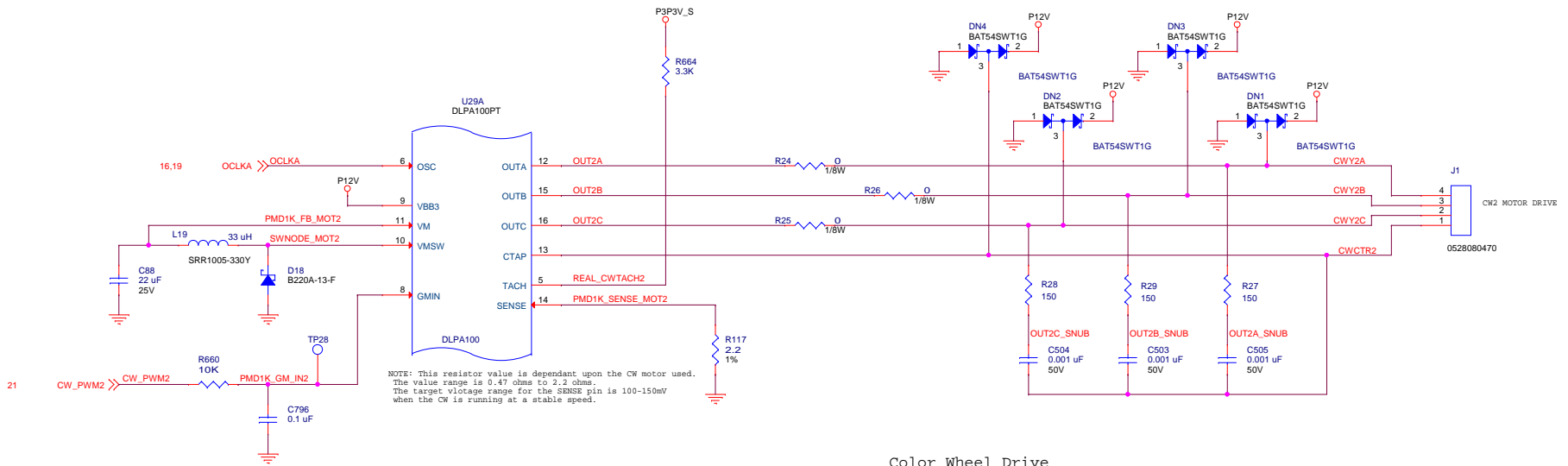




Note: If not using the motor driver on the DLPA100 follow these guidelines for unused pins:  
 GMIN (pin 8) - Ground  
 OSC (pin 6) - Ground  
 SENSE (pin 14) - Ground  
 CTAP (pin 13) - VBB  
 VM (pin 11) - VBB  
 OUTA (pin 12) - No Connect  
 OUTB (pin 15) - No Connect  
 OUTC (pin 16) - No Connect  
 TACH (pin 5) - No Connect  
 VMSW (pin 10) - No Connect  
 VBB (pin 37) - VBB



NOTE: This resistor value is dependant upon the CW motor used.  
 The value range is 0.47 ohms to 2.2 ohms.  
 The target voltage range for the SENSE pin is 100-150mV  
 when the CW is running at a stable speed.

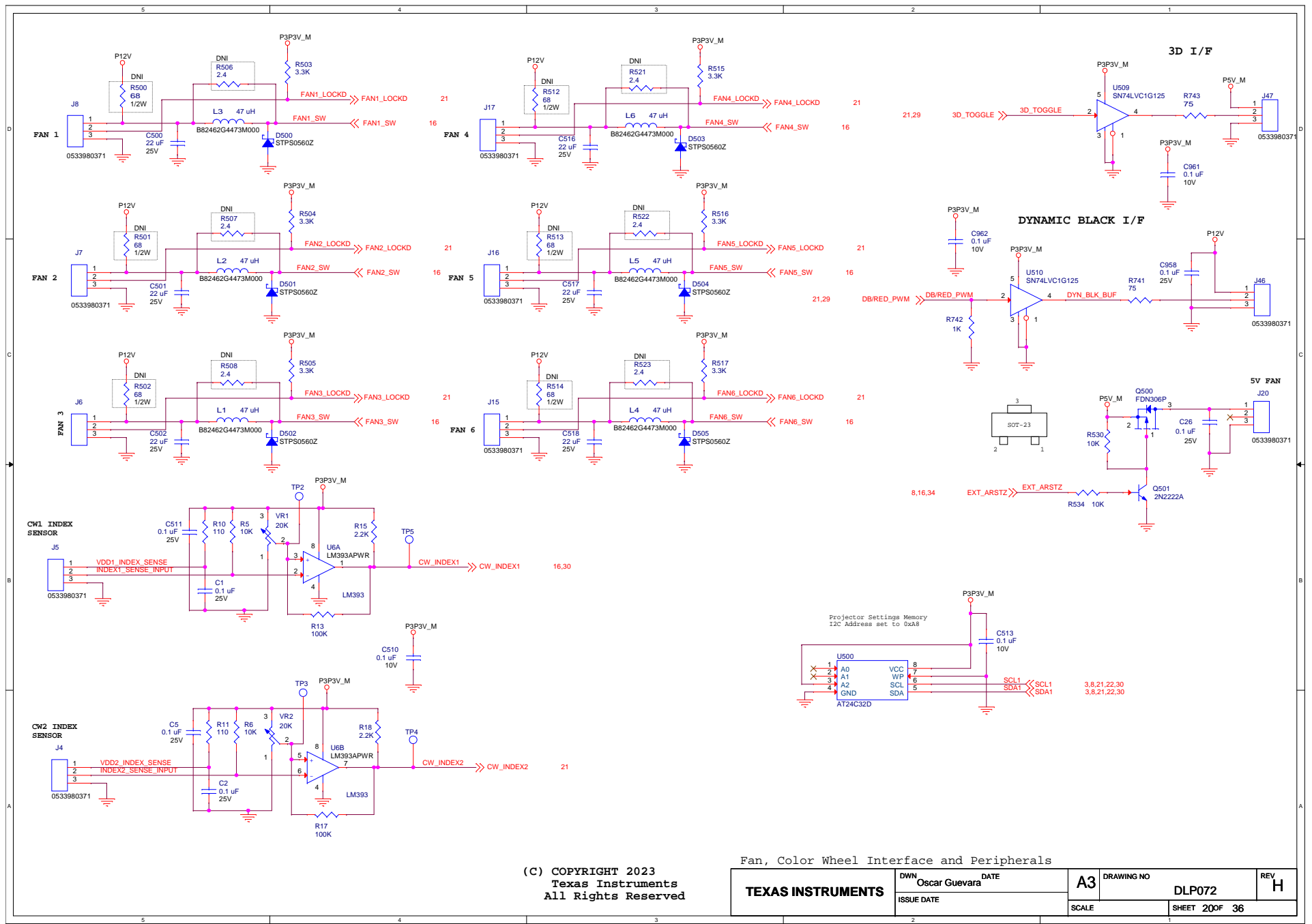


NOTE: This resistor value is dependant upon the CW motor used.  
 The value range is 0.47 ohms to 2.2 ohms.  
 The target voltage range for the SENSE pin is 100-150mV  
 when the CW is running at a stable speed.

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Color Wheel Drive

|                   |                   |      |                |            |     |
|-------------------|-------------------|------|----------------|------------|-----|
| TEXAS INSTRUMENTS | DWN Oscar Guevara | DATE | A3             | DRAWING NO | REV |
|                   | ISSUE DATE        |      |                | DLP072     | H   |
| SCALE             |                   |      | SHEET 19 OF 36 |            |     |

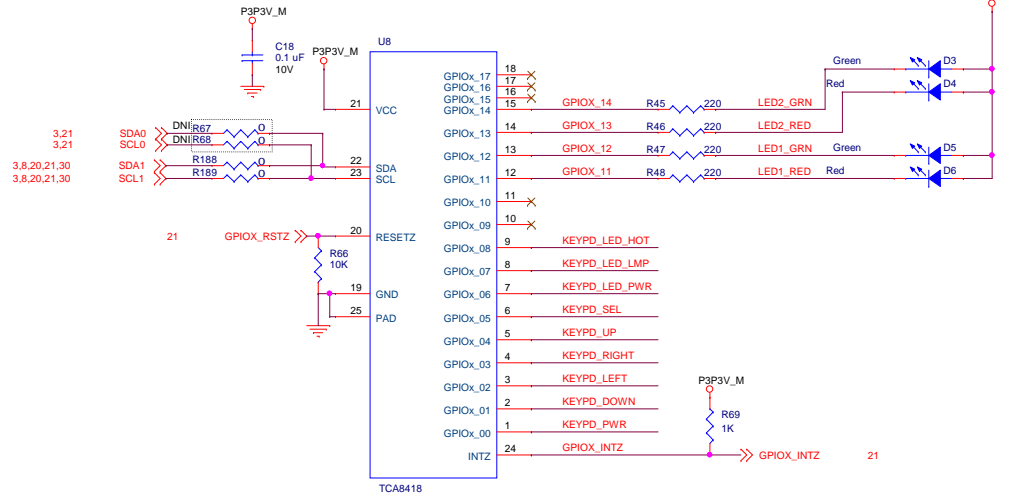


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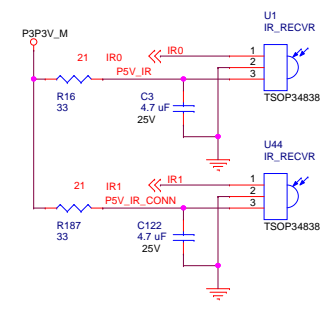
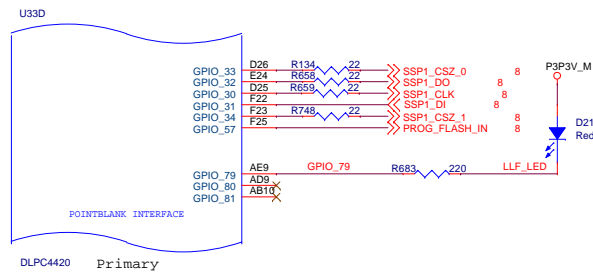
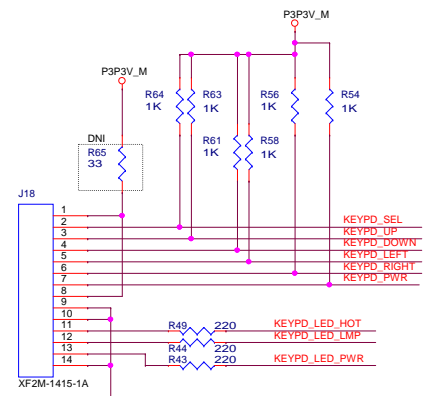
Fan, Color Wheel Interface and Peripherals

|                   |            |               |      |  |       |            |                |     |   |
|-------------------|------------|---------------|------|--|-------|------------|----------------|-----|---|
| TEXAS INSTRUMENTS | OWN        | Oscar Guevara | DATE |  | A3    | DRAWING NO | DLP072         | REV | H |
|                   | ISSUE DATE |               |      |  | SCALE |            | SHEET 20 OF 36 |     |   |





**KEYBOARD INTERFACE**

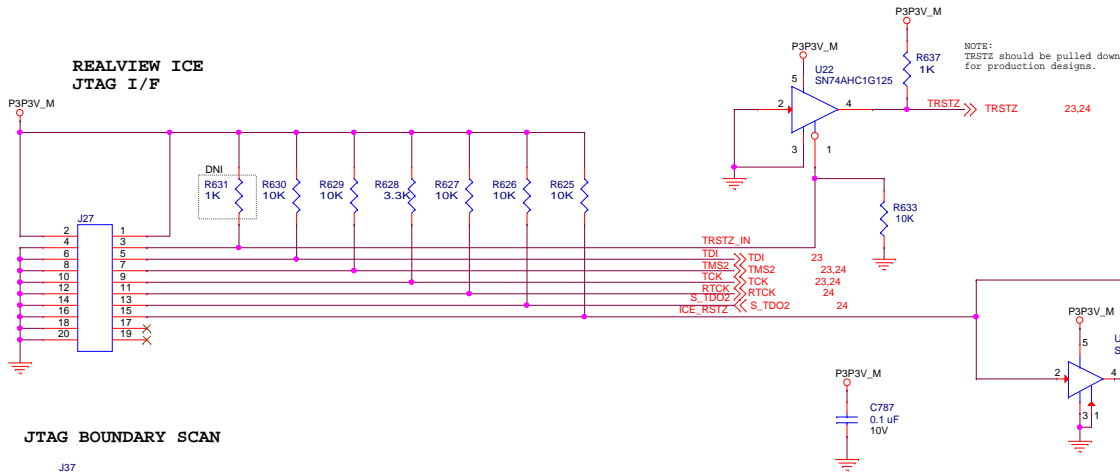


GPIO Expander, Keypad Interface and IR Interface

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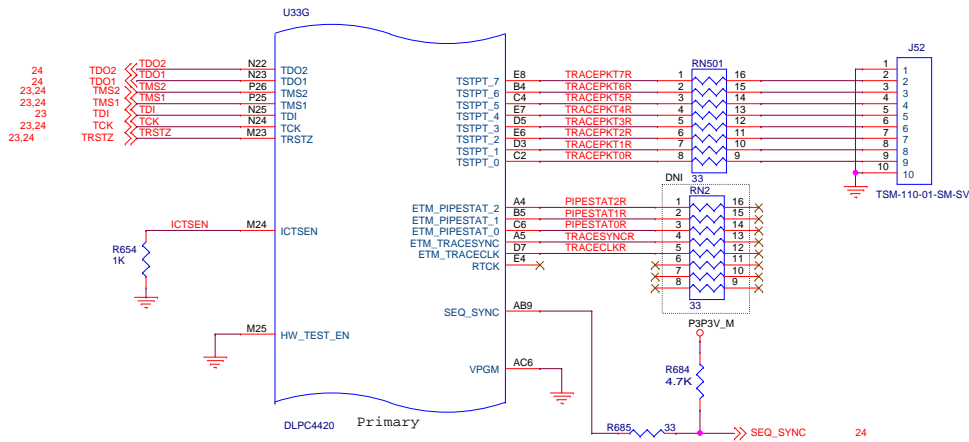
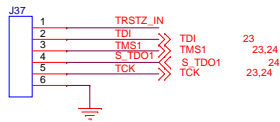
|                          |                   |       |           |                             |                 |
|--------------------------|-------------------|-------|-----------|-----------------------------|-----------------|
| <b>TEXAS INSTRUMENTS</b> | DWN Oscar Guevara | DATE  | <b>A3</b> | DRAWING NO<br><b>DLP072</b> | REV<br><b>H</b> |
|                          | ISSUE DATE        | SCALE |           |                             |                 |

**REALVIEW ICE  
JTAG I/F**



| MANUAL RESET JUMPER |                            |
|---------------------|----------------------------|
| INSTALLED           | HOLD IN RESET              |
| NOT INSTALLED       | NORMAL OPERATION (DEFAULT) |

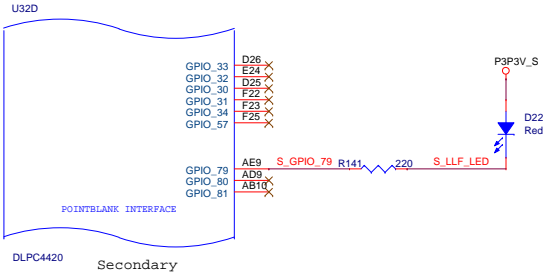
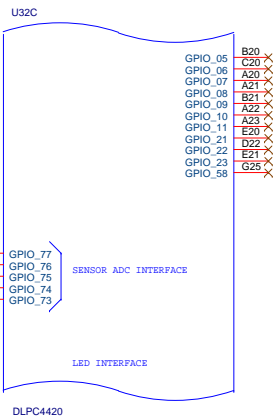
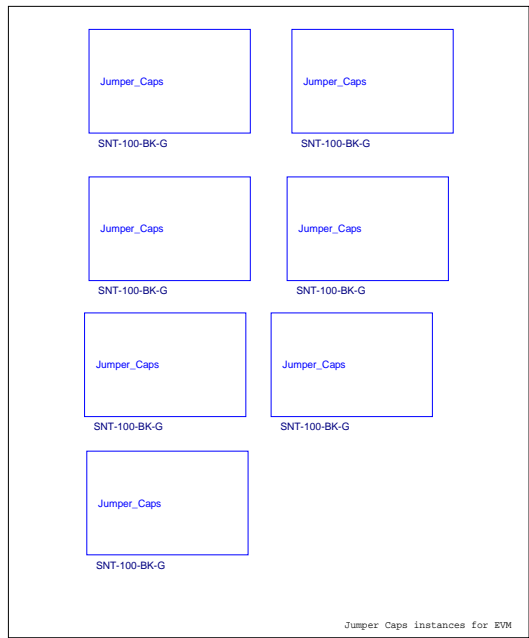
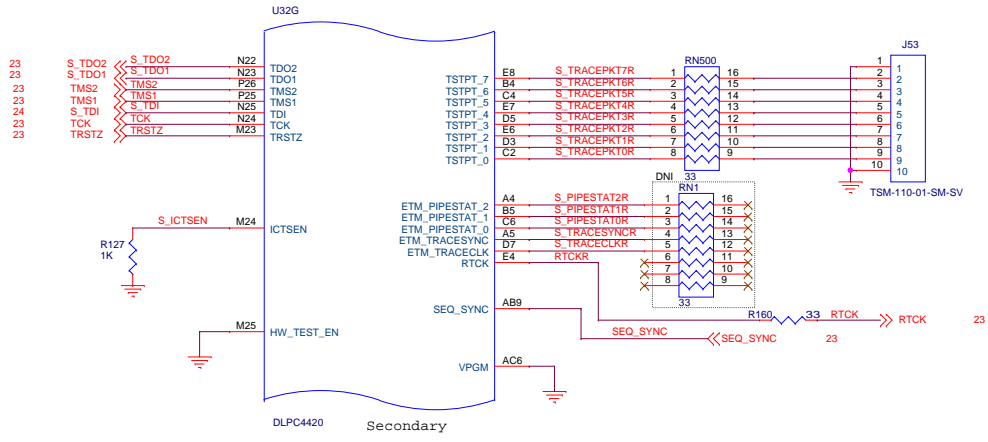
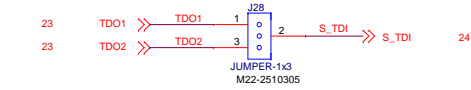
**JTAG BOUNDARY SCAN**



Primary Controller Test Points, ARM Trace, JTAG, and Reset

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|--------------------------|-------------------|------|----------------|-----|
| <b>TEXAS INSTRUMENTS</b> | DWN Oscar Guevara | DATE | DRAWING NO     | REV |
|                          | ISSUE DATE        |      | DLP072         | H   |
| SCALE                    |                   |      | SHEET 23 OF 36 |     |



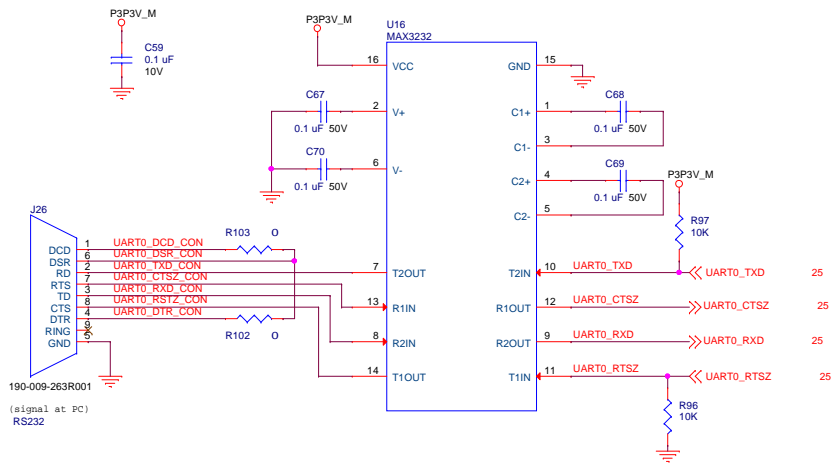
Secondary Controller Test Points, ARM Trace, and JTAG

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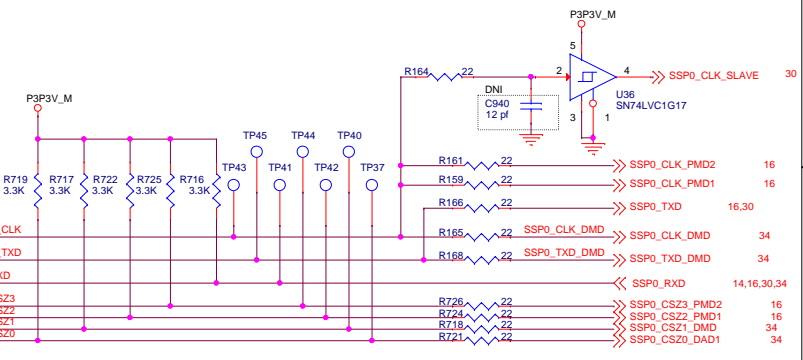
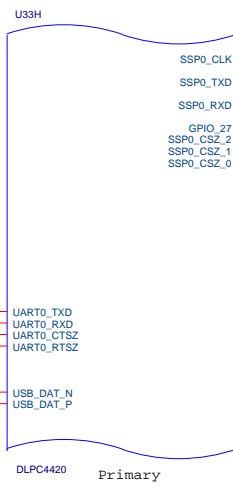
|                   |                   |      |                |            |     |
|-------------------|-------------------|------|----------------|------------|-----|
| TEXAS INSTRUMENTS | DWN Oscar Guevara | DATE | A3             | DRAWING NO | REV |
|                   | ISSUE DATE        |      |                | DLP072     | H   |
| SCALE             |                   |      | SHEET 24 OF 34 |            |     |



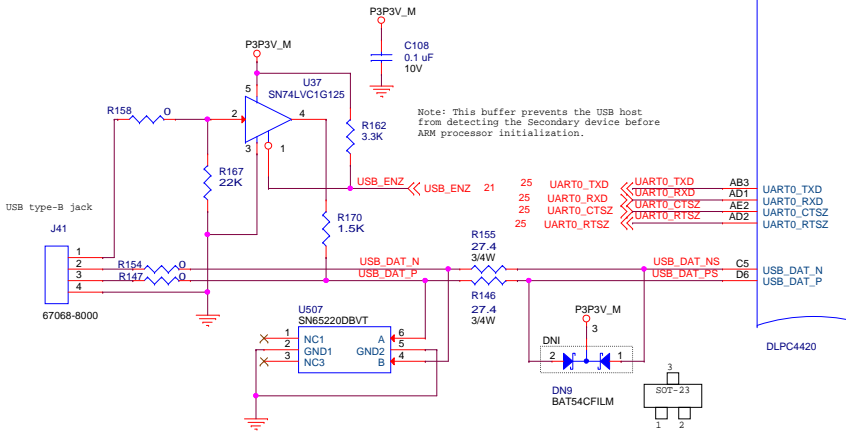
RS - 232 PORT 0



190-009-263R001  
(signal at PC)  
RS232



Note: TI recommends signal integrity analysis be performed for the SPI bus to determine the optimum buffering and termination.

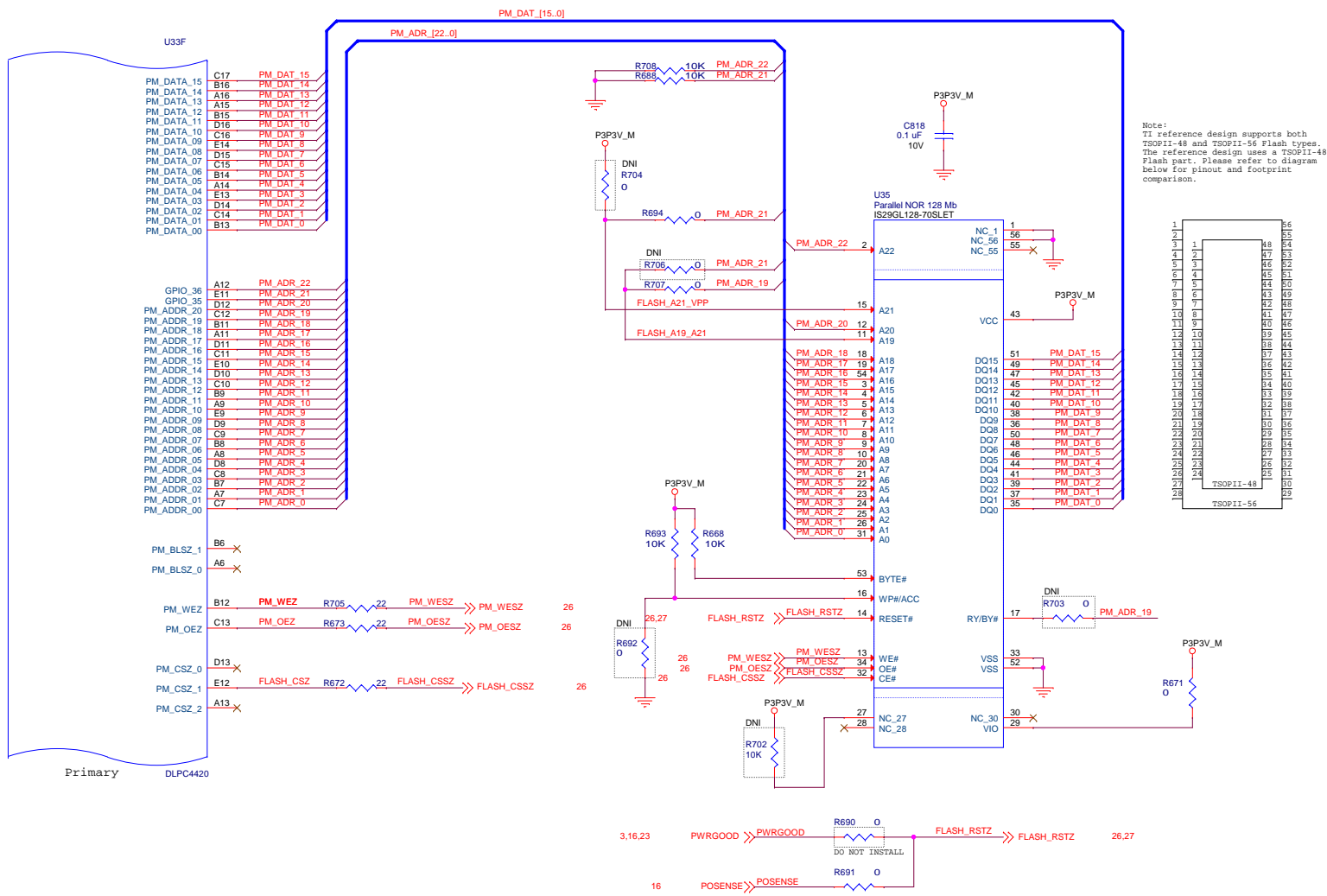


Note: This buffer prevents the USB host from detecting the Secondary device before ARM processor initialization.

Primary Controller RS-232, Synchronous Serial Port, and USB

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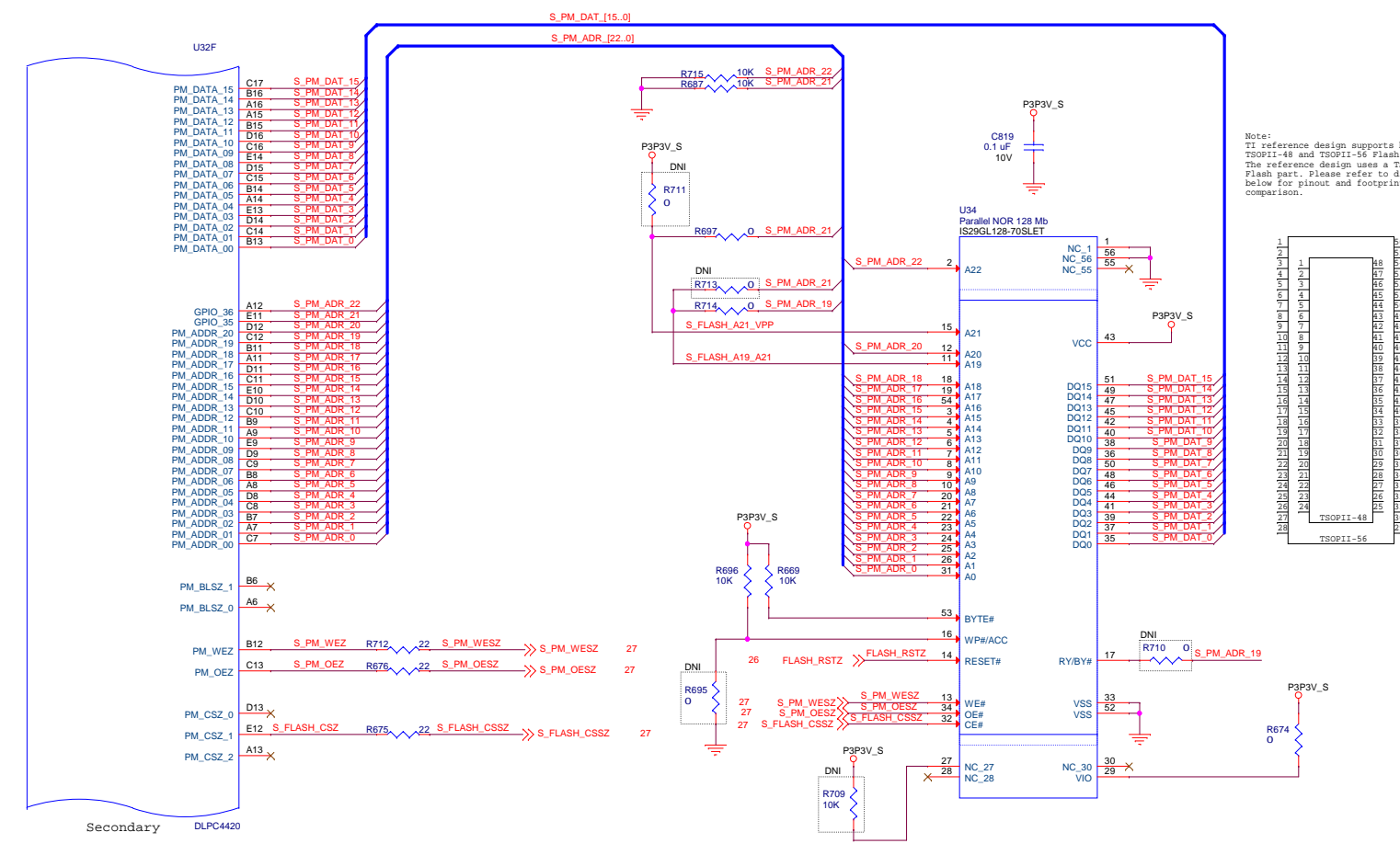
|                   |                   |      |                |            |     |
|-------------------|-------------------|------|----------------|------------|-----|
| TEXAS INSTRUMENTS | DWN Oscar Guevara | DATE | A3             | DRAWING NO | REV |
|                   | ISSUE DATE        |      |                | DLP072     | H   |
| SCALE             |                   |      | SHEET 25 OF 36 |            |     |



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Primary Controller Flash Memory Interface

|                   |                   |       |    |                      |          |
|-------------------|-------------------|-------|----|----------------------|----------|
| TEXAS INSTRUMENTS | DWN Oscar Guevara | DATE  | A3 | DRAWING NO<br>DLP072 | REV<br>H |
|                   | ISSUE DATE        | SCALE |    |                      |          |



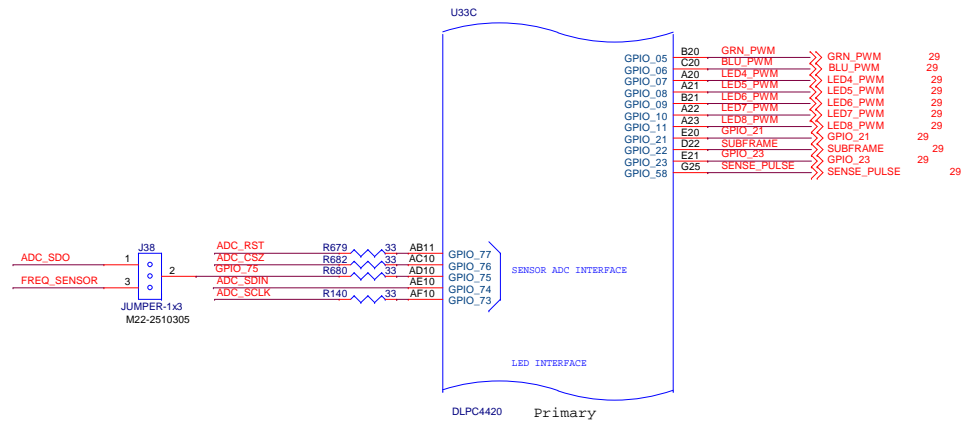
Note:  
 TI reference design supports both  
 TSOP11-48 and TSOP11-56 Flash types.  
 The reference design uses a TSOP11-48  
 Flash part. Please refer to diagram  
 below for pinout and footprint  
 comparison.

|    |    |
|----|----|
| 1  | 56 |
| 2  | 55 |
| 3  | 54 |
| 4  | 53 |
| 5  | 52 |
| 6  | 51 |
| 7  | 50 |
| 8  | 49 |
| 9  | 48 |
| 10 | 47 |
| 11 | 46 |
| 12 | 45 |
| 13 | 44 |
| 14 | 43 |
| 15 | 42 |
| 16 | 41 |
| 17 | 40 |
| 18 | 39 |
| 19 | 38 |
| 20 | 37 |
| 21 | 36 |
| 22 | 35 |
| 23 | 34 |
| 24 | 33 |
| 25 | 32 |
| 26 | 31 |
| 27 | 30 |
| 28 | 29 |

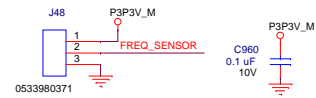
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Secondary Controller Flash Memory Interface

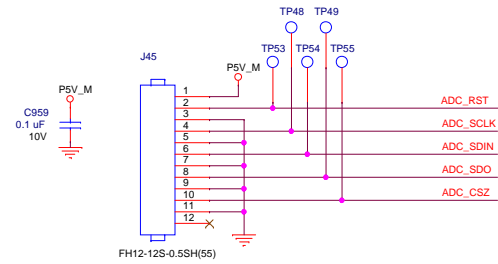
|                          |                        |                      |        |              |
|--------------------------|------------------------|----------------------|--------|--------------|
| <b>TEXAS INSTRUMENTS</b> | DWN Oscar Guevara DATE | <b>A3</b> DRAWING NO | DLP072 | REV <b>H</b> |
|                          | ISSUE DATE             |                      |        |              |



LIGHT TO FREQUENCY SENSOR I/F



ADC INTEGRATING SENSOR BOARD I/F

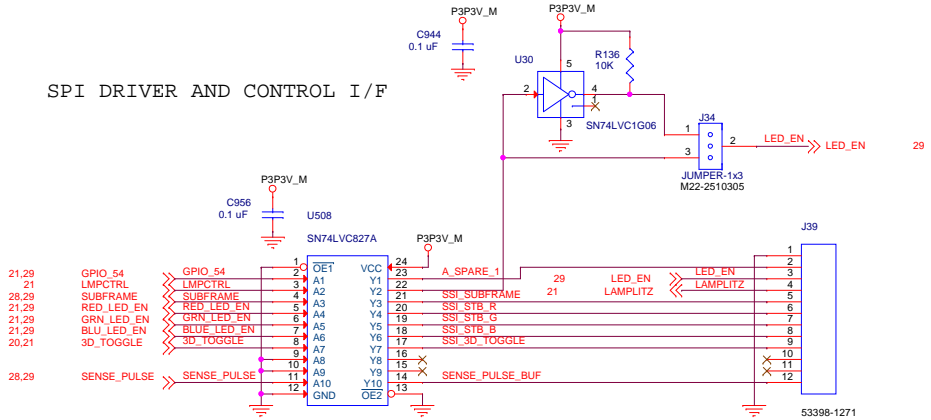


Primary Controller SSI Sensor Interface

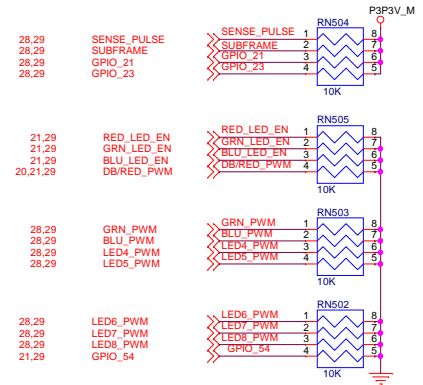
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|                   |                   |      |       |            |          |     |   |
|-------------------|-------------------|------|-------|------------|----------|-----|---|
| TEXAS INSTRUMENTS | DWN Oscar Guevara | DATE | A3    | DRAWING NO | DLP072   | REV | H |
|                   | ISSUE DATE        |      | SCALE | SHEET      | 28 OF 36 |     |   |

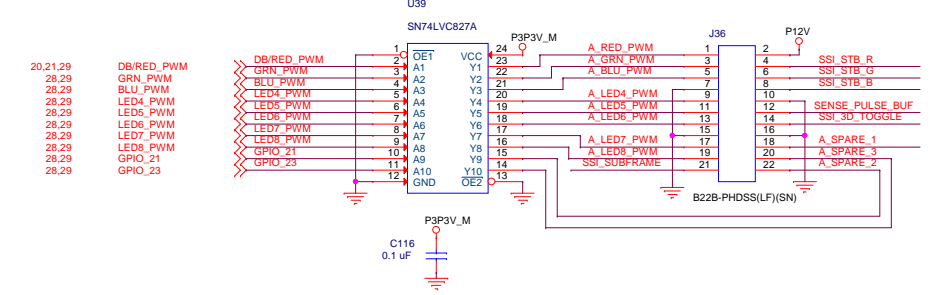
SPI DRIVER AND CONTROL I/F



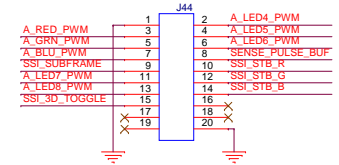
PULL-UP/PULL-DOWN RESISTORS



PWM SSI DRIVER I/F



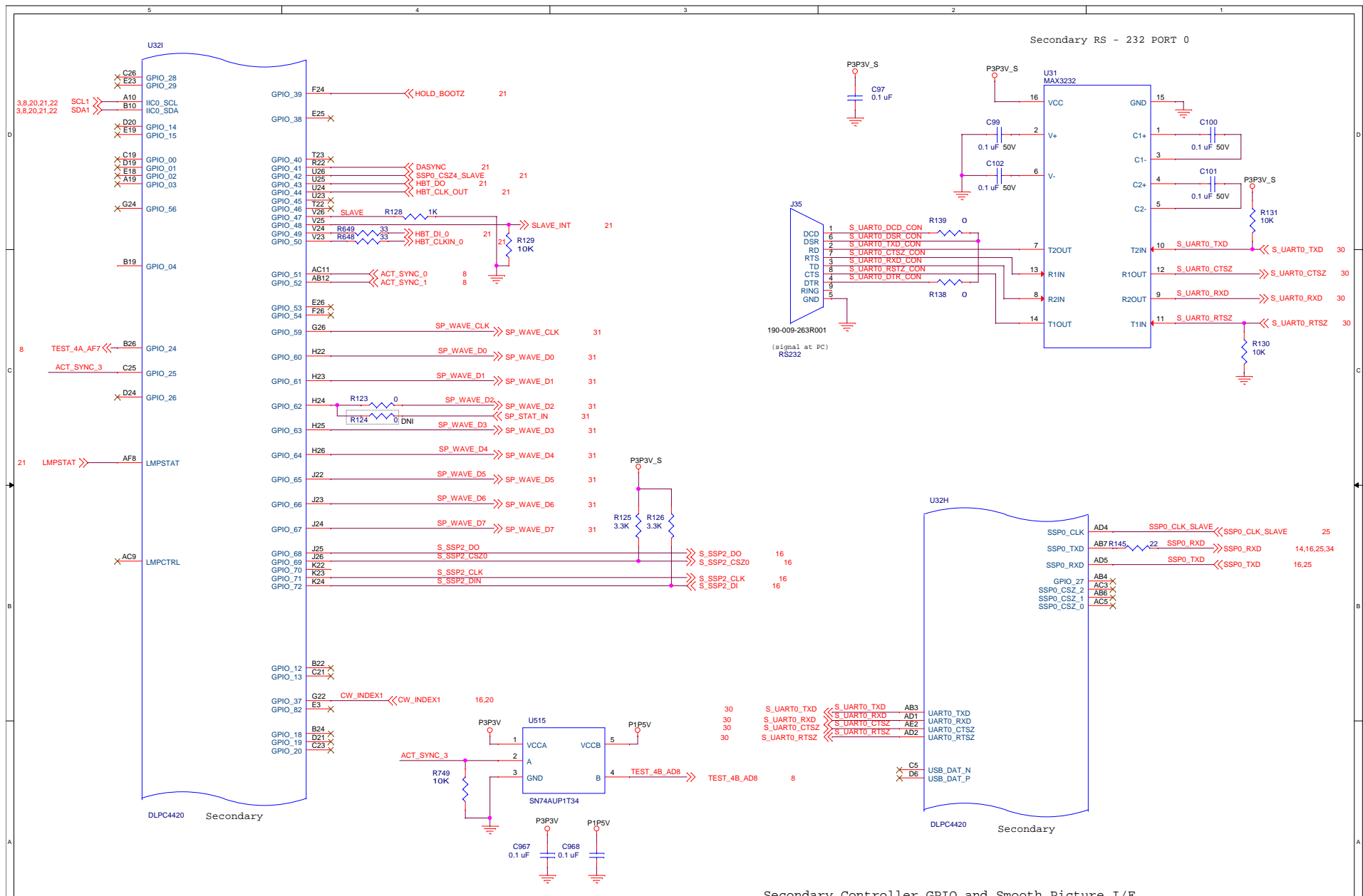
TESTPOINTS



SSI Driver Interfaces

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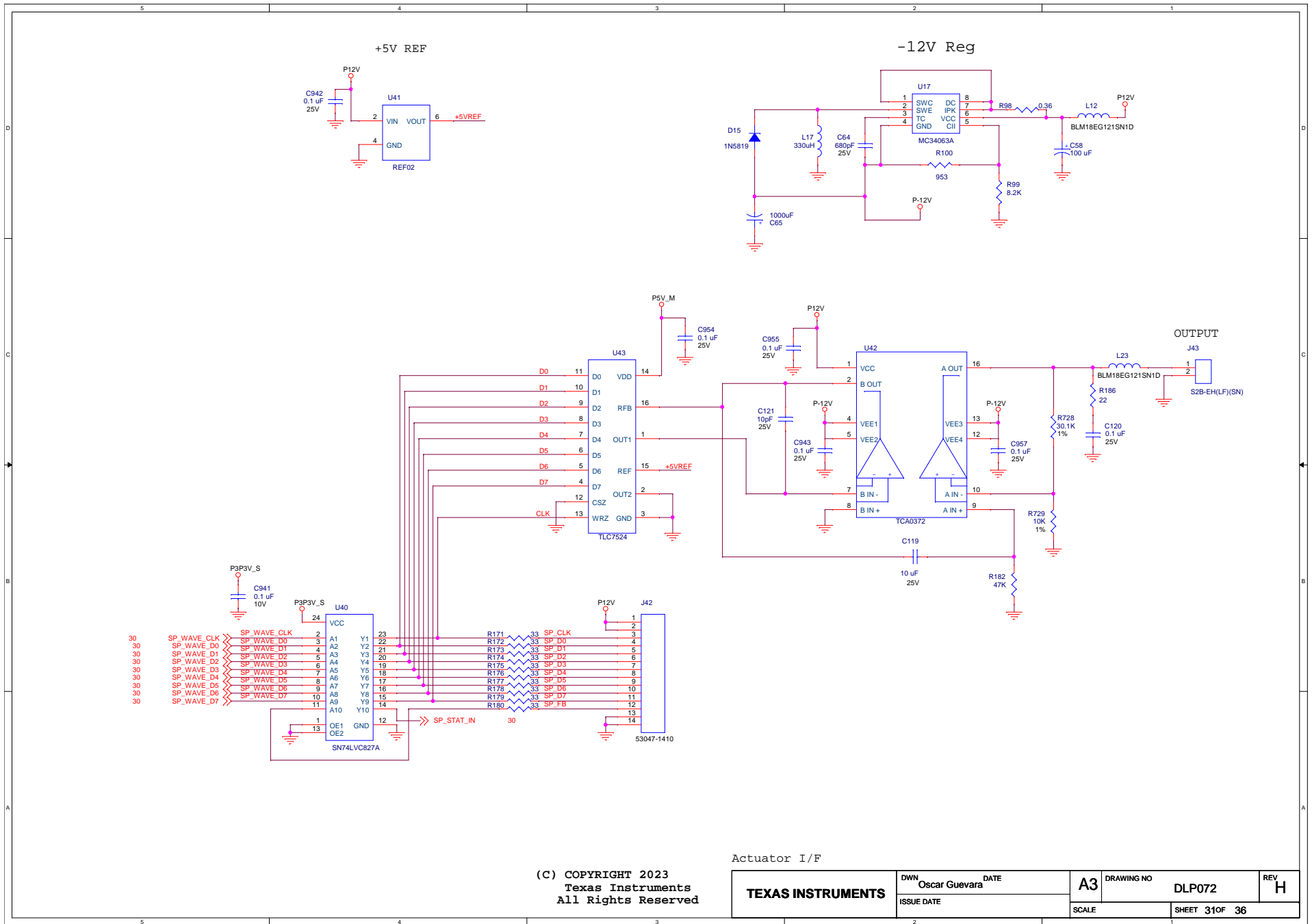
|                   |                   |      |                |            |       |
|-------------------|-------------------|------|----------------|------------|-------|
| TEXAS INSTRUMENTS | DWN Oscar Guevara | DATE | A3             | DRAWING NO | REV H |
|                   | ISSUE DATE        |      |                | DLP072     |       |
| SCALE             |                   |      | SHEET 29 OF 36 |            |       |



Secondary Controller GPIO and Smooth Picture I/F

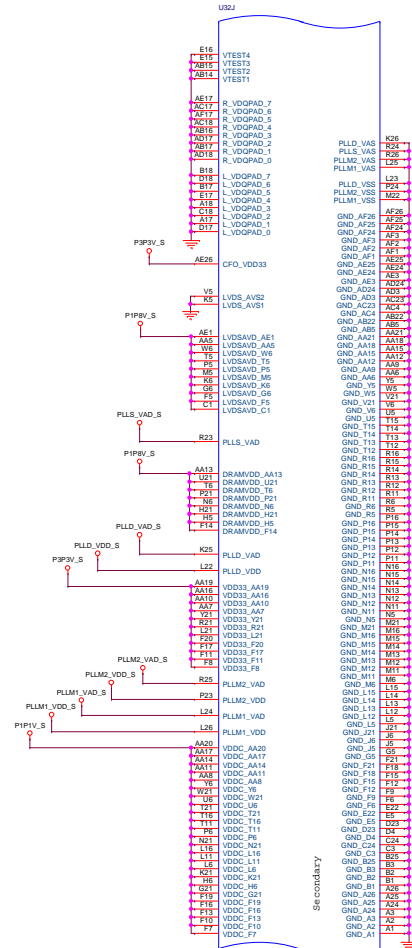
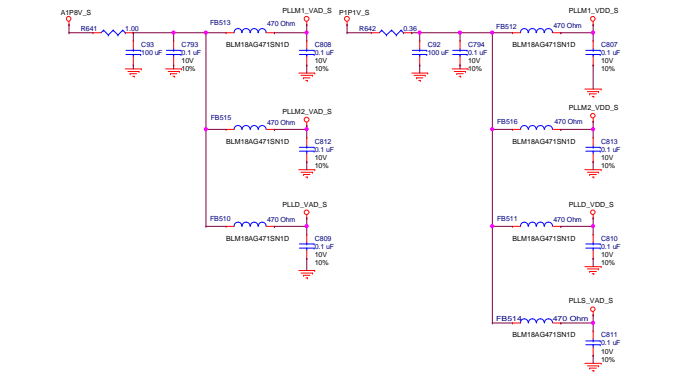
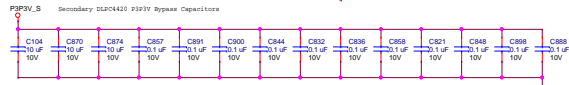
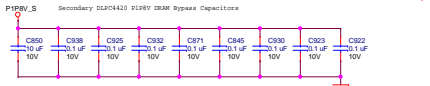
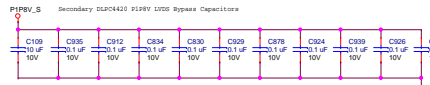
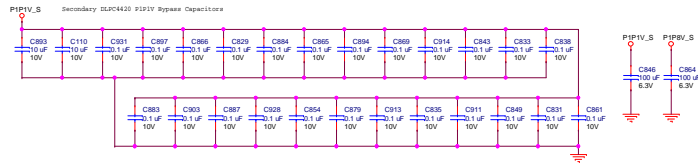
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|-------------------|------------------------|---------------|------------|-----|
| TEXAS INSTRUMENTS | DWN Oscar Guevara DATE | A3            | DRAWING NO | REV |
|                   | ISSUE DATE             |               | DLP072     |     |
| SCALE             |                        | SHEET 30OF 36 |            |     |





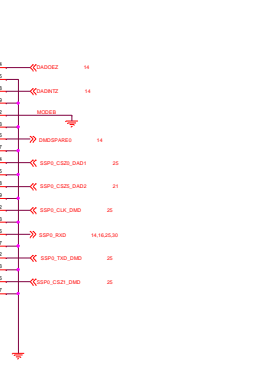
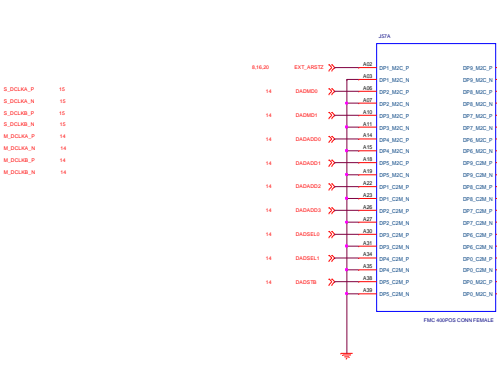
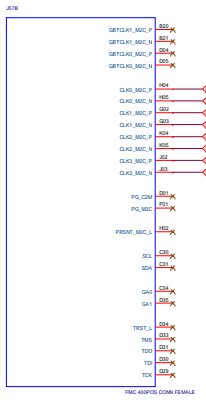
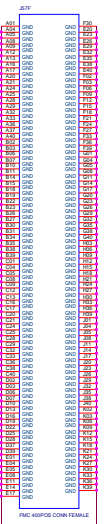
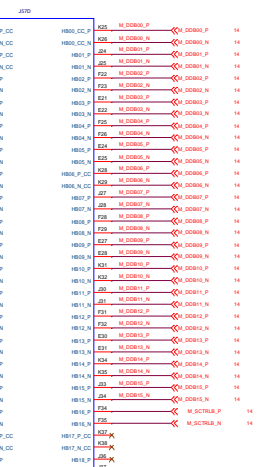
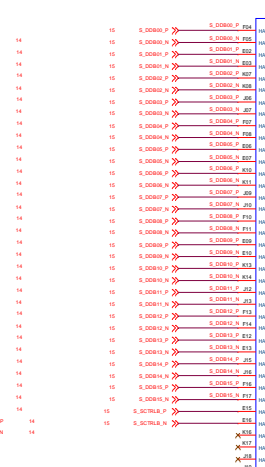
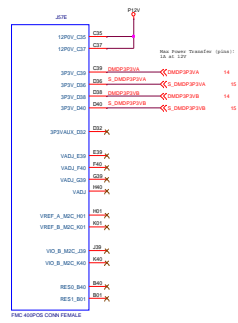




Secondary Controller Power and Bypass Capacitors

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|-------------------|------------|------|----|------------|-----|
| TEXAS INSTRUMENTS | OWN        | DATE | A2 | DRAWING NO | REV |
|                   | ISSUE DATE | DATE |    |            |     |



Revision A:  
Initial Release

Revision B:  
All Pages: Resequenced reference designators to align with layout  
Page 1: Updated notes with correct voltage names  
Updated index  
Page 4: Rearranged DDR3\_1\_DQ[15:0] for routability

Revision C:  
Page 3: Change U5 to Do Not Install  
Updated C545 and C549 as Do Not Install  
Changed U506 to 75 Mhz  
Page 11: Added Note Connecting pin 15 of U24 to P3P3V  
Page 8: Changed R89, R90, R91, R92, and R541 to 0 ohms.

Revision D:  
Page 3: Changed net name TEST\_4A\_AC6 to VX1\_3D\_EN.  
Changed net name TEST\_4A\_AE6 to VX1\_LR\_SYNC.  
Page 8: Added R190, R191, R192, and R193.  
Changed net name TEST\_4A\_AC6 to VX1\_3D\_EN.  
Changed net name TEST\_4A\_AE6 to VX1\_LR\_SYNC.  
Page 11: Connected pin 15 of U24 to P3P3V.  
Page 16: Changed C799 and C801 to 1800pF.  
Page 21: Added note to ballast circuit.  
Page 22: Added R188 and R189.  
Page 23: Changed RN501 to Install, added J52 header.  
Page 24: Changed RN500 to Install, added J53 header.

Revision E:  
Page 11: Changed U24-10, C85 connection from P3P3V to P5V\_S.

Revision F:  
Page 3: Added U514, Y1, R745, R746, R747, C966  
Page 3: Removed FB502, C534, U506  
Page 8: Added J54, J55, and J56  
Page 22: Added R748 and connection to GPIO\_34

Revision G:  
Page 8: Added Off-Page connections to TEST\_4A\_AF7 and TEST\_4B\_AD8.  
Page 30: Added TEST\_4A\_AF7 connection to GPIO\_24 on U32

Revision H:  
Page 3: Updated FE\_12V to RE\_5V  
Removed nets: "USB+5V", "USB\_D+", "USB\_D-"  
Added I2C nets "SCL1", "SDA1"  
Rearraged nets "VX1\_LR\_SYNC", "FE\_RST", "SDA0", "I2C\_BUSY"  
Page 14: Removed J51  
Page 15: Removed J50  
Page 34: Added J57 FMC Connector

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TEXAS INSTRUMENTS

DWN Oscar Guevara DATE  
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A3

DRAWING NO  
DLP072

REV  
H

SCALE

SHEET 35 OF 36

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|                          | ISSUE DATE             |                | DLP072     |                 |
| SCALE                    |                        | SHEET 36 OF 36 |            |                 |