DSI Setup and Debugging Guide v1.0

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Contents

Note: The information in this document is not a substitute for the specifications listed in the corresponding device datasheets. In the event of a discrepancy, the datasheet supersedes this document.

DSI Overview

DSI (Display Serial Interface) is a source synchronous, high speed, low power, differential video interface. The DLPC3430 and DLPC3433 (both a part of the DLPC343x family) support the DSI Type-3 LVDS video interface with up to 4-lanes. DSI is a useful alternative to a parallel interface if a reduction in data lanes is desired. This can be useful to save space in a PCB (printed circuit board) layout, or it can be useful if a desired front end processor has a reduced pin count that only supports DSI video.

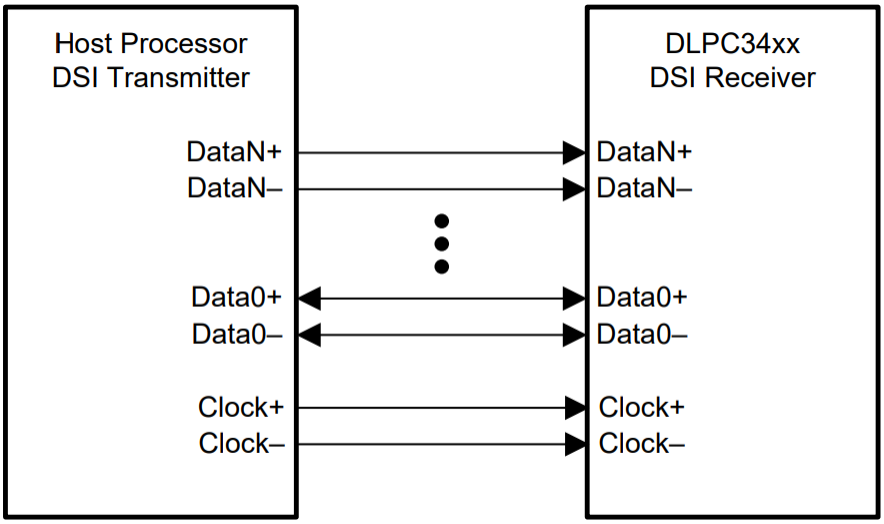

Figure 1: Overview

There are two main transmission modes: differential HS (high speed) mode and single-ended LP (low power) mode. HS mode is used to transmit video data. LP mode is used to send commands or enter a power savings mode. The DLPC343x has specific requirements of when these various modes are allowed. For additional specification details visit mipi.org. A summary of the modes as implemented on the DLPC343x follows:

- LP mode: Signal level is 1.1V (1.2V if VDDLP12 is not tied to VDD) single ended and the clock lane is not used to decode the data.
  - LP11: A low power state when both data lanes (e.g. DD0n and DD0P) are set high.
- HS mode: Signals are 200mV LVDS DDR (low-voltage differential signaling double data rate) and the clock lane is used to decode the data.
  - Note that a set of LP states are commanded (LP11 -> LP01 -> LP00) to transition from LP mode to HS mode. This transition will automatically enable a terminating resistor in the DLPC343x controller. If the termination resistor is not enabled a 400mV signal will be seen on the data lanes. During nominal operation this should never occur.

The DLPC3430 and DLPC3433 controllers implement DSI v1.02.00 and D-PHY MIPI v1.0 (see exceptions in DSI Setup and DSI Timings). While not officially supported, an unpopulated DSI connector is available on the DLPDLCR3010EVM-G2. No DSI connector is available on the DLPDLCR2010EVM (therefore a custom board would be needed).

DLPC343x Setup

- Use a DLPC3430 or DLPC3433 controller for DSI use with the DLP2010 or DLP3010 DMD respectively.
- Configure the number of DSI lanes that will be used with GPIO_01 and GPIO_02. The GPIO pins are sampled during boot up and should be pulled-up or pulled-down appropriately (an 8-kΩ resistor is appropriate).
    - Note that these GPIO pins are used as part of SPI bus 1. The pull-up or pull-down resistors should be appropriately sized to not interfere with the SPI bus. The voltage is sampled during controller startup and is not sampled again during normal operation (thus one cannot dynamically change lanes)

GPIO_02	GPIO_01	Number of DSI Data Lanes
DSI Lane Config 1	DSI Lane Config 0	
0	0	1
0	1	2
1	0	3
1	1	4

Figure 2: GPIO and Lane Configuration

- Ensure the RREF pin is pulled-down to ground through a 30-kΩ ±1% resistor.
- Ensure VDDLP12 is connected to VDD (1.1V +/- 5%). It is also acceptable to tie this pin to a separate 1.2V +/- 6.67% rail; however, this is not necessary. If a separate 1.2V signal is used it must power on after VDD and power down before VDD.
- Startup the DLPC343x controller by pulling PROJ_ON high and the power-up sequence begins.
- Execute the following commands. This can be done through an autoinit batch file but you can also directly send the I2C command after the controller is initialized (HOST_IRQ goes low)
    - *Write DSI Port Enable (0xD7):* Enable the DSI interface. This must be called before setting the DSI HS Clock. Note some firmware has DSI enabled by default but it is still acceptable to call this command.
    - *Write Image Crop (0x10): Select which portion of the input image is used*
    - *Write Display Size (0x12): Select size of active image to be displayed*
    - *Write Input Image Size (0x2e): Specify active data size of input image*
    - *Set DSI HS Clock input (0xBD):* Specify the high speed DSI clock
    - *Write Input Source Select (0x05)*: Set to external video
    - *Write External Video Source Format Select (0x07)*: Auto detect DSI format
    - Example batch file

```
#Write: DSIPortEnable
W 36 d7 00
# Write: ImageCrop: 854x480
W 36 10 00 00 00 00 56 03 e0 01
# Write: DisplaySize: 854x480
W 36 12 00 00 00 00 56 03 e0 01
# Write: InputImageSize: 854x480
W 36 2e 56 03 e0 01
```

```
# Write: DsiHsClockInput
W 36 bd c8 00
# Write: InputSourceSelect, 0 = External Video Port
W 36 05 00
# Write: ExternalVideoSourceFormat 0x00 = DSI Auto
W 36 07 00
```

- Send the DSI signal. It is important this signal is not sent before the DLPC343x is initialized (i.e. the DSI clock and data lines should remain idle in LP11 mode until HOST_IRQ goes low). See the below diagram

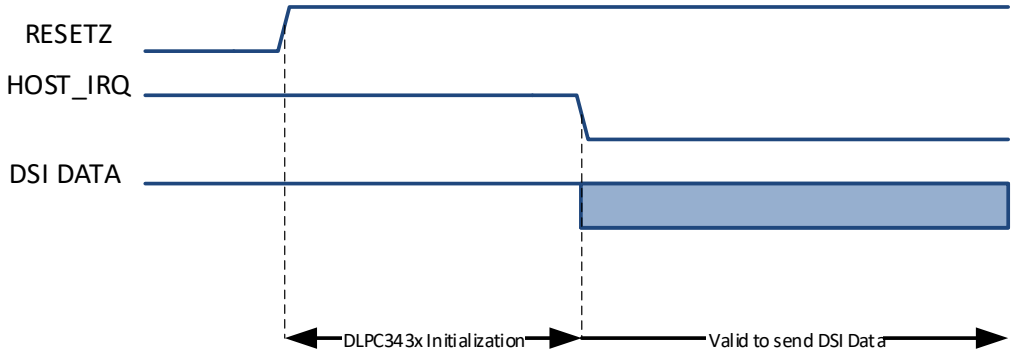

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Figure 3: DSI Startup

DSI Configuration Requirements

DSI Configuration Settings

- HS and LP Setup
    - Blanking Setup
        - HSync Blanking : Use HS Blanking (LP11 not supported)
        - HBPorch Blanking: Use HS Blanking (LP11 not supported)
        - HFPorch Blanking: Use HS Blanking (LP11 not supported)
        - Vsync (blanking and sync): Use LP11 (HS not supported)
        - Vertical Blanking: Use LP11 (HS not supported)
        - Turn clock off during LP Blanking: Disabled
    - Ensure low-power mode between pixels doesn't occur
- Command mode must not be enabled (i.e. MIPI Display Command Set℠, DCS℠, should not be used)
- EOT (End of Transfer) command must be enabled
- BTA (Bus Turn-Around) mode must be disabled

DSI Timings

- Ensure THS_PREPARE + THS_ZERO add to at least 465ns if the clock is 95MHz to 235MHz and ensure they add to at least 565ns if the clock is 80MHz to 94MHz.
- All the general parallel interface requirements in the DLPC343x datasheet must be followed (specifically the *Parallel Interface Frame Timing Requirements* section and the *Parallel Interface General Timing Requirements* section).
- All DSI timing requirements must be followed in addition to the following requirements from the datasheet:

6.15 DSI Host Timing Requirements

These timing requirements describe specific host minimum values that are higher than those specified in the MIPI standards. It is critical for proper operation that the host meet these minimum timing requirements for specified MIPI parameters. The decoded DSI data must also follow all *Parallel Interface Frame Timing Requirements*.

			MIN	MAX	UNIT
Clock lane	Frequency		80	235	MHz
Data lane	Effective data rate		160	470	Mbps
Number of data lanes	Selectable		1	4	Lanes
$t_{HS-PREPARE}$+ $t_{HS-ZERO}$	During a LP to HS transition, the time that the transmitter drives the HS-0 state prior to transmitting the synchronization sequence	80 MHz to 94 MHz HS Clock	565		ns
		95 MHz to 235 MHz HS Clock(1)	465(2)		ns
$t_{HS-SETTLE}$	Time interval during which the HS receiver ignores any data lane HS transitions, starting from the beginning of $T_{HS-PREPARE}$; the HS receiver ignores any data lane transitions before the minimum value, and responds to any data lane transitions after the maximum value	80 MHz to 94 MHz HS Clock		565(3)	ns
		95 MHz to 235 MHz HS Clock		465(3)	ns

(1) Example: At 172 MHz and $t_{HS-PREPARE}$ = 51.46 ns → 51.46 ns + $t_{HS-ZERO}$ ≥ 465 ns. Therefore $t_{HS-ZERO}$≥= 413.54 ns.
(2) Minimum values are higher than those required by the MIPI standard. $t_{HS-PREPARE}$ must be within the MIPI specified range.
(3) Maximum values are higher than those required by the MIPI standard.

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Additional DSI Considerations

- Ensure there are no DSI clock or data signals before the DLPC343x is initialized. In other words the DSI lines must be in LP11 mode. Only after the DLPC343x is initialized should these signals be sent
- The DSI lines are sensitive to temperature. High temperature may cause the image to freeze. Ensure there are no temperature gradients between the different DSI signals and ensure the PCB remains cool. A properly designed board should work over the operating temperature range supported by the DLPC343x controller.
- The propagation delay between the P and N signals should be matched within 8ps.
- DSI signals are very sensitive to EMI (electromagnetic interference) which may cause the image to freeze or be lost. It is recommended to physically separate or shield the signals from known EMI sources
    - Note: It has been observed that using a heat gun to test a PCB under temperature produces enough EMI to cause DSI to fail. If testing a board under temperature it is important to use a heat source that doesn't produce excessive EMI
- Ensure the RREF pin is pulled down to ground through a 30k +/- 1% resistor.
- The input source must be periodic. For example, if a 60 Hz frame rate is being used it must be 60 Hz with very small +/- variance.
- Note that when using Burst mode the clock can be set significantly higher than needed. While perhaps counter intuitive, this may actually save power. That is because the data will quickly transmit in a burst and then the remaining time will be spent in LP11 mode.

Example DSI Configuration and Timings

If setting up a new system it is suggested to start with the below sample timings which are known to work.

- Frame timings

Parameter	Value	Unit
HSync	3	pixels
HBPorch	7	
HFPorch	10	
HActive	854	
Vsync	3	Lines
VBPorch	7	
VFPorch	4	
VActive	480	
Line Time	31.7381	µs
PClk	25.9054	MHz
Frame Rate	60.0002	Hz
DSI Lane clock	210	MHz
Number of Lanes	1	
Play mode	Continuous	
Sync Mode	Events	
Burst Mode	Burst	
HSync Blanking	HS Blanking	
HBPorch Blanking	HS Blanking	
HFPorch Blanking	HS Blanking	
Vertical Blanking	LP11	
EOT Packets	Enabled	
Clock	On during LP blanking	
Pixel Format	Packed RGB565	

- DSI DPhy Timings

Parameter	Value	Unit
HSPrepare	76	ns
HSZero	400	
HSExit	114	
HSTrail	76	
Clk Prepare	76	
ClkZero	247	
ClkTrail	76	
ClkPre	38	
ClkPost	228	
TAGo	228	
Wakeup	1000000	

DSI Waveforms

While accurate DSI signal measurements should be made with a proper DSI analyzer, engineers often do not have easy access to this expensive and specialized equipment. Therefore, some waveforms are shown below taken with passive, single-ended, 500MHz bandwidth probes (P6139A). While signal integrity can't reliably be determined from these waveforms, they can be used to verify that the DSI configuration is generally correct.

In all scope plots below, channel 1 (yellow) is DCLK0P, channel 2 (blue) is DCLK0N, channel 3 (purple) is DD0P, and channel 4 (green) is DD0N. A lot of scope noise is observed below and should not be attributed to incorrect signals. In this setup a 60 Hz video input and 1 data lane is used. A single data lane is useful for debugging so the full serial data can be captured on one lane. The full configuration settings used for the properly configured DSI waveform is at the end of this section.

Nominal: Entire Video Frame

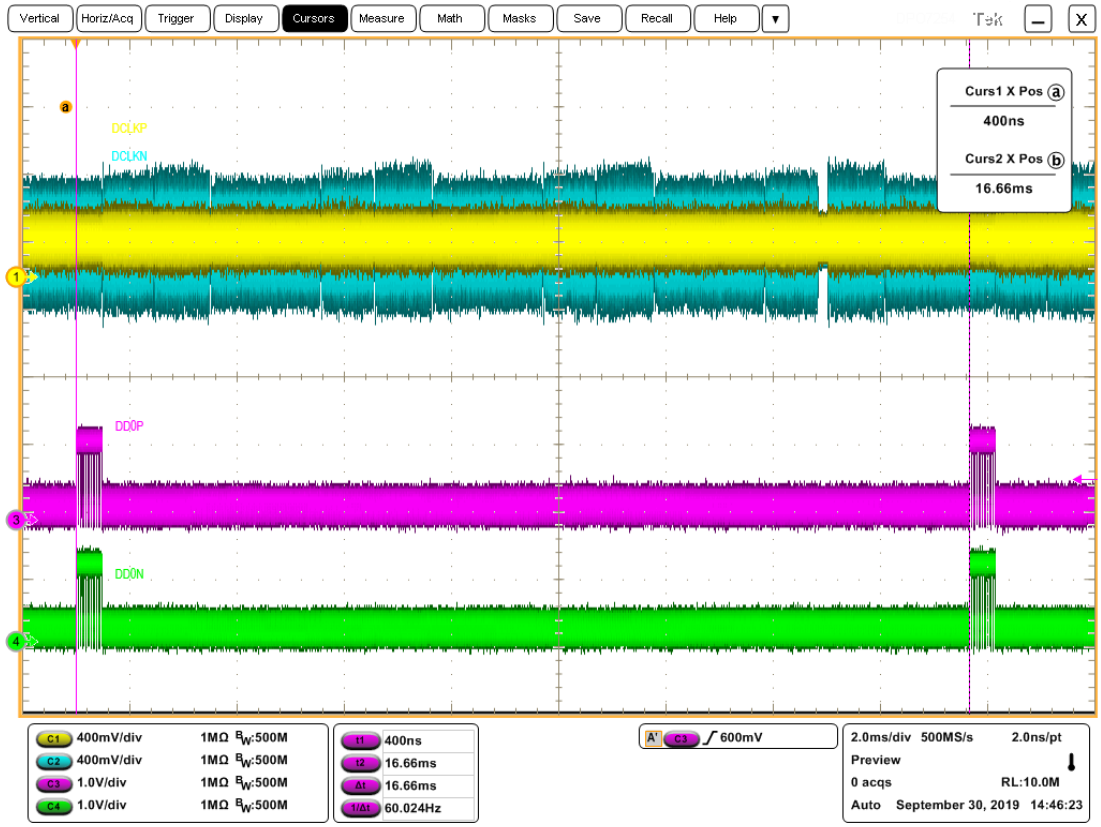

Figure 4: Properly Configured DSI Waveform

In this properly configured DSI waveform, once every frame period (in this case 1 / 60 Hz = 16.67ms), the data lane enters LP11 mode (which is seen above to the right of each cursor as DD0P and DD0N go to 1.1V). Between lines the data is always in HS mode (200mV differential signal). The clock is always in HS mode (200mV differential signal). The larger DCLK0N voltage swing compared to DCLK0P is attributed to scope noise. For these configuration timings see figure

Nominal: Video Transmission

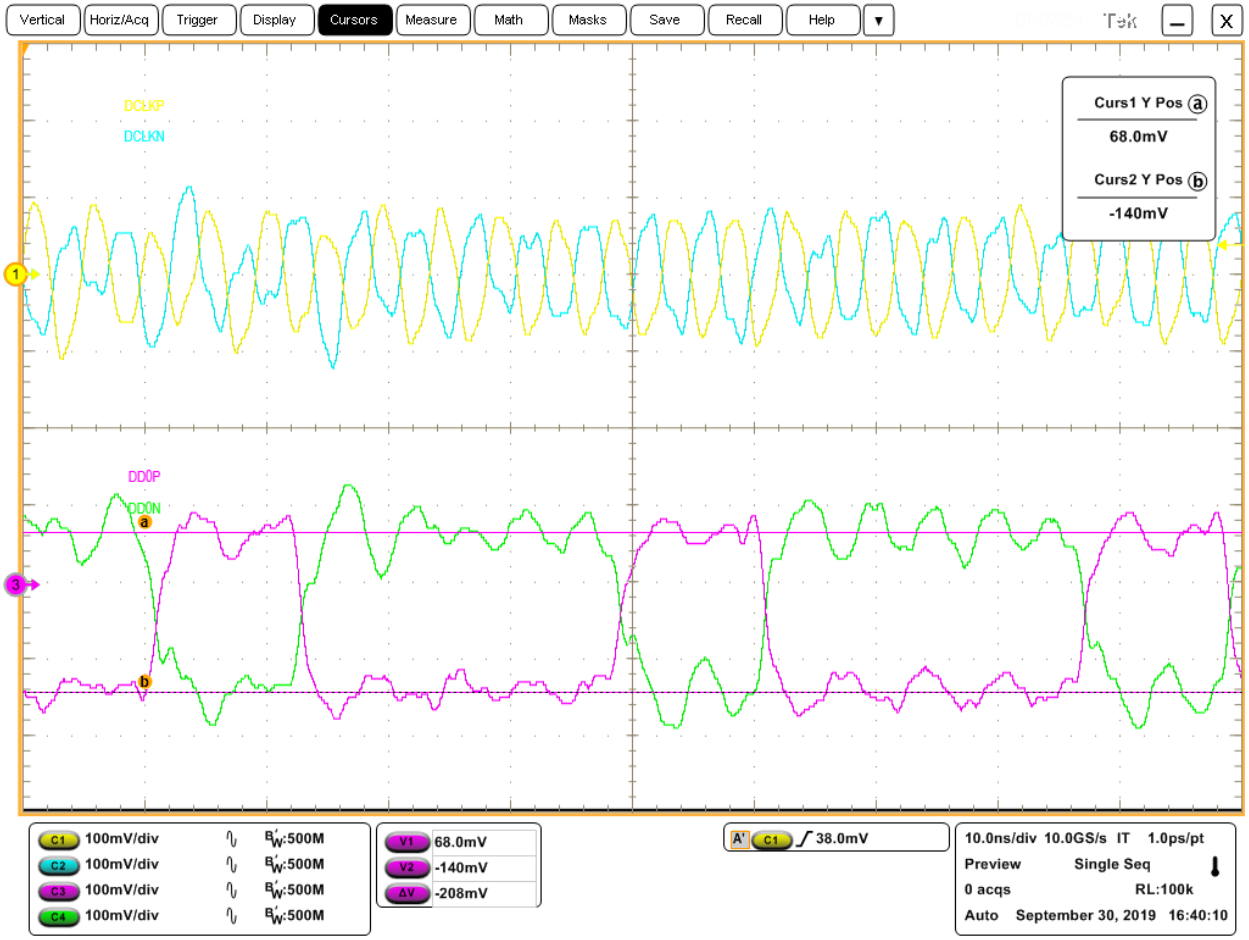

Figure 5: Zoomed in Waveform of Video Transmission

Above is a zoomed in, AC coupled waveform of the DSI signals during HS video transmission. As can be seen, the signals are 200mV differential. As previously mentioned, with the scope utilized, these signals cannot reliably be used to determine signal integrity.

Incorrect: LP during HSYNC

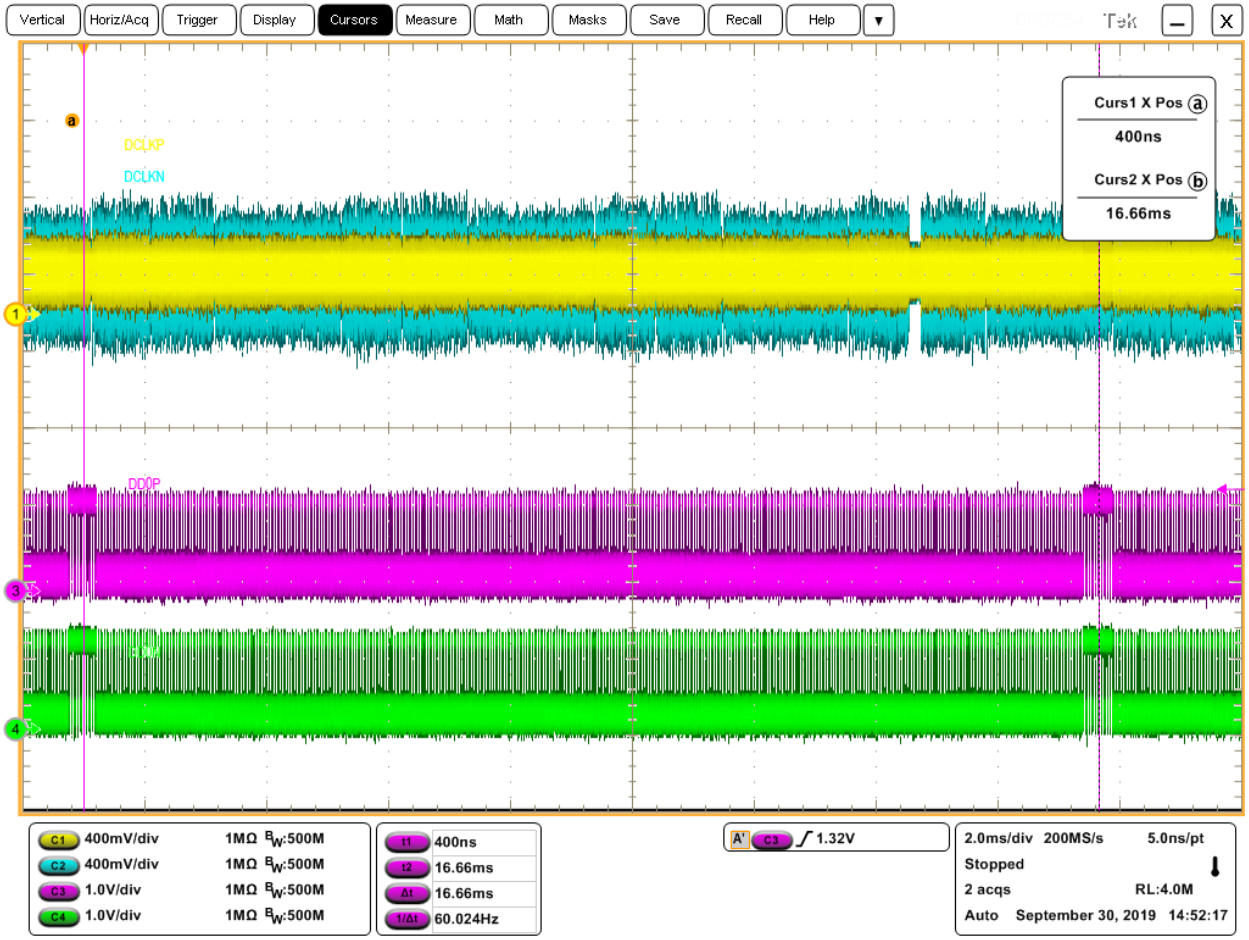

Figure 6: Improperly Configured DSI Waveform (LP Mode During HSYNC)

If LP mode is enabled during HSYNC (or perhaps the horizontal porches) it is seen that the data signals go high between the vertical blanking times. Therefore, instead of the DD0x lanes staying at 200mV differential, it will rapidly switch between 200mV differential and 1.1V single ended. While this may work in some situations, it is not supported by the DLPC343x controller and issues have been seen at high temperature.

Incorrect: Data always in HS Mode

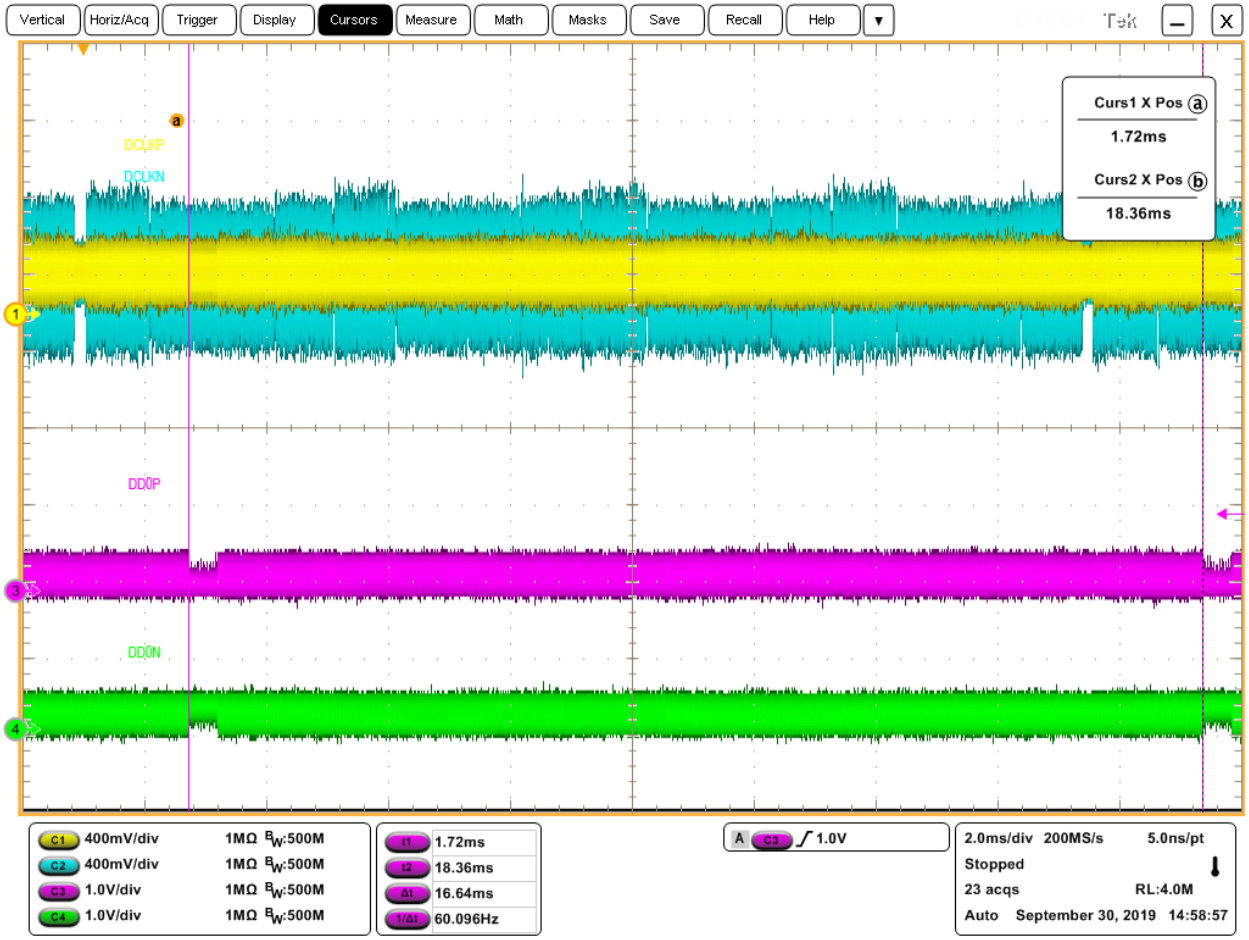

Figure 7: Improperly Configured DSI Waveforms (Data Always in HS Mode)

The DLPC343x controller does not support and will not work if the data lanes never enter LP mode. This can be seen by the DD0x lines always staying in differential mode and never entering 1.1V single ended mode.

Incorrect: Clock enters LP Mode

Figure 8: Improperly Configured DSI Waveforms (Clock Enters LP Mode)

As seen above the clock is entering LP mode (DCLK0P and DCLK0N go to a 1.1V single ended signal) during the vertical blanking time. This is not supported. The clock must always be a 200mV differential signal.

Nominal Timings

A DSI generator from The Moving Pixel Company was used to produce the waveforms shown above. The below screenshots from the DSI generator software is provided below.

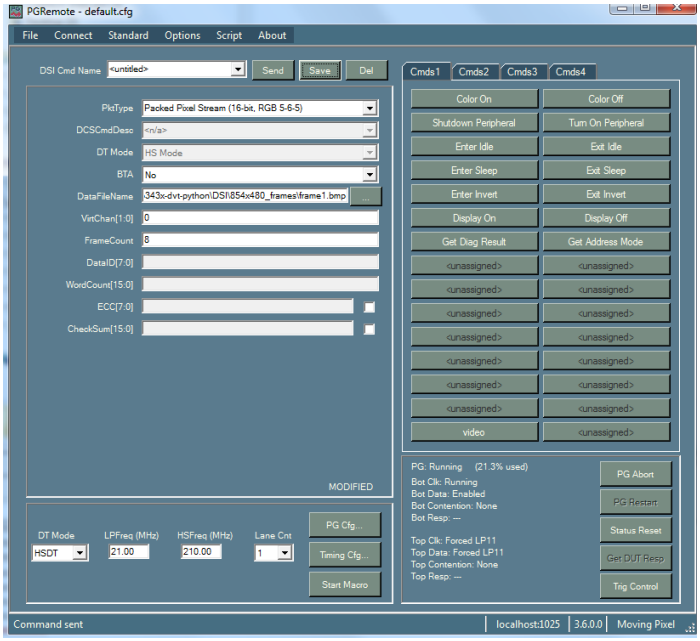

Figure 9: Nominal DSI Settings Overview

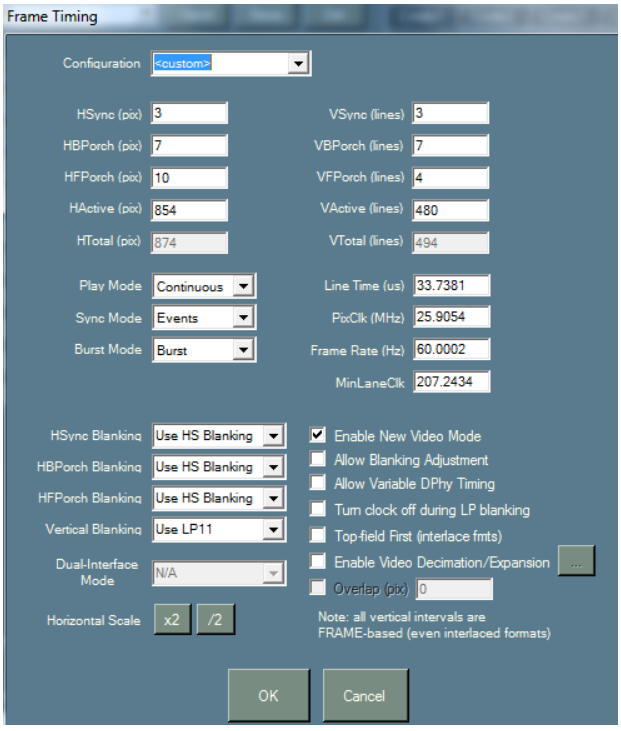

Figure 10: Nominal DSI Frame Timings

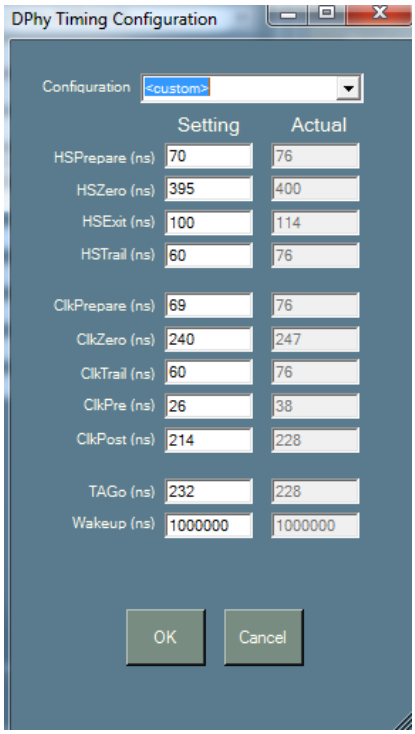

Figure 11: Nominal DSI DPhy Settings

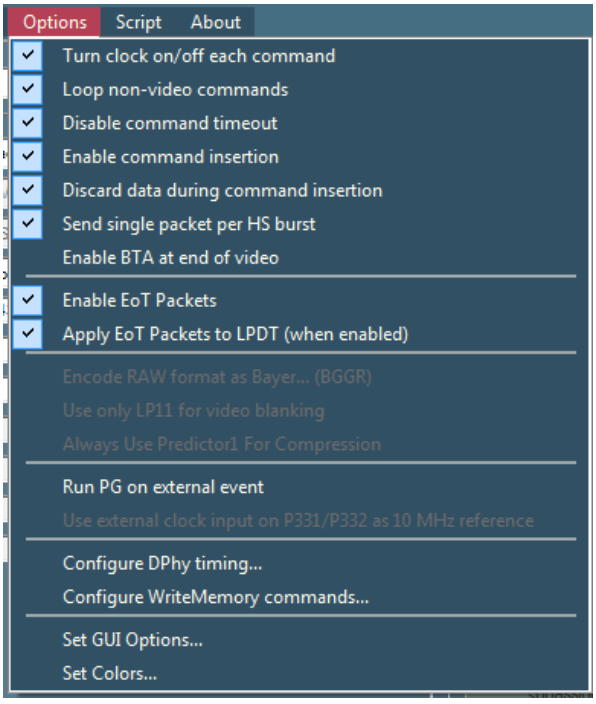

Figure 12: Nominal DSI Additional Settings

Debugging Checklist

Hardware Checks

- ☐ A DLPC3430 or DLPC3433 is used.
- ☐ Number of DSI lanes correctly configured using GPIO_01 and GPIO_02.
- ☐ RREF pin pulled-down to ground through a 30-kΩ ±1% resistor.
- ☐ VDD is between 1.045 V and 1.155 V
- ☐ VDDLP12 connected to VDD (main 1.1V power). It is also acceptable to tie this pin to a separate 1.2V signal.
- ☐ If VDDLP12 is from a separate supply, it is between 1.12 V and 1.28 V, powers-on after VDD, and powers-down before VDD

DSI Configuration Settings

- ☐ DSI clock frequency between 80 MHz and 235 MHz
- ☐ Data lanes between 1 and 4
- ☐ Command mode disabled
- ☐ EOT enabled
- ☐ BTA disabled
- ☐ LP mode during vertical blanking
- ☐ LP mode during vertical sync
- ☐ HS mode during horizontal blanking
- ☐ HS mode during horizontal sync
- ☐ Clock enabled during LP blanking
- ☐ DSI lines in LP11 until DLPC343x controller reset complete

DSI DPHY Settings

- ☐ Ths-prepare + ths-zero 565 ns minimum (465 ns minimum if DSI clock between 95 MHz and 235 MHz)
- ☐ Confirm remaining selected timings are within DPHY Spec. Specifically:
  - ths-exit
  - ths-trail
  - clk-prepare
  - clk-zero
  - clk-trail
  - clk-pre
  - clk-post
  - TAGo
- ☐ Use sample DPHY settings for debugging if needed from Example DSI Configuration and Timings

Video Settings

- One of the below pixel formats used
  - 24-bit RGB888 (3B per pixel)
  - 18-bit RGB666 (2+B per pixel)
  - 18-bit RGB666 (3B loosely packed)
  - 16-bit RGB565 (2B per pixel)
  - 16-bit 4:2:2 YCbCr (2B per pixel)
- PCLK between 1 and 155 MHz
- Horizontal input between 320 and 1280 pixels (assuming horizontal input video)
- Vertical Input between 200 and 800 pixels (assuming horizontal input video)
- Input frame rate between 10 and 120 Hz
- VSYNC High (VSYNC_WE) greater than 1 line
- Vertical back porch (VBP) greater than 2 lines
- Vertical front porch (VFP) greater than 1 line
- Total vertical blanking (TVB) greater than 14 lines (may need to be larger if source active lines per frame doesn't match DMD active lines per frame; see *Parallel Interface Frame Timing Requirements* in the controller datasheet for more info).
- HSYNC High (HSYNC_CS) between 4 and 128 PCLKs
- Horizontal back porch (HBP) greater than 4 PCLKs
- Horizontal front porch (HFP) greater than 8 PCLKs

DLPC343x Settings

- Startup the DLPC343x controller by pulling PROJ_ON high
- The following commands are executed (I2C or autoinit bath file):
  - *Write Image Crop (0x10): Select which portion of the input image is used*
  - *Write Display Size (0x12): Select size of active image to be displayed*
  - *Write Input Image Size (0x2e): Specify active data size of input image*
  - *Write DSI Port Enable (0xd7): Ensure the DSI port is enabled*
  - *Set DSI HS Clock input (0xBD):* Specify the high speed DSI clock
  - *Write Input Source Select (0x05)*: Set to external video
  - *Write External Video Source Format Select (0x07)*: Auto detect DSI format
- The DSI lines are in LP11 mode while the DLPC343x controller is initializing
- The DSI signal is sent after HOST_IRQ goes low

Additional Resources

- DLPC3430 Datasheet
- DLPC3433 Datasheet
- Programmer's guide for the DLPC343x
- DLPC3430 Product Folder
- DLPC3433 Product Folder
- DLP2010 Product Folder
- DLP3010 Product Folder
- DLPDLCR3010EVM-G2 Product Folder
- http://www.mipi.org/

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