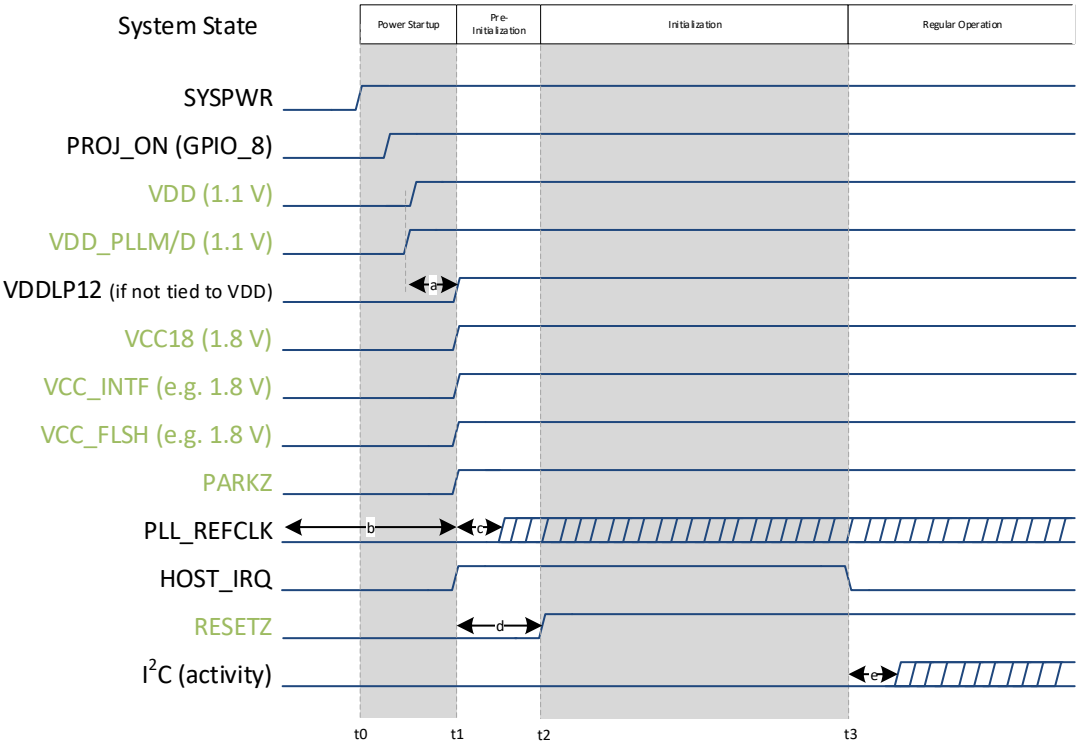
System Power-Up Timing Diagram



t0: SYSPWR applied to the PMIC. All other voltage rails are derived from SYSPWR
t1: All supplies reach 95% of their specified nominal value.
t2: Point where RESETZ is deasserted (goes high). This indicates the beginning of the controller auto-initialization routine.
t3: HOST_IRQ goes low to indicate initialization is complete.

a. VDDLP12 must be powered on after VDD if it is supplied from a separate source
b. PLL_REFCLK is allowed to be active before power is applied
c. PLL_REFCLK must be stable within 5ms of all power being applied. For external oscillator applications this is oscillator dependent, and for crystal applications this is crystal and controller oscillator cell dependent.
d. PARKZ must be high before RESETZ releases to support auto-initialization
e. I^2C activity cannot start until HOST_IRQ goes low to indicate auto-initialization is complete

Color Code:
From PMIC (e.g. DLPA3000)
From other source

Disclaimer: This timing diagram is a best estimate of the startup and has not been verified