Application Report
DLPA071–June 2016

PCB Design Requirements for TI DLP® Pico™ TRP Digital Micromirror Devices

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1 Scope

This document summarizes the PCB layout and PCB design requirements for systems utilizing a TRP digital micromirror device (DMD) in combination with any DLPC343x controller and either the DLPA200x or DLPA300x.

NOTE: The information in this document is not a substitute for the specifications listed in the corresponding device data sheets. In the event of a discrepancy, the data sheet supersedes this document.

WARNING

Failure to adhere to these design guidelines and/or the published device specifications can result in permanent damage to the devices.

2 Applicable Documents

The following TI Documents contain relevant information:

1. DLPC343x display controller datasheets, latest revision. Including DLPC3430, DLPC3433, DLPC3435, DLPC3438, and DLPC3439.
2. DLPA2000, DLPA2005, DLPA3000 and DLPA3005 PMIC datasheets, latest revision
3. DLP2010, DLP3010 and DLP4710 DMD datasheets, latest revision

3 Connectivity Guidelines

3.1 DMD Electrical Connections

Figure 1 shows the DLP2010 DMD and how it is driven in a DLP projection system.

- Data and control are provided by the DLPC3430 or the DLPC3435
- Power is supplied by the DLPA2000 or the DLPA2005

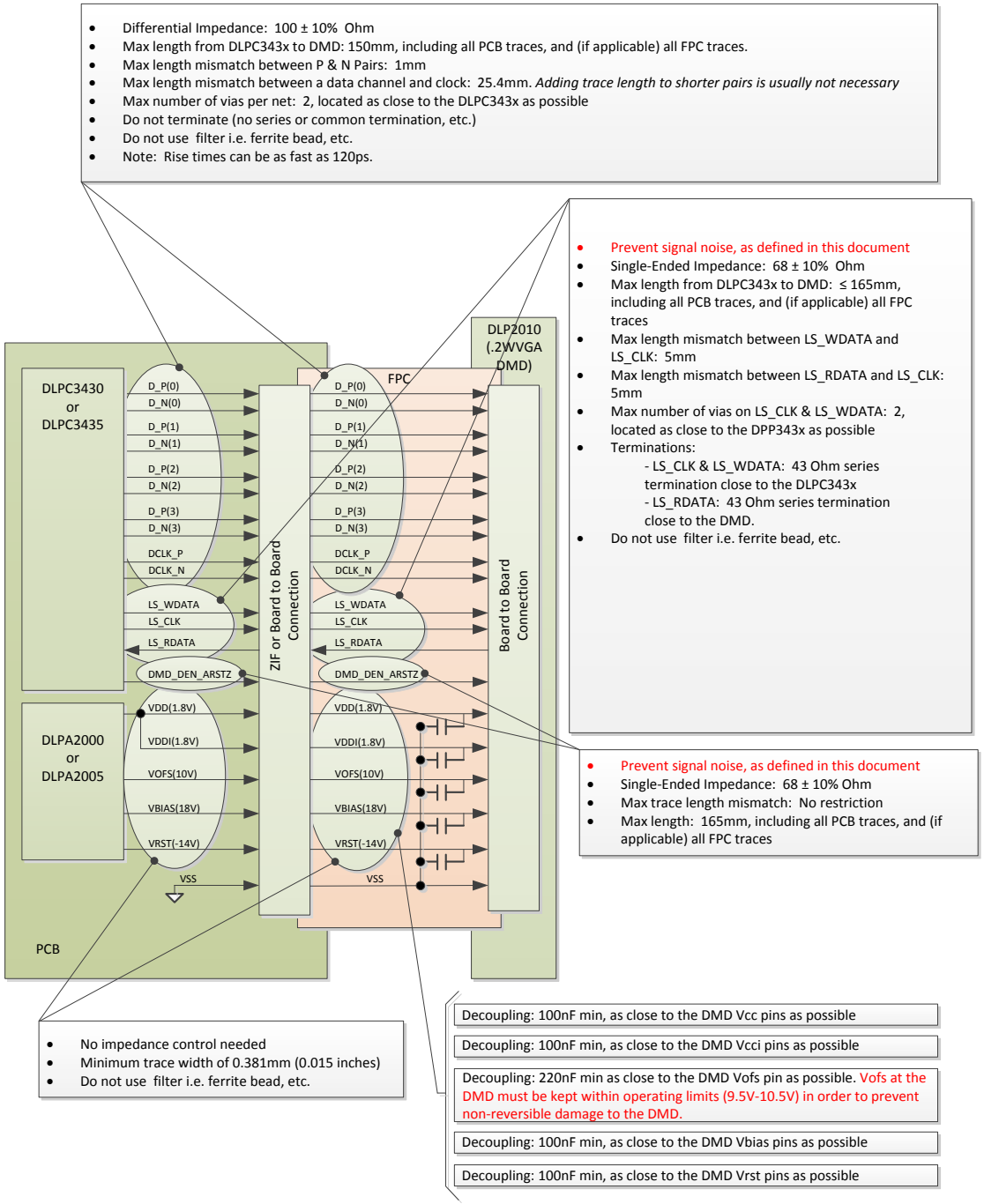

Figure 1. Layout Guidelines for the DLP2010 DMD

Figure 2 shows the DLP3010 DMD and how it is driven in a DLP projection system.

- Data and control are provided by the DLPC3433 or the DLPC3438
- Power is supplied by the DLPA2000, DLPA2005, or the DLPA3000

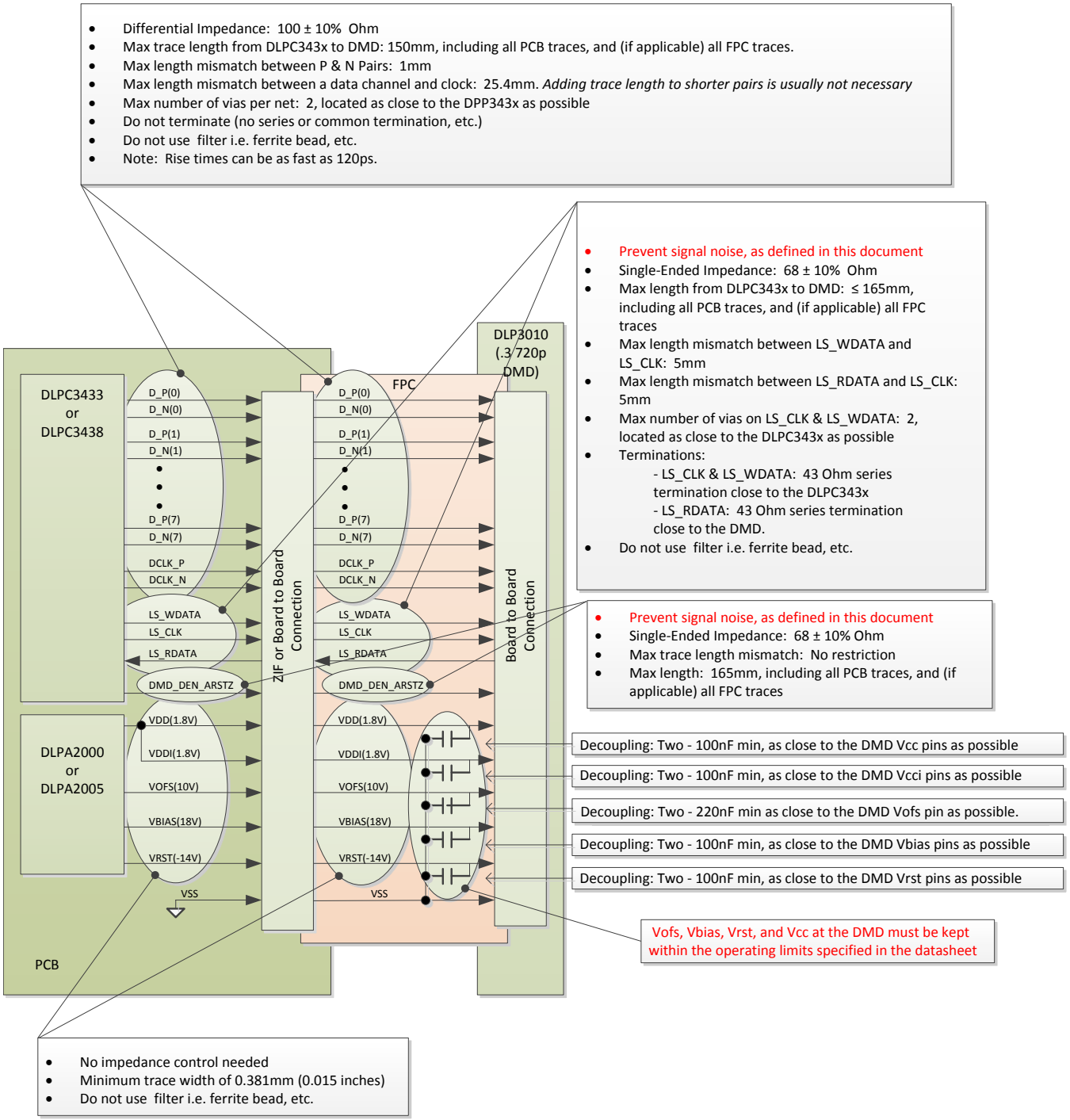

Figure 2. Layout Guidelines for the DLP3010 DMD

Figure 3 shows the DLP4710 DMD and how it is driven in a DLP projection system.

- Data and control are provided by two (2) separate DLPC3439
- Power is supplied by the DLPA3000 or DLPA3005

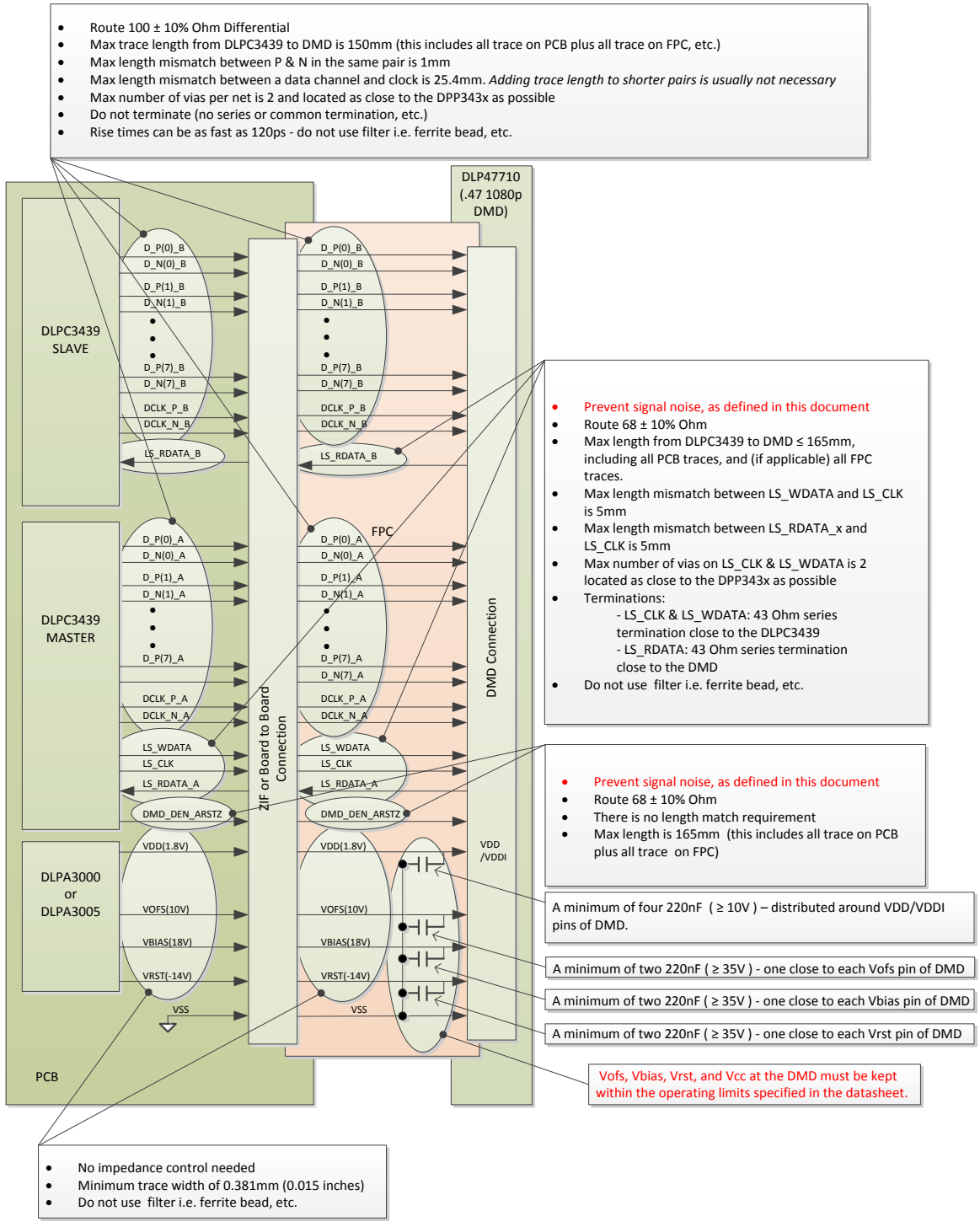

Figure 3. Layout Guidelines for the DLP4710 DMD

The guidelines in Figure 1, Figure 2, and Figure 3 are summaries taken from the DLPC343x datasheet, DLPA200x datasheet, DLPA300x datasheet, DLP2010 datasheet, DLP3010 datasheet and DLP4710 datasheet. For more detail and information, please refer to the individual device data sheets.

3.2 Power Connections

- V_{OFS}, V_{BIAS}, V_{RST}, V_{DD}, & V_{DDI} power rails (at the DLP2010, DLP3010, DLP4710) must be kept within the specified operating range. This includes effects from ripple and DC error.
  - To accommodate power supply transient current requirements, adequate decoupling capacitance must be placed near the DMD V_{OFS}, V_{BIAS}, V_{RST}, V_{DD}, & V_{DDI} pins
- To accommodate power supply transient current requirements, adequate decoupling capacitance must be placed near the DMD V_{OFS}, V_{BIAS}, V_{RST}, V_{DD}, & V_{DDI} pins.
- Never hot-swap the DMD. At the instant the DMD physical interface is connected or disconnected, all DMD power supply rails and signals must be at zero volts (not driven).
- Never allow power to be applied to the DMD when one or more DMD signal pins are not being driven.
- Adhere to the power-up and power-down procedures specified in the DMD datasheet, and never allow the DMD power supply levels to be outside of the *Recommended Operating Conditions* specified in the DMD datasheet.

3.3 Signal Noise Definition

During operation, it is critical to prevent the coupling of noise onto the LS bus and the DMD_DEN_ARSTZ signal. In this context, any of the following conditions are considered “noise”:

- Shorting to another signal
- Shorting to power
- Shorting to ground
- Intermittent connection, *which includes “hot-swapping”*
- An electrical “open” condition
- An electrical “floating” condition
- Inducing electromagnetic interference which is strong enough to affect the integrity of the signal(s)
- Unstable inputs (conditions outside the specified operating range) to any of the device power rails
- Voltage fluctuations on the device ground pins

4 DMD Power-up and Power-down

The manner in which the DMD is powered-up and powered-down is critical to its proper operation. The DLPA200x and DLPA300x are designed to provide the required power-up and power-down sequences, provided that the following conditions are met:

DLPA200x systems (see the DLPA2000 or DLPA2005 datasheet for details):

- **PROJ_ON transitioning high**: VIN and 1.8 V to LS_IN are in operating range.
- **PROJ_ON is high:** VIN and 1.8 V to LS_IN are in operating range.
- **PROJ_ON transitioning low (normal shutdown):** VIN and 1.8 V to LS_IN are in operating range for at least 35 ms plus the time it takes V_{OFS}, V_{BIAS} & V_{RST} to drop within 4 V of GND. (1)
- **PROJ_ON is high when UVLO fault occurs:** VIN and 1.8 V to LS_IN are in operating range for at least 35.5 µs (Vbias delay) + 4.4 µs (Vofs delay) + the time it takes V_{OFS}, V_{BIAS} & V_{RST} to drop within 4 V of GND.

DLPA300x systems (see the DLPA3000 or DLPA3005 datasheet for details):

- **PROJ_ON transitioning high:** VIN is in operating range.
- **PROJ_ON is high:** VIN is in operating range while PROJ_ON is high.
- **PROJ_ON transitioning low (normal shutdown):** VIN is in operating range for at least 35 ms plus the time it takes V_{OFS}, V_{BIAS} & V_{RST} to drop within 4 V of GND.
- **PROJ_ON is high when UVLO fault occurs:** VIN is in operating range for at least 35.5 µs (Vbias delay) + 4.4 µs (Vofs delay) + the time it takes V_{OFS}, V_{BIAS} & V_{RST} to drop within 4 V of GND.

(1) The time it takes V_{OFS}, V_{BIAS} & V_{RST} to drop from operating levels to within 4 V of GND is system dependent. It is expected that the user determine this value for every design.

5 Manufacturing Best Practices

In order to prevent possible DMD failures during system manufacturing, it is recommended that the following "best practices" be followed:

- Any device electrically interfacing to the DMD must follow all of the guidelines specified in this document and in the applicable datasheets. This includes cabling, test electronics, power distribution, on/off procedure, DMD connect/disconnect, etc.
- All connectors have an insertion and removal life. Insertion and removal cycles for connectors between the DLPC343x and the DMD should not exceed the manufacturers stated lifetime maximum.
  - The DLP2010 can mate to two (2) different connectors. The AXT540124 has an insertion/removal life of 50 cycles, which is suitable for use in end-products. The AXT5E4026 has an insertion/removal life of 3000 cycles, which is suitable for factory equipment.
- As with FPCs used in a product, any and all FPCs used in the factory should be designed in accordance with the guidelines specified in this document and in the applicable datasheets.
- Optical engine production is typically a manual process requiring a human operator to connect the DMD, power on, assemble/test, power down, and disconnect. Every time this cycle is performed there is a possibility of an operator error, such as:
  - Powering on before connecting the DMD (hot plug).
  - Disconnecting the DMD before powering down (hot unplug).
  - Not fully mating the DMD to the test electronics.

It is recommended to keep the number of assembly/test stations where the DMD is power cycled to a minimum. This will reduce the probability of damage to the DMD due to operator error.

6 Abbreviations

PCB - Printed Circuit Board

FPC - Flexible Printed Circuit

DMD - Digital Micromirror Device

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