DLP® PICO Processor 2607 ASIC

Check for Samples: DLPC2607

FEATURES

- Supports Reliable Operation of the .2 nHD, .24 VGA, and .3 WVGA DMDs
- Multi-Mode, 24-Bit Input Pixel Interfaces:
  - Supports Parallel or BT656 Bus Protocol
  - Supports Input Sizes From QVGA Through WVGA
  - Supports 1 to 60-Hz Frame Rates
  - Supports Pixel Clock up to 33.5 MHz
  - Supports Landscape and Portrait Orientations
  - Support 8, 16, 18, and 24-Bit Bus Options
  - Supports 3 Input Color Bit-Depth Options:
    - RGB888, YCrCb888
    - RGB666, YCrCb666
    - RGB565, 4:2:2 YCrCb
- Pixel Data Processing:
  - Image Resizing (Scaling)
  - Frame Rate Conversion
  - Color Coordinate Adjustment
  - Automatic Gain Control
  - Programmable Degamma
  - Spatial-Temporal Multiplexing (Dithering)
  - Video Processing Support:
    - Color Space Conversion
    - 4:2:2 to 4:4:4 Chroma Interpolation
    - Field Scaled De-interlacing
- Packaged in a 176-Pin, 0.4-mm Pitch, VFBGA
- External Memory Support:
  - 166-MHz Mobile DDR SDRAM
  - 33.3-MHz Serial FLASH
- WVGA, VGA, and nHD DMD Display Support
  - DMD Bit-Plane Generation and Formatting
  - Programmable Bit-Plane Display Sequencer (Controls the LED Enables and DMD Loading)
  - 76.2-MHz Double Data Rate (DDR) DMD I/F
  - Pulse-Width Modulation (PWM) for Mirrors:
    - Auto DMD Parking at Power-Down
    - 24-Bit Bit-Depth on DMD
- System Control:
  - I^2C Control of Device Configuration
  - Programmable Splash Screens
  - Programmable LED Current Control
  - DMD Power and Mirror Driver Control
  - DMD Horizontal and Vertical Display Image Flip
  - Display Image Rotation
  - Flash-Based Configuration Batch Files
  - I/F Sleep Still Image Power Savings Mode
- Test Support:
  - Built-in Test Pattern Generation
  - JTAG With Boundary Scan Test Support

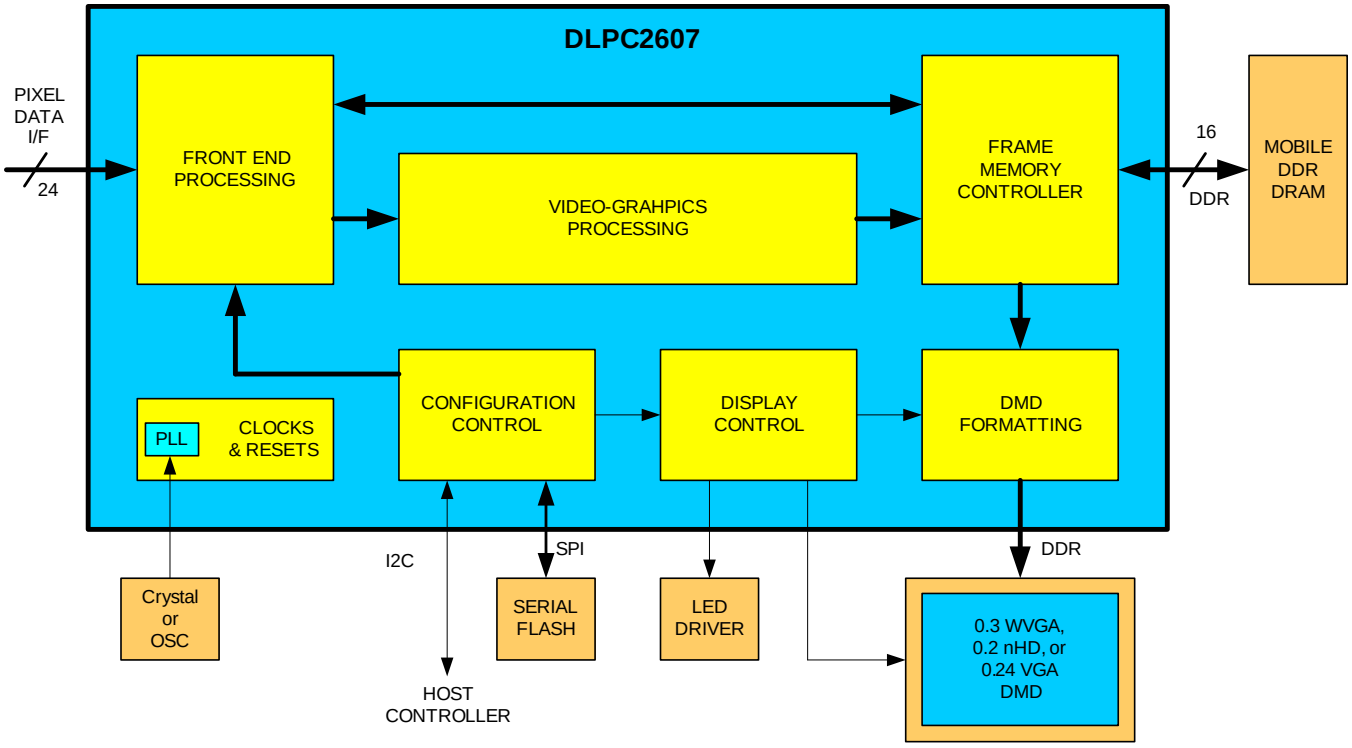
APPLICATIONS

- Embedded Mobile Projection
  - Smartphone
  - Tablet
  - Camera
  - Laptop
- Mobile Accessories
- Wearable (Near-Eye) Displays
- Battery-Operated Projectors
- Digital Signage

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION

The DLPC2607 is a low-power DLP digital controller for battery-powered display applications. The controller performs the image processing and display control necessary to support the .3 WVGA, .24 VGA, and .2 nHD DMDs. The DLPC2607 device can be used in systems where the projection display is embedded in a mobile device, as well as in accessory systems.



Accessory System Application

A typical accessory projector application is shown in Figure 1. For this application, the DLPC2607 device is controlled by a separate control processor (typically a MSP430) and the image data is received from a TVP5151 video decoder device. For this application, the ASIC only supports periodic sources.

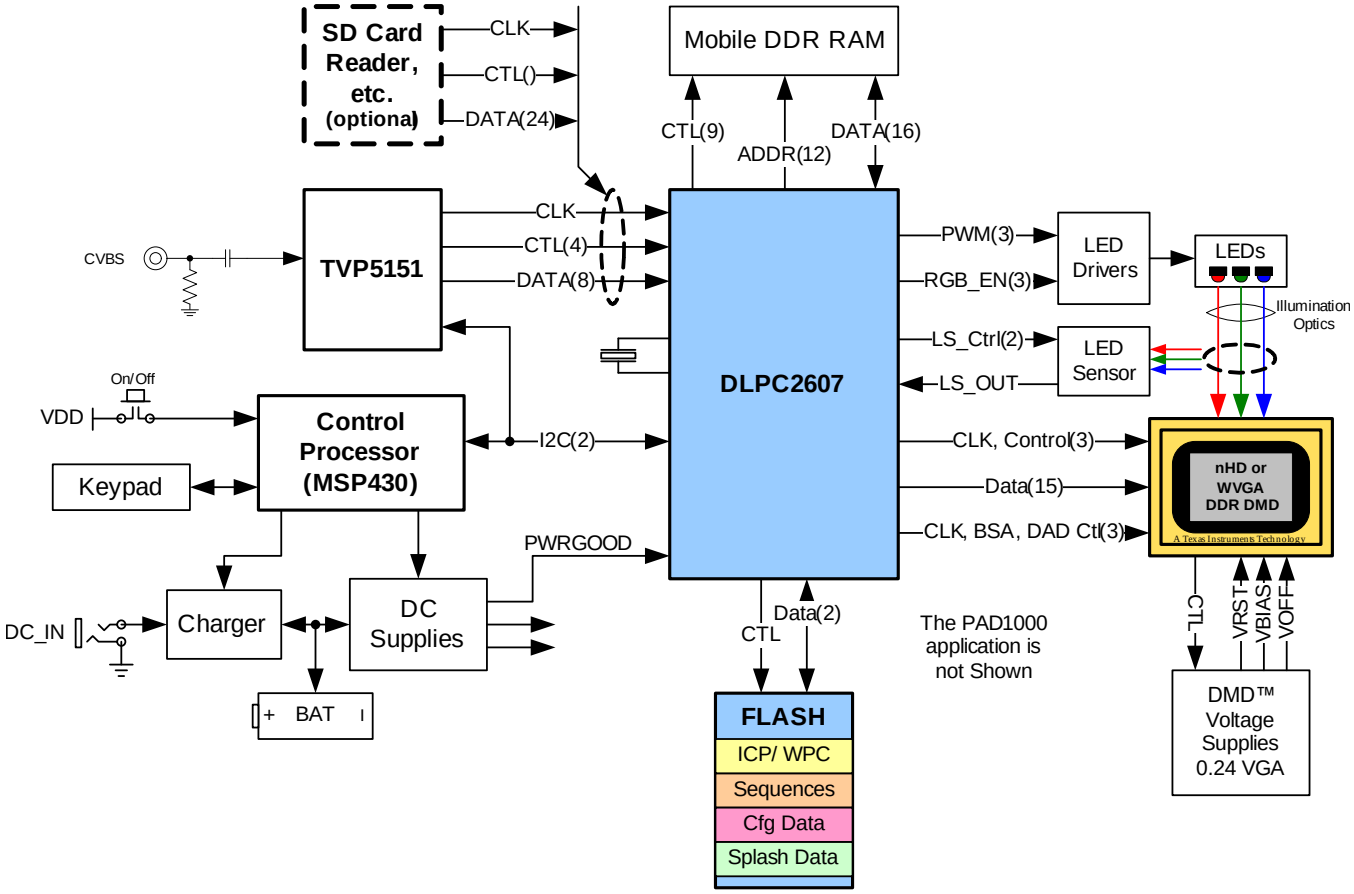


Figure 1. Typical Standalone Projector System Block Diagram

Embedded System Application

Figure 2 shows a typical embedded projection system using the DLPC2607 device. In this application, the DLPC2607 device receives control and data from the processor chip of the main mobile device (for example: a smartphone, tablet, or so forth) and supports both still and motion video sources. To support still images, the ASIC uses a triple-buffer arrangement for the formatter bit-plane buffer with a free-running sequence to maintain the display rate. The triple-buffer allows the source frame to be captured, then synchronously realigned to the free-running output display rate. To support motion video, the ASIC provides an option to synchronize the display update rate to the source.

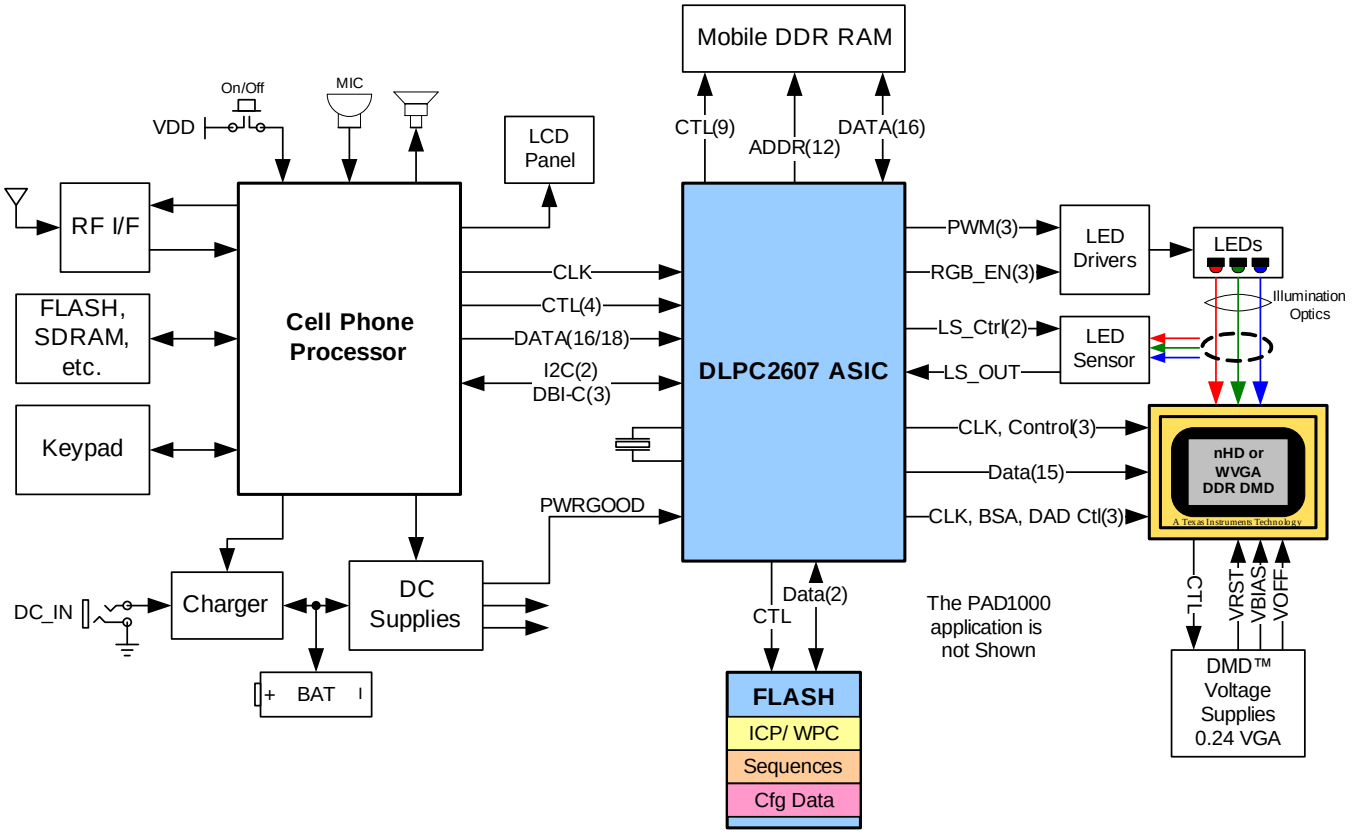


Figure 2. Typical Embedded System Block Diagram

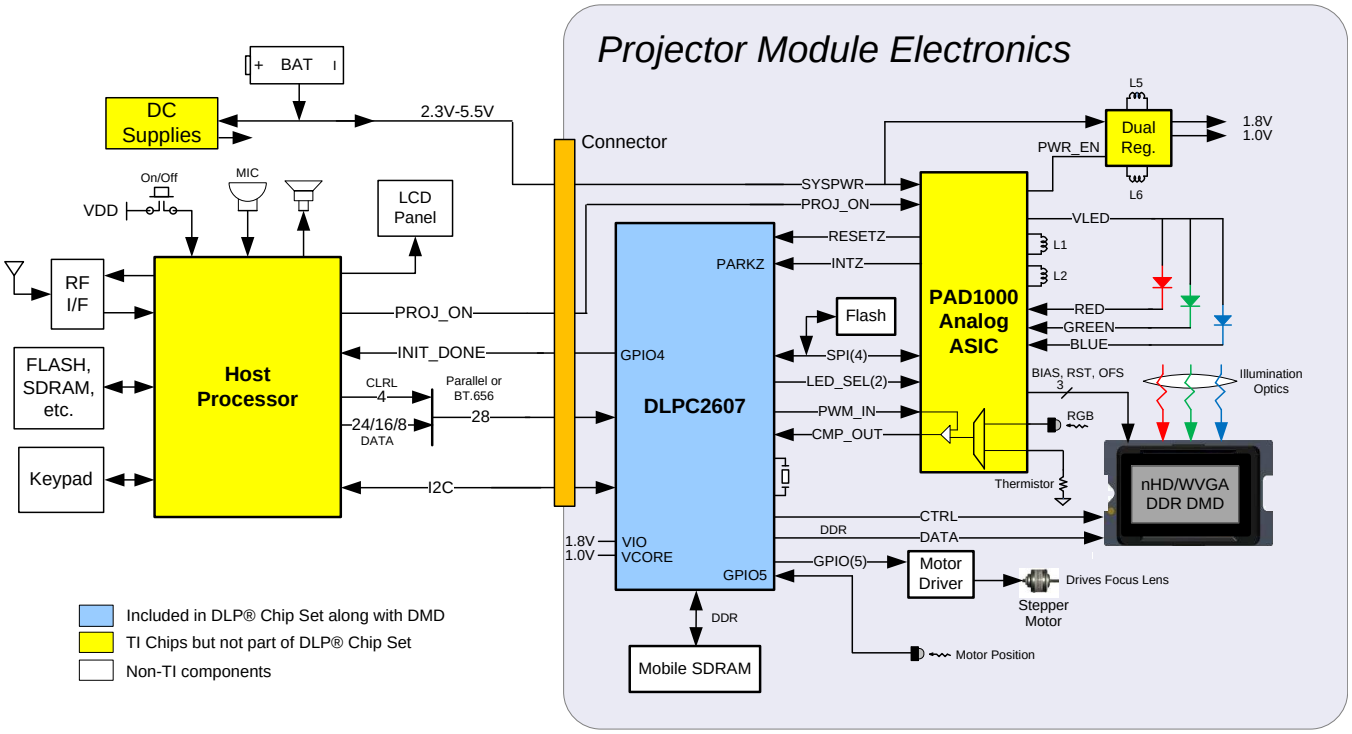


Figure 3. Typical Embedded System Block Diagram When Using a PAD1000

As with prior DLP® electronics solutions, image data is 100% digital from the DLPC2607 device input port to the image projected on to the display screen. The image stays in digital form and is never converted into an analog signal. The DLPC2607 device processes the digital input image and converts the data into bit-plane format as needed by the DMD. The DMD then reflects light to the screen using binary pulse-width modulation (PWM) for each pixel mirror. The viewer's eyes integrate this light to form brilliant, crisp images.

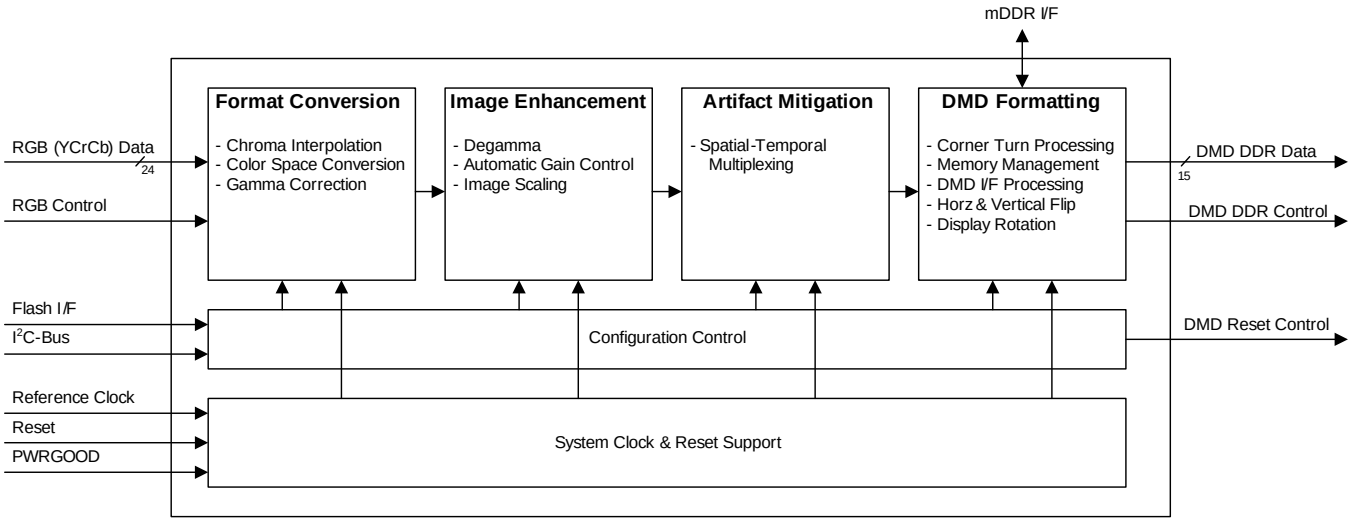


Figure 4. DLPC2607 Functional Block Diagram

Signal Functional Descriptions

This section describes the input and output characteristics of signals that interface to the DLPC2607 device by functional groups. The table includes I/O power and type characteristic references, which are further described in subsequent sections.

Table 1. DLPC2607 Functional Pin Descriptions(1)

Pin		I/O		Clock	Device Initialization and Reference Clock
Name	No.	Power	Type	System	Description
RESETZ	J14	VCC18	I1	Async	DLPC2607 Power-On Reset. Self-configuration starts when a low-to-high transition is detected on this pin. All ASIC power and clocks must be stable before this reset is de-asserted. (Hysteresis buffer) Note that the following seven signals are 3-stated while $\overline{\text{RESET}}$ is asserted: DMD_PWR_EN, LEDDVR_ON, LED_SEL_0,LED_SEL_1, SPICLK, SPIDOUT, SPICSZ0 External pullups or downs should be added as needed to these signals to avoid floating inputs where these signals are driven.
PLL_REFCLK_I	K15	VCC18 (filter)	I4	N/A	Reference Clock Crystal Input. If an external oscillator is used in place of a crystal, then this pin should be used as the oscillator Input.
PLL_REFCLK_O	J15		O14	N/A	Reference Clock Crystal Return. If an external oscillator is used in place of a crystal, then this pin should be left unconnected (floating).

(1) Each device connected to the SPI bus must be operated off VCC_FLSH

Table 2. (1)

Pin		I/O		Clock	Flash Interface
Name	**No.**	**Power**	**Type**	**System**	**Description**
SPICLK	A4	VCC_ FLSH	O24	N/A	Clock for the external SPI device or devices
SPIDIN	B4		I2	SPICLK	Serial Data input from the external SPI device or devices
SPICSZ0	A5		O24	SPICLK	Chip Select 0 output for the external SPI Flash device. Active low
SPICSZ1	C6		O24	SPICLK	Chip Select 1 output for the external SPI PAD1000 device. Active low
SPIDOUT	C5		O24	SPICLK	Serial Data output to the external SPI device or devices. This pin sends address and control information as well as data when programming

(1) Each device connected to the SPI bus must be operated off VCC_FLSH

Table 3.

Pin		I/O		Clock	Main Video Data and Control
Name	**No.**	**Power**	**Type**	**System**	**Description**
$\overline{\text{PARK}}$	B8	VCC_ INTF	I3	Async	DMD Park Control (active low) is set high to enable typical operation. It should be set high prior to releasing $\overline{\text{RESET}}$, or within 500 µs after releasing $\overline{\text{RESET}}$. It should be set low a minimum of 500 µs before any power is to be removed from the DLPC2607. (Hysteresis buffer).
LED_ENABLE	A11		I3	Async	LED Enable (active high input). A logic low on this signal forces LEDDRV_ON low and LED_SEL(1:0) = b00. These signals are enabled 100 ms after LED_ENABLE transitions from low to high. (Hysteresis buffer).
DBIC_CSZ	B10		I3	SCL	UNUSED/ RESERVED (DBI-C Chip Select): Should be pulled-up to VCC_INTF.
SCL	A10		B38	N/A	I^2C Clock (hysteresis buffer) bidirectional, open-drain signal. An external pullup is required. No I^2C activity is permitted for a minimum of 100 ms after $\overline{\text{PARK}}$ and $\overline{\text{RESET}}$ are set high.
SDA	C10		B38	SCL	I^2C Data (hysteresis buffer) bidirectional, open-drain signal. An external pullup is required.
GPIO4_INTF	C9		B34	Async	General Purpose I/O 4 (Hysteresis buffer) Primary usage is to indicate when auto-initialization is complete (also referred to as INIT-DONE - which is when GPIO4 transitions high then low following release of $\overline{\text{RESET}}$) and to flag a detected error condition in the form of a logic high, pulsed Interrupt flag subsequent to INIT-DONE.
GPIO5_INTF	B9		B34	Async	General Purpose I/O 5 (Hysteresis buffer) For applications that use focus motor control with a sensor: This pin is an input that is connected to the motor position sensor. For applications that use non-focus motor control with a sensor: This pin should be configured to be an output at logic 0 and left unconnected.

Table 4.

Pin		I/O		Clock	Main Video Data and Control	
					Description	
Name	No.	Power	Type	System	Parallel RGB Mode	BT.656 I/F Mode
PCLK (Hysteresis)	D13	VCC_ INTF	I3	N/A	Pixel Clock (1)	Pixel Clock (1)
PDM_CVS_TE	H15		B34	ASYNC	Parallel Data Mask (2)	Unused (3)
VSYNC_WE	H14		I3	ASYNC	Vsync (4)	Unused (3)
HSYNC_CS	H13		I3	PCLK	Hsync (4)	Unused (3)
DATEN_CMD	G15		I3	PCLK	Data Valid (4)	Unused (3)
PDATA[0]	G14		I3	PCLK	Data (5)	Data0 (5)
PDATA[1]	G13		I3	PCLK	Data (5)	Data1 (5)
PDATA[2]	F15		I3	PCLK	Data (5)	Data2 (5)
PDATA[3]	F14		I3	PCLK	Data (5)	Data3 (5)
PDATA[4]	F13		I3	PCLK	Data (5)	Data4 (5)
PDATA[5]	E15		I3	PCLK	Data (5)	Data5 (5)
PDATA[6]	E14		I3	PCLK	Data (5)	Data6 (5)
PDATA[7]	E13		I3	PCLK	Data (5)	Data7 (5)
PDATA[8]	D15		I3	PCLK	Data (5)	Unused (3)
PDATA[9]	D14		I3	PCLK	Data (5)	Unused (3)
PDATA[10]	C15		I3	PCLK	Data (5)	Unused (3)
PDATA[11]	C14		I3	PCLK	Data (5)	Unused (3)
PDATA[12]	C13		I3	PCLK	Data (5)	Unused (3)
PDATA[13]	B15		I3	PCLK	Data (5)	Unused (3)
PDATA[14]	B14		I3	PCLK	Data (5)	Unused (3)
PDATA[15]	A15		I3	PCLK	Data (5)	Unused (3)
PDATA[16]	A14		I3	PCLK	Data (5)	Unused (3)
PDATA[17]	B13		I3	PCLK	Data (5)	Unused (3)
PDATA[18]	A13		I3	PCLK	Data (5)	Unused (3)
PDATA[19]	C12		I3	PCLK	Data (5)	Unused (3)
PDATA[20]	B12		I3	PCLK	Data (5)	Unused (3)
PDATA[21]	A12		I3	PCLK	Data (5)	Unused (3)
PDATA[22]	C11		I3	PCLK	Data (5)	Unused (3)
PDATA[23]	B11		I3	PCLK	Data (5)	Unused (3)

(1) Pixel Clock capture edge is software programmable.
(2) Data Mask is optional for parallel bus operation. If unused, it should be pulled to ground through a resistor.
(3) Unused inputs should be pulled-down to ground through an external resistor.
(4) VSYNC, HSYNC, and Data Valid polarity is software programmable.
(5) PDATA(23:0) bus mapping is pixel format and source mode dependent. For details, see later sections.

Table 5. (1)

Pin		I/O		Clock	DMD Interface
Name	**No.**	**Power**	**Type**	**System**	**Description**
DMD_D0	M15	VCC18	O58	DMD_DCLK	DMD Data Pins. DMD Data pins are double data rate (DDR) signals that are clocked on both edges of DMD_DCLK. All 15 DMD data signals are use to interface to the WVGA and VGA DMDs; however, only 12 of the 15 are used to interface to an nHD DMD. The standard nHD interconnect is to utilize pins DMD_D(11:0). However, DMD_D(14:3) must be used to interface to the nHD DMD when the I^2C programmable option to reverse the bit-order of the DMD interface pins is selected (DMD Bus Swap Control, I^2C: 0xA7).
DMD_D1	N14				
DMD_D2	M14				
DMD_D3	N15				
DMD_D4	P13				
DMD_D5	P14				
DMD_D6	P15				
DMD_D7	R15				
DMD_D8	R12				
DMD_D9	N11				
DMD_D10	P11				
DMD_D11	R11				
DMD_D12	N10				
DMD_D13	P10				
DMD_D14	R10				
DMD_DCLK	N13			N/A	DMD Data Clock (DDR)
DMD_LOADB	R13			DMD_DCLK	DMD Data Load Signal (active low). This signal requires an external pullup to VCC18.
DMD_SCTRL	R14			DMD_DCLK	DMD Data Serial Control Signal
DMD_TRC	P12			DMD_DCLK	DMD Data Toggle Rate Control
DMD_DAD_BUS	L13			DMD_SAC_CLK	DMD DAD Bus Data
DMD_DAD_STRB	K13			DMD_SAC_CLK	DMD DAD Bus Strobe
DMD_DAD_OEZ	M13			Async	DMD Reset Driver Output Enable (active low). To properly park the DMD, this signal requires a 30-kΩ to 100-kΩ external pullup resistor connected to VCC18.
DMD_SAC_BUS	L14			DMD_SAC_CLK	DMD SAC Bus Data
DMD_SAC_CLK	L15			N/A	DMD SAC Bus Clock

(1) Each device connected to the SPI bus must be operated off VCC_FLSH

Table 6.

Pin		I/O		Clock	SDRAM Interface
Name	**No.**	**Power**	**Type**	**System**	**Description**
MEM0_CLK_P	D1	VCC18	O74	N/A	mDDR memory, Differential Memory Clock
MEM0_CLK_N	E1		O74		
MEM0_A0	P1		O64	MEM_CLK	mDDR memory, Multiplexed Row, and Column Address
MEM0_A1	R3				
MEM0_A2	R1				
MEM0_A3	R2				
MEM0_A4	A1				
MEM0_A5	B1				
MEM0_A6	A2				
MEM0_A7	B2				
MEM0_A8	D2				
MEM0_A9	A3				
MEM0_A10	P2				
MEM0_A11	B3				
MEM0_A12	D3				
MEM0_BA0	M3				mDDR memory, Bank Select
MEM0_BA1	P3				
MEM0_RASZ	P4				mDDR memory, Row Address Strobe (active low)
MEM0_CASZ	R4				mDDR memory, Column Address Strobe (active low)
MEM0_WEZ	R5				mDDR memory, Write Enable (active low)
MEM0_CSZ	J3				mDDR memory, Chip Select (active low)
MEM0_CKE	C1				mDDR memory, Clock Enable (active high)
MEM0_LDQS	J2		B64	N/A	mDDR memory, Lower Byte, R/W Data Strobe
MEM0_LDM	J1		O64	MEM0_LDQS	mDDR memory, Lower Byte, Write Data Mask
MEM0_DQ0	N1		B64	MEM0_LDQS	mDDR memory, Lower Byte, Bidirectional R/W Data
MEM0_DQ1	M2				
MEM0_DQ2	M1				
MEM0_DQ3	L3				
MEM0_DQ4	L2				
MEM0_DQ5	K2				
MEM0_DQ6	L1				
MEM0_DQ7	K1				
MEM0_UDQS	G1		B64	N/A	mDDR memory, Upper Byte, R/W Data Strobe
MEM0_UDM	H1		O64	MEM0_UDQS	mDDR memory, Upper Byte, Write Data Mask
MEM0_DQ8	H2		B64	MEM0_UDQS	mDDR memory, Upper Byte, Bidirectional R/W Data
MEM0_DQ9	G2				
MEM0_DQ10	H3				
MEM0_DQ11	F3				
MEM0_DQ12	F1				
MEM0_DQ13	E2				
MEM0_DQ14	F2				
MEM0_DQ15	E3				

Table 7.

Pin		I/O		Clock	LED Driver Interface	
Name	**No.**	**Power**	**Type**	**System**	**Description**	
GPIO1_RPWM	N8	VCC18	O14	Async	General Purpose I/O 1 (Output only). If the PAD1000 is not used, then this output must be used as the Red LED PWM signal used to control the LED current.(1) If the PAD1000 is used, then this output can be used as a general purpose output controlled by the WPC processor.	
GPIO2_GPWM	P9		O14	Async	General Purpose I/O 2 (Output only). If the PAD1000 is not used, then this output must be used as the Green LED PWM signal used to control the LED current.(1) If the PAD1000 is used, then this output can be used as a general purpose output controlled by the WPC processor.	
GPIO3_BPWM	R8		O14	Async	General Purpose I/O 3 (Output only). If the PAD1000 is not used, then this output must be used as the Blue LED PWM signal used to control the LED current.(1) If the PAD1000 is used, then this output can be used as a general purpose output controlled by the WPC processor.	
LED_SEL_0	R6		O14	Async	LED Enable SELECT. Controlled by programmable DMD Sequence Timing. (Hysteresis buffer).	
LED_SEL_1	N6		O14	Async	LED_SEL(1:0)	Selected LED
					00	None
					01	Red
					10	Green
					11	Blue
					These outputs should be input directly to the PAD1000 if used. If the PAD1000 is not used, then a decode circuit is required to decode the selected LED enable.	
LEDDRV_ON	P7		O14	Async	LED Driver Enable. Active high output control to external LED Driver Logic (master enable). Is driven high 100 ms after LED_ENABLE is driven high. Driven low immediately when either LED_ENABLE or $\overline{\text{PARK}}$ is driven low.	
DMD_PWR_EN	K14		O14	Async	DMD Power Regulator Enable (active high). This is an active high output that should be used to control DMD V_{OFFSET}, V_{BIAS}, and V_{RESET} voltages. DMD_PWR_EN is driven high as a result of the $\overline{\text{PARK}}$ input signal being set high. However, DMD_PWR_EN is held high for 500 µs after the $\overline{\text{PARK}}$ input signal is set low before it is driven low. TI recommends a weak external pulldown resistor to keep this signal at a known state during power-up reset.	

(1) The PAD1000 is not available for initial DLPC2607 design applications. When the PAD1000 is NOT used, all LED PWM signals are forced high when LEDDRV_ON = 0, software LED control is disabled or the sequence stops.

Table 8.

Pin		I/O		Clock	White Point Correction Light Sensor I/F
Name	**No.**	**Power**	**Type**	**System**	**Description**
CMP_OUT	A6	VCC_ 18	I1	Async	Successive Approximation ADC Comparator Output (DLPC2607 Input). Assumes a successive approximation ADC is implemented with either a Light Sensor or Thermo-couple or both feeding one input of an external Comparator and the other side of the Comparator driven from the CMP_PWM pin of the ASIC. It should be pulled-down to ground if this function is not used. (Hysteresis buffer)
CMP_PWM	B7		O14	Async	Successive Approximation Comparator Pulse-Width Modulation Input. Supplies a PWM signal to drive the successive approximation ADC Comparator used in Light-to-Voltage light sensor applications. It should be left unconnected if this function is not used.
GPIO0_CMPPWR	P5		B14	Async	Power control signal for the WPC light sensor and other analog support circuits using the DLPC2607 ADC. Alternately, it provides General Purpose Input or Output I/O to the WPC microprocessor internal to the DLPC2607 device. It should be left unconnected if not used. (Hysteresis buffer)

Table 9.

Pin		I/O		Clock	White Point Correction Light Sensor I/F
Name	**No.**	**Power**	**Type**	**System**	**Description**
HWTEST_EN	A9	VCC _INTF	I3	N/A	Manufacturing Test Enable signal. Should be connected directly to ground on the PCB for typical operation. Includes weak internal pulldown.

Table 10.

Pin		I/O		Clock	White Point Correction Light Sensor I/F
Name	**No.**	**Power**	**Type**	**System**	**Description**
JTAGTDI	P6	VCC _18	I1	JTAGTCK	JTAG, Serial Data In. Includes weak internal pullup. (When JTAGRSTZ is held low, this input can be used as ICP/ WPC debug port RXD.)
JTAGTCK	N5			N/A	JTAG, Serial Data Clock. Includes weak internal pullup.
JTAGTMS	N7			JTAGTCK	JTAG, Test Mode Select. Includes weak internal pullup.
JTAGTDO	R7		O14	JTAGTCK	JTAG, Serial Data Out
JTAGRSTZ	P8		I1	ASYNC	JTAG, RESET (active low). Includes weak internal pullup. This signal must be tied to ground, through an external ≤ 15-kΩ resistor, for typical operation.

Table 11.

Pin		I/O		Clock	Test and Debug Interfaces	
Name	**No.**	**Power**	**Type**	**System**	**Description**	
TSTPT_0	B6	VCC18	B18	Async	Test Pin 0 – Sampled as an input test mode selection control upon release of $\overline{\text{RESET}}$, and then driven as an output. Includes weak internal pulldown. (1) **Normal use**: Reserved for test output (ICP/ WPC debug port TXD). Should be left open or unconnected for typical use. **Alternative use**: If focus motor control is used, this pin is used as the motor driver chip enable. An external pullup should not be applied to this pin to avoid putting the DLPC2607 device in a test mode.	
TSTPT_1	A8	VCC18	B18	Async	Test Pin 1 – Sampled as an input test mode selection control upon release of $\overline{\text{RESET}}$, and then driven as an output. Includes weak internal pulldown.(1) **Normal use**: Reserved for test output. Should be left open or unconnected for typical use. **Alternative use**: If focus motor control is used, this pin is used as the motor driver data bit1 (LSB). An external pullup should not be applied to this pin to avoid putting the DLPC2607 device in a test mode.	
TSTPT_2	C7	VCC18	B18	Async	Test Pin 2 – Sampled as an input test mode selection control upon release of $\overline{\text{RESET}}$, and then driven as an output. Includes weak internal pulldown.(1) **Normal use**: Reserved for test output. Should be left open or unconnected for typical use. **Alternative use**: If focus motor control is used, this pin is used as the motor driver motor driver data bit2. An external pullup should not be applied to this pin to avoid putting the DLPC2607 device in a test mode.	
TSTPT_3	B5	VCC18	B18	Async	Test Pin 3 – Sampled as an input test mode selection control upon release of $\overline{\text{RESET}}$, and then driven as an output. Includes weak internal pulldown.(1) **Normal use**: Reserved for test output. Should be left open or unconnected for typical use. **Alternative use**: If focus motor control is used, this pin is used as the motor driver motor driver data bit3. An external pullup should not be applied to this pin to avoid putting the DLPC2607 device in a test mode.	
TSTPT_4	A7	VCC18	B18	Async	Test Pin 4 – Sampled as an input test mode selection control upon release of $\overline{\text{RESET}}$, and then driven as an output. Includes weak internal pulldown.(1) **Normal use**: Reserved for test output. Should be left open or unconnected for typical use. **Alternative use**: If focus motor control is used, this pin is used as the motor driver data bit4 (MSB). An external pullup should not be applied to this pin to avoid putting the DLPC2607 device in a test mode.	
					Without External Pullup (1)	With External Pullup (2)
					Enables auto-initialization from flash	Disables auto-initialization and facilitates flash programming via I^2C of a blank flash
TSTPT_5	C8	VCC18	B18	Async	Test Pin 5 – Sampled as an input test mode selection control upon release of $\overline{\text{RESET}}$ and then driven as an output. Includes weak internal pulldown.(1) **Normal use**: Reserved for test output. Should be left open or unconnected for typical use. **Alternative use**: Not yet defined. An external pullup should not be applied to this pin to avoid putting the DLPC2607 device in a test mode.	
TSTPT_6	N9	VCC18	B18	Async	Test Pin 6 and PLL REFCLK Frequency Selection – Sampled as an input test mode selection control upon release of $\overline{\text{RESET}}$ and then driven as an output. Includes weak internal pulldown.(1) **Normal use**: Reserved for test output. Should be left open or unconnected for typical use. **Alternative use**: Not yet defined. This pin is sampled upon de-assertion of RESTZ to determine REFCLK Frequency Selection. DLPC2607 I^2C address is set corresponding to the sampled input value as follows:	
					Without External Pullup (1)	With External Pullup (2)
					PLL assumes REFCLK = 16.67 MHz	PLL assumes REFCLK = 8.33 MHz

(1) If operation does not call for an external pullup and there is no external logic that might overcome the weak internal pulldown resistor, then this I/O can be left open or unconnected for typical operation. If operation does not call for an external pullup, but there is external logic that might overcome the weak internal pulldown resistor, then an external pulldown resistor is recommended to ensure a logic low.
(2) External pullup resistor must be 15 kΩ or less.

Table 11. (continued)

Pin		I/O		Clock	Test and Debug Interfaces	
Name	**No.**	**Power**	**Type**	**System**	**Description**	
TSTPT_7	R9	VCC18	B18	Async	Test Pin 7 and I^2C Address Selection – Sampled as an input test mode selection control upon release of $\overline{\text{RESET}}$ and then driven as an output. Includes weak internal pulldown. **Normal use**: Reserved for Test Output. Should be left open or unconnected for typical use. **Alternative use**: Not yet defined. This pin is sampled upon de-assertion of $\overline{\text{RESET}}$ to determine I^2C Address Selection. DLPC2607 I^2C address is set corresponding to the sampled input value as follows:	
					Without External Pullup (1)	With External Pullup (2)
					I^2C slave Write Address = x36 I^2C slave Read Address = x37	I^2C slave Write Address = x3A I^2C slave Read Address = x3B

Power and Ground Pins

Power and ground connections to the DLPC2607 device are made up of these groupings:

Table 12. DLPC2607 Power and Ground Pin Descriptions(1)

Power Group Name	Description	Pin Number
VDD10	1-V core logic power supply	D5, D9, F4, F12, J4, J12, M6, M8, M11
VDD_PLL	1-V power supply for the internal PLL	H12
VCC18	1.8-V power supply for all I/O other than the Host, Video Interface and the SPI flash buses	C4, D8, E4, G3, K3, K12, L4, M5, M9, M12, N4, N12
VCC_FLSH	1.8-V, 2.5-V, or 3.3-V power supply for SPI Flash bus I/O	D6
VCC_INTF	1.8-V, 2.5-V, or 3.3-V power supply for all I/Os on the Host or Video Interface (includes I^2C, DBI-C, PDATA, video syncs, $\overline{\text{PARK}}$, and LED_ENABLE pins)	D11, E12
GND	Common Ground	D4, D7, D10, D12, G4, G12, H4, K4, L12, M4, M7, M10
RTN_PLL	Analog Ground Return for the PLL (This must be connected to the common ground GND through a ferrite)	J13
Reserved	No Connects. Other signals can be routed through the ball on these pins (versus going around them) to ease routing if desired	C2, C3, N2, N3

(1) 134 total signal I/O pins, 38 total power or ground pins, and 4 total reserved pins

I/O Characteristics

Voltage and current characteristics for each I/O type signal listed previously in the DLPC2607 pin description table are summarized in Table 13. All inputs and outputs are LVCMOS.

Table 13. I/O Characteristics(1)

I/O Type	Description	VCCIO (nom)	V_{IL}(2) (min)	V_{IL} (max)	V_{IH} (min)	V_{IH}(3) (max)	I_{IN}(4) (max)	V_{OH}(5) (min)	V_{OL}(6) (max)	I_{OH}(7) (min)	I_{OL}(8) (min)	ITS (9) (max)
		(V)	(V)	(V)	(V)	(V)	(µA)	(V)	(V)	(mA)	(mA)	(µA)
I1	Input (STD)	1.8	–0.3	0.5	1.2	3	± 10					
I2	Input (FLSH)	1.8	–0.3	0.5	1.2	3	± 10					
		2.5	–0.3	0.7	1.7	3.6	± 10					
		3.3	–0.3	0.8	2	3.6	± 10					
I3	Input (INTF)	1.8	–0.3	0.5	1.2	3	± 10					
		2.5	–0.3	0.7	1.7	3.6	± 10					
		3.3	–0.3	0.8	2	3.6	± 10					
I4	Input (REFCLK)	1.8	–0.3	0.5	1.2	3	± 10					
O14	1× Output (STD/ REFCLK)	1.8						1.25	0.4	2.89	2.58	± 10
O24	1× Output (FLSH)	1.8						1.25	0.4	2.89	2.58	± 10
		2.5						1.7	0.7	6.3	6.2	± 10
		3.3						2.4	0.4	9.38	5.29	± 10
O58	2× Output (DMD)	1.8						1.25	0.4	5.78	6.41	± 10
O64(10)	1× Output (MEM)	1.8						1.53	0.19	4	4	± 10
O74(10)	1× Output (MEM DIFF)(11)	1.8						1.53	0.19	4	4	± 10
B14	1× Bi-directional (STD) output	1.8	–0.3	0.5	1.2	3	± 10	1.25	0.4	2.89	2.58	± 10
B18(12)	2× Bi-directional (STD) output	1.8	–0.3	0.5	1.2	3	± 10	1.25	0.4	5.72	5.15	± 10
B34	1× Bi-directional (INTF) output	1.8	–0.3	0.5	1.2	3	± 10	1.25	0.4	2.89	2.58	± 10
		2.5	–0.3	0.7	1.7	3.6	± 10	1.7	0.7	6.3	6.2	± 10
		3.3	–0.3	0.8	2	3.6	± 10	2.4	0.4	9.38	5.29	± 10
B38	2× Bi-directional (INTF) output	1.8	–0.3	0.5	1.2	3	± 10	2.4	0.4	5.72	5.15	± 10
		2.5	–0.3	0.7	1.7	3.6	± 10	1.7	0.7	12.7	12.4	± 10
		3.3	–0.3	0.8	2.0	3.6	± 10	1.25	0.4	18.68	10.57	± 10
B64(10)	1× Bi-directional (MEM) output	1.8	–0.3	0.57	1.19	2.2	± 10	1.53	0.19	4	4	± 10

(1) Pin PLL_REFCLK_I is a crystal oscillator input pin and is not tested during VIH/VIL testing.
(2) V_{IL} (min) is the absolute minimum voltage that should be applied to each corresponding pin.
(3) V_{OH} (max) is the maximum voltage that should be applied to each corresponding pin.
(4) Input leakage current with no internal pullup or pulldown. V_{IN} = 0 or V_{IN} = VCCIO Where VCCIO = I/O supply voltage
(5) I_{OH} = – rated current
(6) I_{OL} = + rated current
(7) V_{OH} = V_{OH} Max
(8) V_{OL} = V_{OL} Max
(9) 3-state Output leakage current. V_{IN} = 0 or V_{IN} = VCCIO Where VCCIO = I/O supply voltage
(10) O64, O74, and B64 buffers are tested to only 100 µA for IOH/IOL due to tester limitations.
(11) The O74 mDDR differential clock (CK) output is simply a pair of single-ended drivers driven by a true and complementary signal.
(12) B18 buffers are not tested for IIH.

Table 14 provides resistance characteristics for internal pullup and pulldown resistors. Note that the resistance is dependent on the supply voltage level applied to the I/O.

Table 14. Internal Pullup and Pulldown Characteristics(1)(2)

Internal Pullup and Pulldown Resistor Characteristics	VCCIO =	MIN	MAX	UNIT
Weak pullup resistance	3.3 V	N/A	N/A	kΩ
	2.5 V	33	89	kΩ
	1.8 V	50.3	157.3	kΩ

(1) The description column of Table 1 identifies whether the corresponding signal includes an internal pullup or pulldown resistor.
(2) Due to tester limitations, only the 1.8-V pullup resistors are measured and no pulldown resistors are measured.

Table 14. Internal Pullup and Pulldown Characteristics[1][2] (continued)

Internal Pullup and Pulldown Resistor Characteristics	VCCIO =	MIN	MAX	UNIT
Weak pulldown resistance	3.3 V	17.8	79.6	kΩ
	2.5 V	37	109	kΩ
	1.8 V	51.8	184.1	kΩ

Absolute Maximum Ratings[1]

PARAMETER		CONDITIONS	MIN	MAX	UNIT
Voltage[2]	V_{DD10}		–0.5	1.32	V
	VDD_PLL		–0.5	1.32	V
	V_{CC18}		–0.5	2.75	V
	VCC_FLSH		–0.5	3.60	V
	V_{CC_INTF}		–0.5	3.60	V
	V_I 1.8 V, 2.5 V, 3.3 V [3]		–0.5	3.60	V
Operating junction temperature range, T_J			–30	105	ºC
Storage temperature range, T_{stg}			–40	125	ºC
ESD	Electrostatic discharge immunity[3]	Human body model (HBM)		± 2000	V
		Charged device model (CDM)		± 500	V

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND, and at the device not at the power supply.
(3) Applies to external input and bidirectional buffers.

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VDD10	1-V supply voltage, core logic		0.95	1	1.05	V
VDD_PLL	Analog voltage for PLL		0.95	1	1.05	V
VCC18	1.8-V supply voltage (for all non-FLASH and Host interface signals)		1.71	1.8	1.89	V
VCC_FLSH	Configuration and control I/O supply voltage (variable)	1.8-V LVCMOS	1.71	1.8	1.89	V
		2.5-V LVCMOS	2.375	2.5	2.625	V
		3.3-V LVCMOS	3.135	3.3	3.465	V
VCC_INTF	Pixel interface supply voltage (variable)	1.8-V LVCMOS	1.71	1.8	1.89	V
		2.5-V LVCMOS	2.375	2.5	2.625	V
		3.3-V LVCMOS	3.135	3.3	3.465	V
V_I	Input voltage		–0.3		VCCIO[1] + 0.3	V
V_O	Output voltage		0		VCCIO[1]	V
VESDHBM	ESD sensitivity [2]	Human Body Model			±2000	V
VESDCDM	ESD sensitivity [2]	Charged Device Model			±500	V
t_{RAMP}	Power supply ramp time		10			µs

(1) VCCIO represents the actual supply voltage applied to the corresponding I/O.
(2) ESD specifications are targets. These values are updated when testing is completed.

Thermal Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_J	Operating junction temperature		–30		105	ºC

Thermal Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_A	Operating Ambient temperature	See (1) (2)	–30		85	ºC

(1) I/O simulations (using IBIS models) are strongly recommended for operation near the extremes of the supported ambient operating temperature range to ensure that the PCB design provides acceptable signal integrity.
(2) The Operating Ambient temperature range assumes zero forced air flow, a JEDEC JESD51 Junction-to-Ambient Thermal Resistance value at zero forced air flow ($R_{\theta JA}$ at 0 m/s), a JEDEC JESD51 standard test card and environment, along with min and max estimated power dissipation across process, voltage, and temperature. Thermal conditions vary by application, which impacts $R_{\theta JA}$. Thus, maximum operating ambient temperature varies by application.
(a) $T_{A\_min} = T_{J\_min} – (P_{D\_min} \times R_{\theta JA}) = –30°C - (0.0W \times 64.96°C/W) = –30°C$
(b) $T_{A\_min} = T_{J\_min} – (P_{D\_min} \times R_{\theta JA}) = 105°C - (0.3W \times 64.96°C/W) = 85°C$

The underlying thermal limitation for the DLPC2607 device is that the maximum operating junction temperature (T_J) must not be exceeded. This temperature is dependent on operating ambient temperature, airflow, PCB design (including the component layout density and the amount of copper used), power dissipation of the DLPC2607 device, and power dissipation of surrounding components. The DLPC2607 package is designed primarily to extract heat through the power and ground planes of the PCB, thus copper content and airflow over the PCB are important factors.

General Electrical Requirements

Typical Current and Power Dissipation

Table 15. Typical Current and Power Dissipation

Supply	Typical Voltage (V)	WVGA Applications		nHD Applications	
		Typical Current (mA)	Typical Power (mW)	Typical Current (mA)	Typical Power (mW)
I/F Sleep Mode DISabled (1) (2) (3)					
VCC_INTF	1.8	0	0.1	0	0.1
VCC_FLSH(4)	2.5	0	0	0	0
VCC18	1.8	28.2	50.8	22.7	40.9
VDD_PLL	1	2.8	2.8	2.8	2.8
VDD10	1	39	39.0	37.7	37.7
Total			92.7		81.5
I/F Sleep Mode ENabled (1) (2) (3)					
VCC_INTF	1.8	0	0.1	0	0.1
VCC_FLSH	2.5	0	0	0	0
VCC18(4)	1.8	27	48.6	22.5	40.4
VDD_PLL	1	2.8	2.8	2.8	2.8
VDD10	1	30.6	30.6	29.3	29.3
Total			82.1		72.6

(1) I/F Sleep is a programmable parameter that can be set to save power in free-run, sequencer mode when displaying still images on the DMD. When I/F Sleep is Enabled, any images applied to the input bus to the DLPC2607 device are ignored.
(2) Power for both I/F sleep mode Disabled and I/F sleep mode Enabled was measured while transferring a full 864 × 480 landscape image at periodic 30 frames per second. The image was a 12 × 6 color checkerboard.
(3) All measurements were taken on a TI internal reference design board at 25°C ambient.
(4) VCC_FLSH power was 0 at the time of the measurement because flash accesses are limited when the ASIC is being configured.

Interface Timing Requirements

This section defines the timing requirements for the external interfaces for the DLPC2607 ASIC.

Parallel Bus Interface

The parallel bus interface complies with standard graphics interface protocol, which includes a vertical sync signal (VSYNC_WE), horizontal sync signal (HSYNC_CS), optional data valid signal (DATAEN_CMD), a 24-bit data bus (PDATA), and a pixel clock (PCLK). The polarity of both syncs are programmable as is the active edge of the clock. Figure 5 shows the relationship of these signals. The data valid signal (DATAEN_CMD) is optional in that the DLPC2607 device provides auto-framing parameters that can be programmed to define the data valid window based on pixel and line counting relative to the horizontal and vertical syncs.

In addition to these standard signals, an optional side-band signal (PDM_CVS_TE) is available, which allows periodic frame updates to be stopped without losing the displayed image. When PDM_CVS_TE is active, it acts as a data mask and does not allow the source image to be propagated to the display. A programmable PDM polarity parameter determines if it is active high or active low. This parameter defaults to make PDM_CVS_TE active high, thus if this function is not desired, then it should be tied to a logic low on the PCB. PDM_CVS_TE is restricted to change only during vertical blanking. Note that VSYNC_WE must remain active at all times (in Lock-to-VSYNC mode) or the display sequencer stops and causes the LEDs to be shut off.

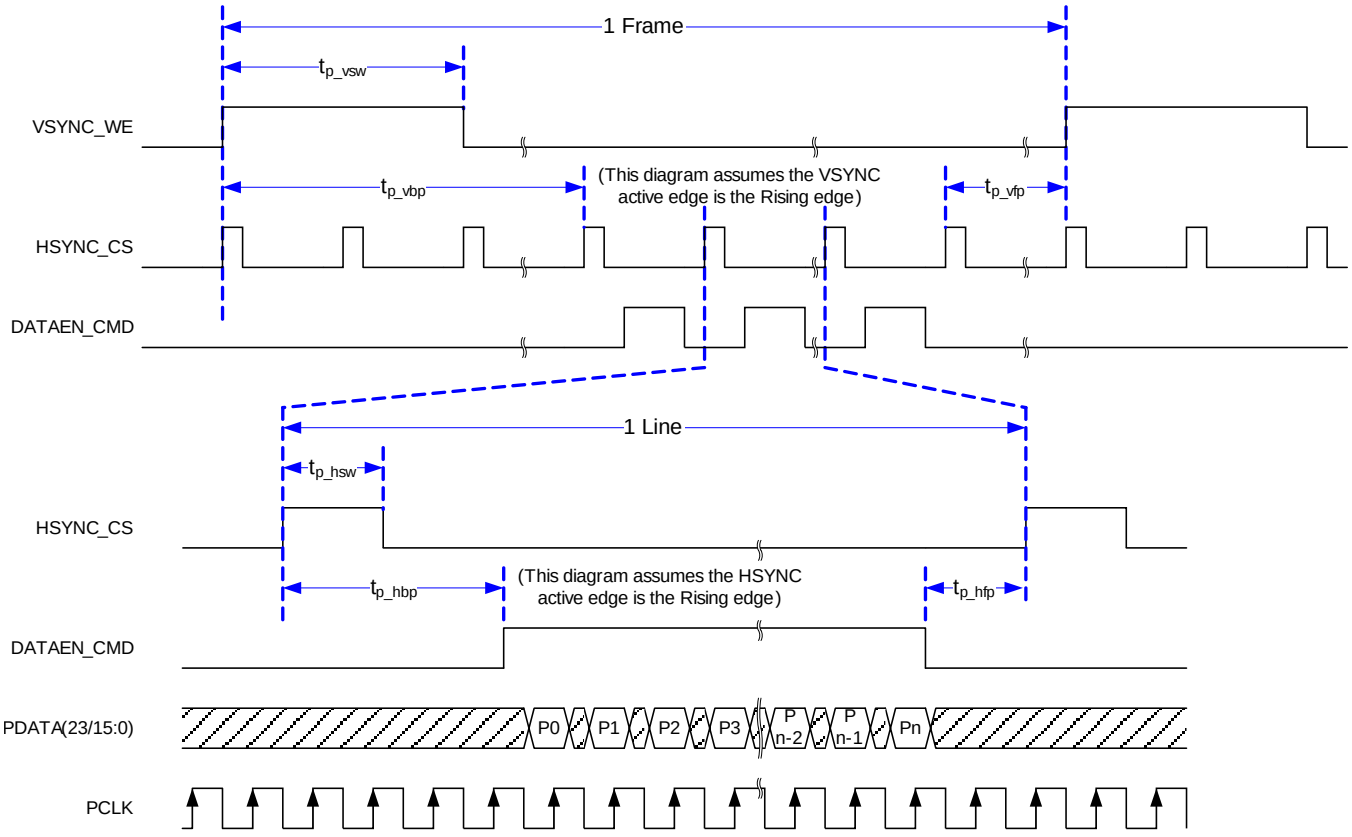


Figure 5. Parallel I/F Frame Timing

Interface Timing Requirements (continued)

Table 16. Parallel I/F Frame Timing Requirements

PARAMETER	DESCRIPTION	TEST CONDITION	MIN	MAX	UNIT
t_{p_vsw}	Pulse Width – VSYNC_WE high	50% reference points	1		lines
t_{p_vbp}	Vertical Back Porch – time from the leading edge of VSYNC_WE to the leading edge HSYNC_CS for the first active line (1)	50% reference points	2		lines
t_{p_vfp}	Vertical Front Porch – time from the leading edge of the HSYNC_CS following the last active line in a frame to the leading edge of VSYNC_WE (1)	50% reference points	1		lines
t_{p_tvb}	Total Vertical Blanking – time from the leading edge of HSYNC_CS following the last active line of one frame to the leading edge of HSYNC_CS for the first active line in the next frame. This is equal to the sum of Vertical Back Porch (t_{p_vbp}) + Vertical Front Porch (t_{p_vfp}).	50% reference points	12		lines
t_{p_hsw}	Pulse Width – HSYNC_CS high	50% reference points	4	128	PCLKs
t_{p_hbp}	Horizontal Back Porch – time from rising edge of HSYNC_CS to rising edge of DATAEN_CMD	50% reference points	4		PCLKs
t_{p_hfp}	Horizontal Front Porch – time from falling edge of DATAEN_CMD to rising edge of HSYNC_CS	50% reference points	8		PCLKs
t_{p_thh}	Total Horizontal Blanking – sum of horizontal front and back porches	50% reference points			(2) PCLKs

(1) The programmable parameter Vertical Sync Line Delay (I^2C: 0x23) must be set such that: 6 – Vertical Front Porch (t_{p_vfp})' (min 0) ≤ Vertical Sync Line Delay ≤ Vertical Back Porch ($tp_{\_vbp}$) – 2 (max 15). The default value for Vertical Sync Line Delay is set to 5; thus, only a Vertical Back Porch less than 7 requires potential action.

(2) Total horizontal blanking is driven by the max line rate for a given source, which is a function of resolution and orientation. See Table 18 for max line rate for each source and display combination. t_{p_thb} = Roundup [(1000 x f_{clock})/ LR] – APPL where f_{clock} = Pixel Clock rate in MHz, LR = line rate in kHz and the number of active pixels per (horizontal) line is APPL. If t_{p_thb} is calculated to be less than t_{p_hbp} + t_{p_hfp}, then the pixel clock rate is too low, or the line rate is too high, and one or both must be adjusted.

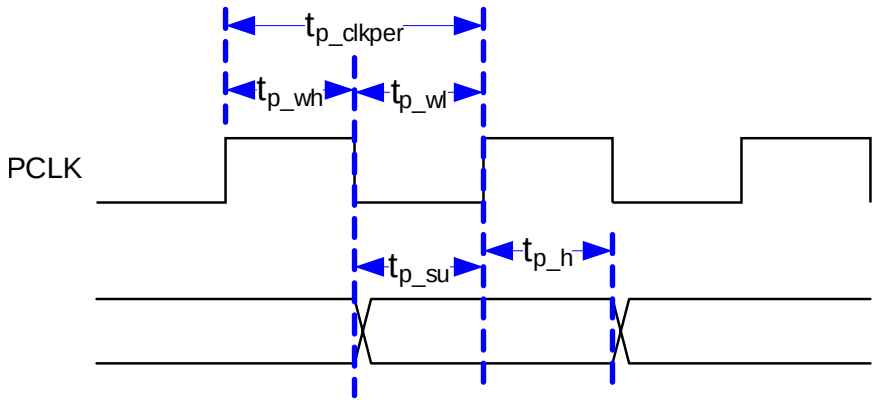


Figure 6. Parallel and BT.656 I/F General Timing

Table 17. Parallel I/F General Timing Requirements

PARAMETER	DESCRIPTION		MIN	MAX	UNIT
f_{clock}	Clock frequency, PCLK		1	33.5	MHz
t_{p_clkper}	Clock period, PCLK	50% reference points	29.85	1000	ns
t_{p_clkjit}	Clock jitter, PCLK	Max f_{clock}	(1)	(1)	
t_{p_wh}	Pulse-width low, PCLK	50% reference points	10		ns
t_{p_wl}	Pulse-width high, PCLK	50% reference points	10		ns
t_{p_su}	Setup time – HSYNC_CS, DATEN_CMD, PDATA (23:0) valid before the active edge of PCLK (2)	50% reference points	3		ns

(1) Clock jitter (in ns) should be calculated using this formula: Jitter = (1/ f_{clock} – 28.35 ns). Setup and hold times must be met during clock jitter.

(2) See Figure 6.

Table 17. Parallel I/F General Timing Requirements (continued)

PARAMETER	DESCRIPTION		MIN	MAX	UNIT
t_{p_h}	Hold time – HSYNC_CS, DATEN_CMD, PDATA (23:0) valid after the active edge of PCLK (2)	50% reference points	3		ns
t_t	Transition time – all signals	20% to 80% reference points	0.2	4	ns

Table 18. Parallel I/F Max Supported Horizontal Line Rate

DMD	Parallel Bus Source	Landscape Format		Portrait Format	
		Resolution (HxV)	Max Line Rate (kHz)	Resolution (HxV)	Max Line Rate (kHz)
0.3 WVGA and 0.24 VGA Diamond	NSTC (1)	720 × 240 (2)	17	Not supported	N/A
	PAL (1)	720 × 288 (2)	20	Not supported	N/A
	QVGA	320 × 240 (2)	17	240 × 320 (2)	22
	QWVGA	427 × 240 (2)	17	240 × 427 (3),(2)	27
	nHD	640 × 360 (2)	25	360 × 640 (2)	42
	3:2 VGA	640 × 430 (2)	30	430 × 640 (2)	45
	4:3 VGA	640 × 480 (2)	34	480 × 640 (2)	45
	WVGA-720	720 × 480 (2)	34	480 × 720 (2)	51
	WVGA-752	752 × 480 (2)	34	480 × 752 (2)	53
	WVGA-800	800 × 480 (2)	34	480 × 800 (2)	56
	WVGA-852	852 × 480 (2)	34	480 × 852 (2)	56
	WVGA-853	853 × 480 (2)	34	480 × 853 (2)	56
	WVGA-854	854 × 480 (2)	34	480 × 854 (2)	56
	WVGA-864	864 × 480 (2)	34	480 × 864 (2)	56
0.2 nHD Manhattan	NSTC (1)	720 × 240 (2)	32	Not supported	N/A
	PAL (1)	720 × 288 (2)	39	Not supported	N/A
	QVGA	320 × 240	32	240 × 320 (2)	42
	QWVGA	427 × 240	32	240 × 427 (2)	52
	nHD	640 × 360	48	360 × 640 (2)	79
	3:2 VGA	640 × 430 (2)	50	430 × 640 (2)	74
	4:3 VGA	640 × 480 (2)	50	480 × 640 (2)	66
	WVGA-720	720 × 480 (2)	44	480 × 720 (2)	66
	WVGA-752	752 × 480 (2)	42	480 × 752 (2)	66
	WVGA-800	800 × 480 (2)	40	480 × 800 (2)	66
	WVGA-852	852 × 480 (2)	37	480 × 852 (2)	66
	WVGA-853	853 × 480 (2)	37	480 × 853 (2)	66
	WVGA-854	854 × 480 (2)	37	480 × 854 (2)	66
	WVGA-864	864 × 480 (2)	37	480 × 864 (2)	66

(1) NTSC and PAL are assumed to be interlaced sources
(2) Not supported for 100 to 120-Hz operation
(3) See the Functional Limitations Section

Device Information

Parallel Bus Interface

The parallel bus interface supports six data transfer formats:

- 16-bit RGB565
- 18-bit RGB666
- 18-bit 4:4:4 YCrCb666
- 24-bit RGB888
- 24-bit 4:4:4 YCrCb888
- 16-bit 4:2:2 YCrCb (standard sampling assumed to be Y0Cb0, Y1Cr0, Y2Cb2, Y3Cr2, Y4Cb4, Y5Cr4, …)

The required PDATA(23:0) bus mapping for these six data transfer formats are shown in Figure 7.

Parallel Bus Mode – 4:4:4 RGB and YCrCb Sources

PDATA(15:0) – 565 Mapping to 888

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDATA(15:0) of the Input Pixel data bus																
Bus Assignment Mapping	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
RGB Data bit mapping on the ASIC																
4:4:4 YCrCb Data bit mapping on the ASIC																

PDATA(17:0) – 666 Mapping to 888

	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDATA(17:0) of the Input Pixel data bus																		
Bus Assignment Mapping	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
RGB Data bit mapping on the ASIC																		
4:4:4 YCrCb Data bit mapping on the ASIC	Cr 5	Cr 4	Cr 3	Cr 2	Cr 1	Cr 0	Y 5	Y 4	Y 3	Y 2	Y 1	Y 0	Cb 5	Cb 4	Cb 3	Cb 2	Cb 1	Cb 0

PDATA(23:0) – 888 Mapping

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDATA(23:0) of the Input Pixel data bus																								
Bus Assignment Mapping	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
RGB Data bit mapping on the ASIC																								
4:4:4 YCrCb Data bit mapping on the ASIC	Cr 7	Cr 6	Cr 5	Cr 4	Cr 3	Cr 2	Cr 1	Cr 0	Y 7	Y 6	Y 5	Y 4	Y 3	Y 2	Y 1	Y 0	Cb 7	Cb 6	Cb 5	Cb 4	Cb 3	Cb 2	Cb 1	Cb 0

Parallel Bus Mode - 16-bit YCrCb 4:2:2 Source

PDATA(23:0) – Cr/CbY880 Mapping

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDATA(23:0) of the Input Pixel data bus																								
Bus Assignment Mapping	Cr/ Cb 7	Cr/ Cb 6	Cr/ Cb 5	Cr/ Cb 4	Cr/ Cb 3	Cr/ Cb 2	Cr/ Cb 1	Cr/ Cb 0	Y 7	Y 6	Y 5	Y 4	Y 3	Y 2	Y 1	Y 0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Data bit mapping on the pins of the ASIC																								

Figure 7. PDATA Bus – Parallel I/F Mode Bit Mapping

BT.656 Interface

The DLPC2607 ASIC input interface supports the industry standard BT.656 parallel video interface. See the appropriate ITU-R BT.656 specification for detailed interface timing requirements.

Table 19. BT.565 I/F General Timing Requirements(1)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{clock}	Clock frequency, PCLK		1	33.5	MHz
t_{p_clkper}	Clock period, PCLK	50% reference points	29.85	1,000	ns
t_{p_clkjit}	Clock jitter, PCLK	Maximum f_{clock}	(2)	(2)	
t_{p_wh}	Pulse duration low, PCLK	50% reference points	10		ns
t_{p_wl}	Pulse duration high, PCLK	50% reference points	10		ns
t_{p_su}	Setup time – HSYNC, DATEN, PDATA(23:0) valid before the active edge of PCLK	50% reference points	3		ns
t_{p_h}	Hold time – HSYNC, DATEN, PDATA(23:0) valid after the active edge of PCLK	50% reference points	3		ns
t_t	Transition time – all signals	20% to 80% reference points	0.2	4	ns

(1) The BT.656 I/F accepts 8-bit per color, 4:2:2 YCb/Cr data encoded per the industry standard via PDATA(7:0) on the active edge of PCLK (that is, programmable) as shown in Figure 6.
(2) Clock jitter should be calculated using this formula: Jitter = (1/ f_{clock} – 28.35 ns). Setup and hold times must be met during clock jitter.

BT.656 data bits should be mapped to the DLPC2607 PDATA bus as shown in Figure 8.

BT.656 Bus Mode – YCrCb 4:2:2 Source

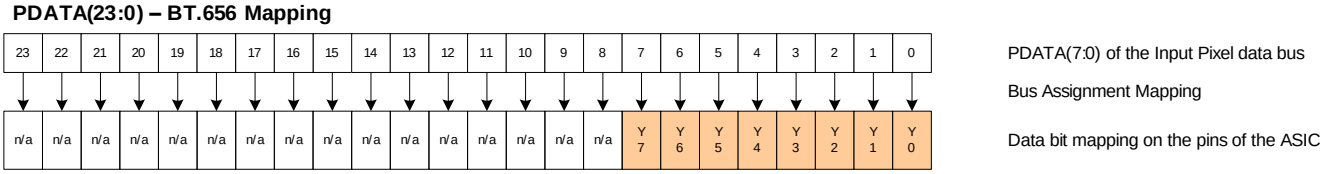


Figure 8. DLPC2607 PDATA Bus – BT.656 I/F Mode Bit Mapping

100 to 120-Hz 3-D Display Operation

The DLPC2607 device supports 100 to 120-Hz 3-D display operation, but is limited to a narrow set of configurations. 3-D operation is limited to:

- 0.2 nHD DMDs only
- nHD, WQVGA and QVGA source resolutions
- Parallel bus interface only (All pixel formats are supported)
- Landscape source and display orientation only
- Non-interlaced video-graphics only
- 100 ±1% or 120 ±1% source frame rates
- Un-packed, full resolution, frame sequential, 3-D format (that is each 100 or 120-Hz source frame contains a single, full resolution, eye frame separated by VSYNCs, where an eye frame is contains image data for a single left or right eye; not both)
- Minimum line rates that satisfy the high frame rates

To support 3-D operation, the DLPC2607 device should be run in Lock-to-VSYNC mode with 1× frame rate multiplication (that is, no frame rate multiplication). Each DMD frame is displayed at the source frame rate in the order it is received.

Because of the high frame rate of the source, the source line rate must be much higher than typical, but still can not exceed the rates defined in Table 18. The minimum line rate is limited by the maximum frame rate and minimum total vertical blanking. The following tables provide a summary of the line rate range assuming the minimum total vertical blanking (TVB).

Table 20. 100 to 120-Hz Operational Limitations

Source	Resolution (APPL x ALPF)	MIN Frame Rate	NOM Frame Rate	MAX Frame Rate	MIN TVB (tp_tvb)	MAX Line Rate	MIN Line Rate	MIN Clock Rate
		(Hz)	(Hz)	(Hz)	(Lines)	(KHz)	(KHz)	(MHz)
nHD	640 × 360	99	100	101	12	48	(1)	(2)
WQVGA	427 × 240	99	100	101	12	32	(1)	(2)
QVGA	320 × 240	99	100	101	12	32	(1)	(2)
nHD	640 × 360	118.8	120	121.2	12	48	(1)	(2)
WQVGA	427 × 240	118.8	120	121.2	12	32	(1)	(2)
QVGA	320 × 240	118.8	120	121.2	12	32	(1)	(2)

(1) The following equation should be used to determine the minimum line rate for a given application. The application can not be supported if the calculated minimum line rate exceeds the maximum line rate defined elsewhere in this table;
Line_Rate_min (KHz) = Frame_Rate_max (Hz) × [ALPF + TVB] /1000
Where: TVB = Total Vertical Blanking (in lines)
ALPF = Active Lines Per Frame
Frame_Rate_max = Max frame rate including all expected wander

(2) The following equation should be used to determine the minimum Pixel Clock rate for a given application. The application can not be supported if the calculated minimum Pixel Clock rate exceed the max Pixel Clock rate defined in Error! Reference source not found.;
Pixel_Clock_min (MHz) = Line_Rate_max (KHz) × (APPL + 12) / 1000
Where: APPL = Active Pixels Per Line
Line_Rate_max = Max line rate including all expected wander

It is assumed that a front-end device ahead of the DLPC2607 device converts all 3-D sources to the 3-D format defined previously and provides any needed left or right-eye selection control directly to the 3-D glasses (that is, the DLPC2607 device does not control the glasses). Note that the DLPC2607 device includes a double buffer frame memory, which causes the displayed image to be delayed one frame relative to its input. This requires left or right eye-frame shutter control to be inverted prior to being sent to the glasses.

Flash Memory Interface

The DLPC2607 ASIC flash memory interface consists of a SPI flash serial interface at 33.3 MHz (nominal).

Table 21. Flash Interface Timing Requirements(1) (2)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{clock}	Clock frequency, SPI_CLK(3)		33.3266	33.34	MHz
t_{p_clkper}	Clock period, SPI_CLK	50% reference points	29.994	30.006	ns
t_{p_wh}	Pulse width low, SPI_CLK	50% reference points	10		ns
t_{p_wl}	Pulse width high, SPI_CLK	50% reference points	10		ns
t_t	Transition time – all signals	20% to 80% reference points	0.2	4	ns
t_{p_su}	Setup time – SPI_DIN valid before SPI_CLK falling edge	50% reference points	10		ns
t_{p_h}	Hold time – SPI_DIN valid after SPI_CLK falling edge	50% reference points	0		ns
t_{p_clqv}	SP_ICLK clock low to output valid time – SPIDOUT and SPI_CSZ	50% reference points		1	ns
t_{p_clqx}	SPI_CLK clock low output hold time – SPI_DOUT and SPI_CSZ	50% reference points	–1		ns

(1) Standard SPI protocol is to transmit data on the falling edge of SPI_CLK and to capture data on the rising edge. The DLPC2607 device does transmit data on the falling edge, but it also captures data on the falling edge rather than the rising edge. This provides support for SPI devices with long clock-to-Q timing. The DLPC2607 device hold capture timing is set to facilitate reliable operation with standard external SPI protocol devices.

(2) With the above output timing, the DLPC2607 device provides the external SPI device 14-ns input set-up and 14-ns input hold relative to the rising edge of SPI_CLK.

(3) This range includes the 200 ppm of the external oscillator (but no jitter).

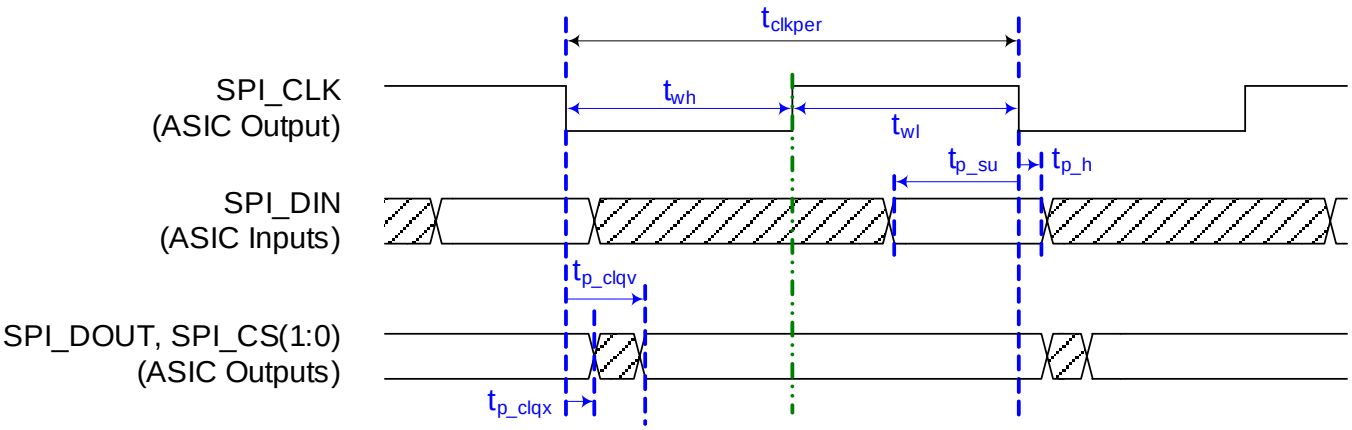


Figure 9. Flash I/F Timing

DMD Interface

The DLPC2607 ASIC DMD interface consists of a 76.19-MHz (nominal) DDR output-only interface with LVCMOS signaling.

Table 22. DMD Interface Timing Requirements(1)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{clock}	Clock frequency, DMD_DCLK and DMD_SAC_CLK(2)		76.198	76.206	MHz
t_{p_clkper}	Clock period, DMD_DCLK and DMD_SAC_CLK	50% reference points	13.123	15	ns
t_{p_wh}	Pulse duration low, DMD_DCLK and DMD_SAC_CLK	50% reference points	6.2		ns
t_{p_wl}	Pulse duration high, DMD_DCLK and DMD_SAC_CLK	50% reference points	6.2		ns
t_t	Transition time – all signals	20% to 80% reference points	0.3	2	ns
t_{p_su}	Output setup time – DMD_D(14:0), DMD_SCTRL, DMD_LOADB and DMD_TRC relative to both rising and falling edges of DMD_DCLK(3) (4)	50% reference points		1.5	ns
t_{p_h}	Output hold time – DMD_D(14:0), DMD_SCTRL,DMD_LOADB and DMD_TRC signals relative to both rising and falling edges of DMD_DCLK(3) (4)	50% reference points		1.5	ns
$t_{p\_d1\_skew}$	DMD data skew – DMD_D(14:0), DMD_SCTRL, DMD_LOADB, and DMD_TRC signals relative to each other(5)	50% reference points		0.2	ns
$t_{p\_clk\_skew}$	Clock skew – DMD_DCLK and DMD_SAC_CLK relative to each other	50% reference points		0.2	ns
$t_{p\_d2\_skew}$	DAD/SAC data skew - DMD_SAC_BUS, DMD_DRC_OEZ(6), DMD_DRC_BUS, and DMD_DRC_STRB signals relative to DMD_SAC_CLK	50% reference points		0.2	ns

(1) Assumes a 30-Ω series termination for all DMD interface signals (except DAD_DMD_OEZ)
(2) This range includes the 200 ppm of the external oscillator (but no jitter).
(3) Assumes minimum DMD setup time = 1 ns and minimum DMD hold time = 1 ns
(4) Output setup and hold numbers already account for controller clock jitter. Only routing skew and DMD setup/hold need be considered in system timing analysis.
(5) Assumes DMD data routing skew = 0.1 ns max
(6) DMD_DAD_OEZ requires a 30 to 100-kΩ external pullup resistor connected to VCC18 to achieve proper timing.

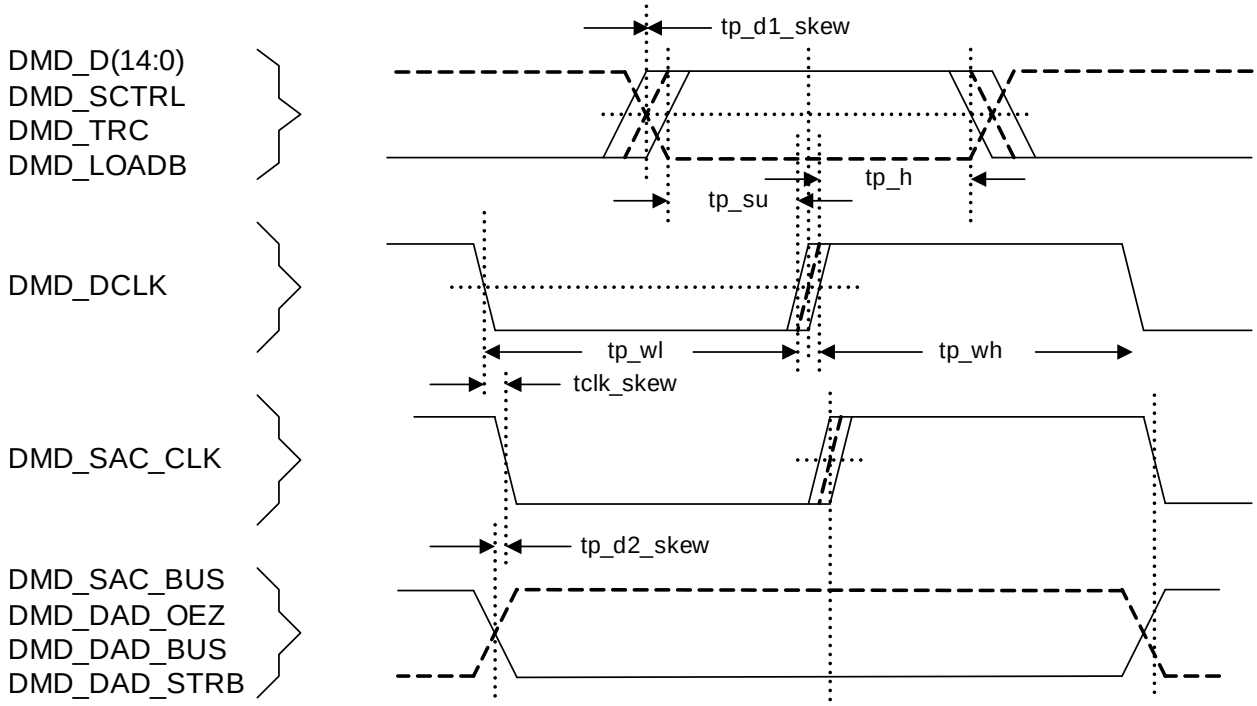


Figure 10. DMD I/F Timing

Mobile DDR Memory I/F

The DLPC2607 ASIC Mobile DDR Memory interface consists of a 16-bit wide, mobile DDR interface (that is, LVCMOS signaling) operated at 133.33 MHz (nominal).

The DLPC2607 controller mobile DDR memory interface consists of a 16-bit wide, mobile DDR interface (that is, LVCMOS signaling) operated at 133.33 MHz (nominal).

Table 23. Mobile DDR Memory Interface Timing Requirements(1) (2) (3)

PARAMETER		MIN	MAX	UNIT
t_{CYCLE}	Cycle-time reference	7500		ps
t_{CH}	CK high pulse width(4)	2700		ps
t_{CL}	CK low pulse width(4)	2700		ps
t_{DQSH}	DQS high pulse width(4)	2700		ps
t_{DQSL}	DQS low pulse width(5)	2700		ps
t_{WAC}	CK to address and control outputs active	–2870	2870	ps
t_{QAC}	CK to DQS output active		200	ps
t_{DAC}	DQS to DQ and DM output active	–1225	1225	ps
t_{DQSRS}	Input (read) DQS and DQ skew(6)		1000	ps

(1) This includes the 200 ppm of the external oscillator (but no jitter).
(2) Output setup and hold numbers already account for controller clock jitter. Only routing skew and memory setup/hold must be considered in system timing analysis.
(3) Assumes a 30-Ω series termination on all signal lines.
(4) CK and DQS pulse duration specs for the DLPC2607 assume it is interfacing to a 166-MHz mDDR device. Even though these memories are only operated at 133.33 MHz, according to memory vendors, the rated t_{CK} spec (that is 6 ns) can be applied to determine minimum CK and DQS pulse duration requirements to the memory.
(5) CK and DQS pulse duration specs for the DLPC2607 assume it is interfacing to a 166-MHz mDDR device. Even though these memories are only operated at 133.33 MHz, according to memory vendors, the rated t_{CK} spec (that is 6 ns) can be applied to determine minimum CK and DQS pulse duration requirements to the memory.
(6) Note that DQS must be within the t_{DQSRS} read data-skew window but need not be centered.

Mobile DDR Memory I/F Timing

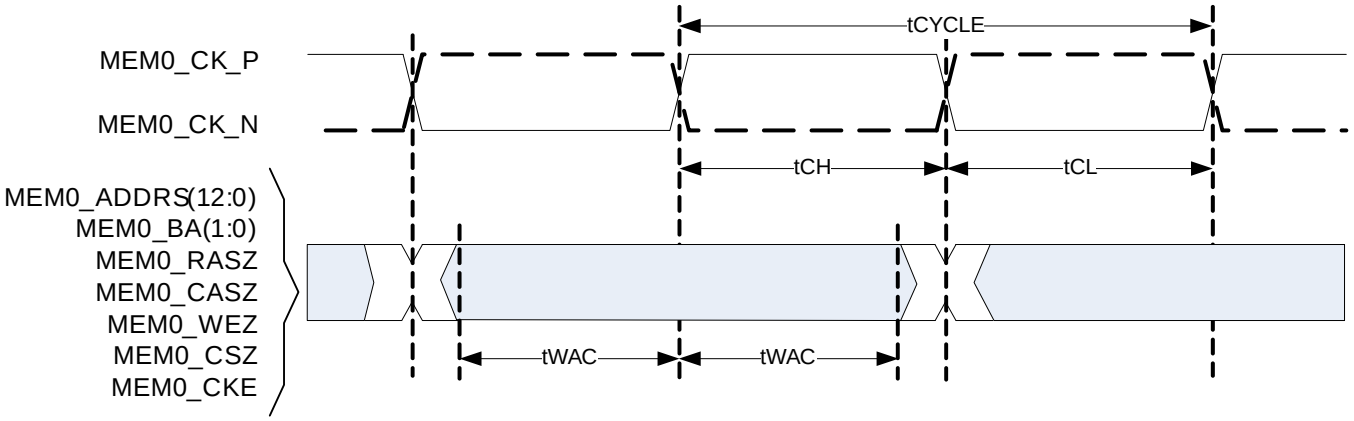


Figure 11. mDRR Memory Address and Control Timing

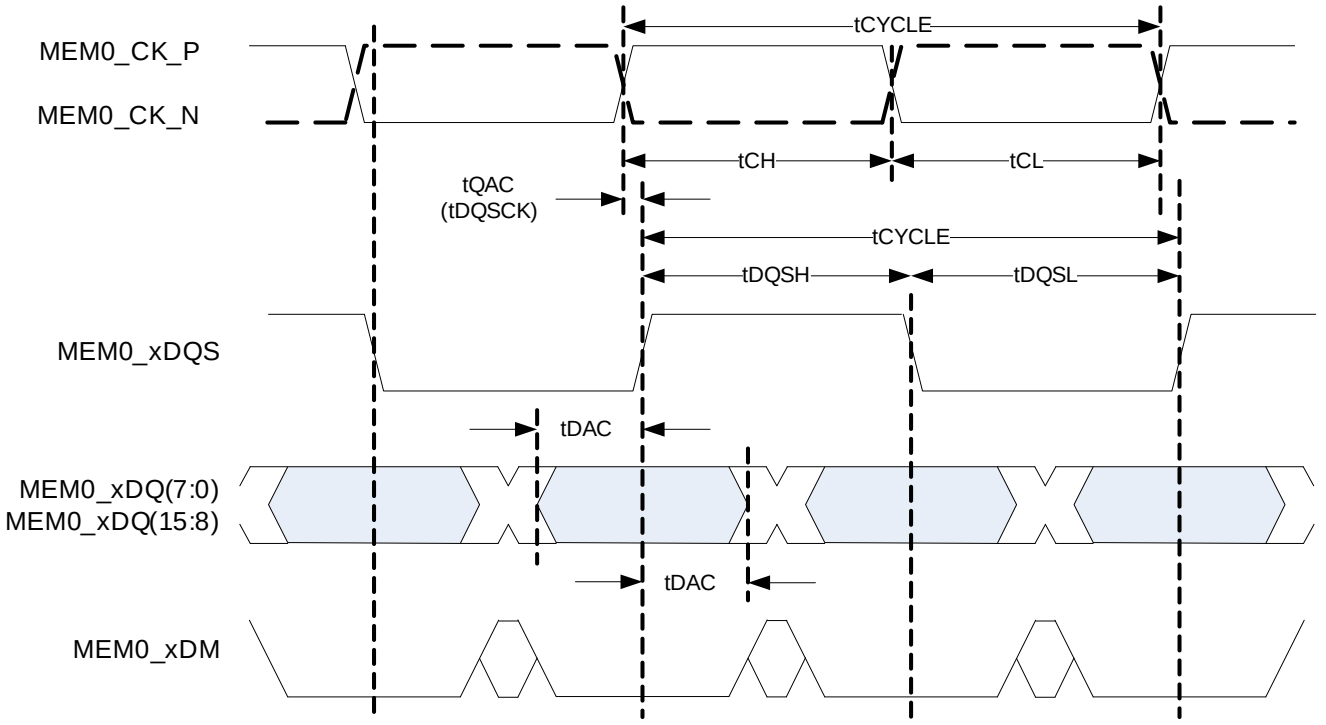


Figure 12. mDRR Memory Write Dtat Timing

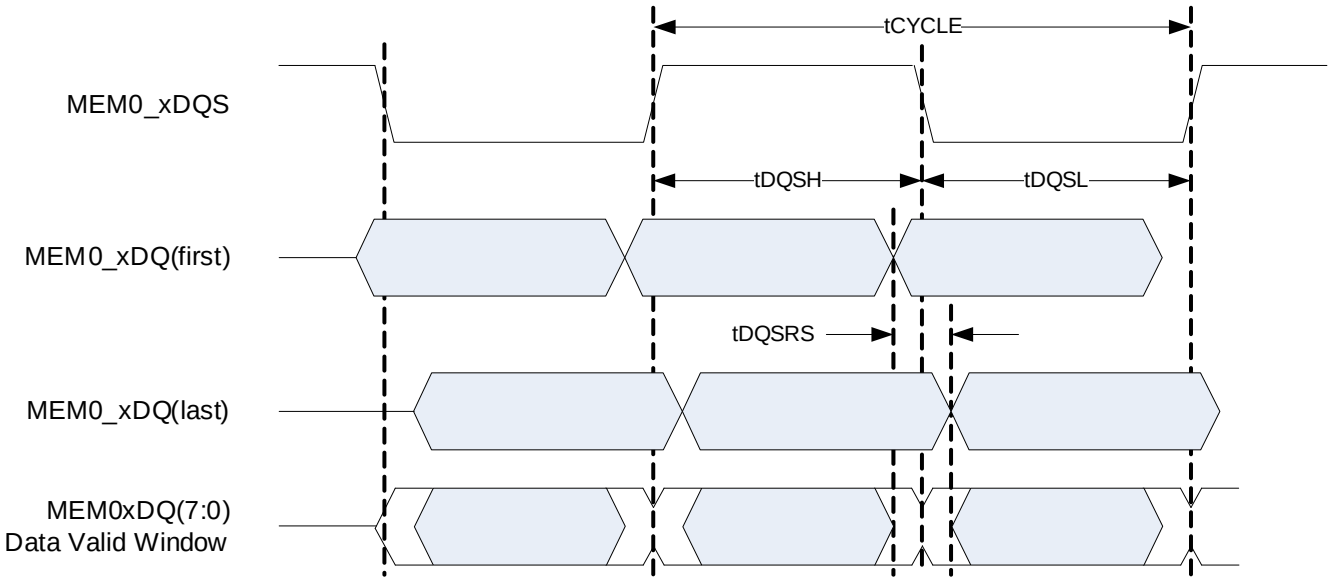


Figure 13. mDDR Memory Read Data Timing

SYSTEM DESIGN CONSIDERATION — APPLICATION INFORMATION

System Power Considerations

The following is a summary of the required power delivery requirements for DLPC2607 for various VCC_FLSH and VCC_INTF power options.

Table 24. Configuration Based Power Supply Requirements

ASIC Power Rail	Usage	Nominal Voltage (V)	Total Supply Margin (1)
VCC_INTF (2)	Video Interface I/O	1.8, 2.5, or 3.3	± 5%
VCC_FLSH (3)	Flash I/O	1.8, 2.5, or 3.3	± 5%
VDD_PLL (4)	Internal PLL	1	± 5%
VCC18	mDDR and DMD I/O	1.8	± 5%
VDD10	ASIC Core	1	± 5%

(1) Total Supply Margin = DC Offset Budget + AC Noise Budget
(2) VCC_INTF is independent of all other supplies.
(3) VCC_FLSH is independent of all other supplies.
(4) When possible, TI recommends to use a tighter supply tolerance (± 3%) for the power to the PLL in order to improve system noise immunity.

System Power-Up and Power-Down Sequence

Although the DLPC2607 device requires an array of power supply voltages, (that is, VDD, VDD_PLL, VCC_18, VCC_FLSH, VCC_INTF), there are no restrictions regarding the relative order of power supply sequencing to avoid damaging the DLPC2607 device. This is true for both power-up and power-down scenarios. Similarly there is no minimum time between powering-up or powering-down the different supplies feeding the DLPC2607 device.

NOTE

Often, there are power sequencing requirements for devices that share the supplies with the DLPC2607 device.

From a functional standpoint, there is one specific power sequencing recommendation to ensure proper operation. In particular, all ASIC power should be applied and allowed to reach the minimum specified voltage levels before RESET is de-asserted to ensure proper power-up initialization is performed. All I/O power should remain applied as long as 1-V core power is applied and RESET is de-asserted.

NOTE

When VDD10 core power is applied but I/O power is not applied, additional leakage current may be drawn.

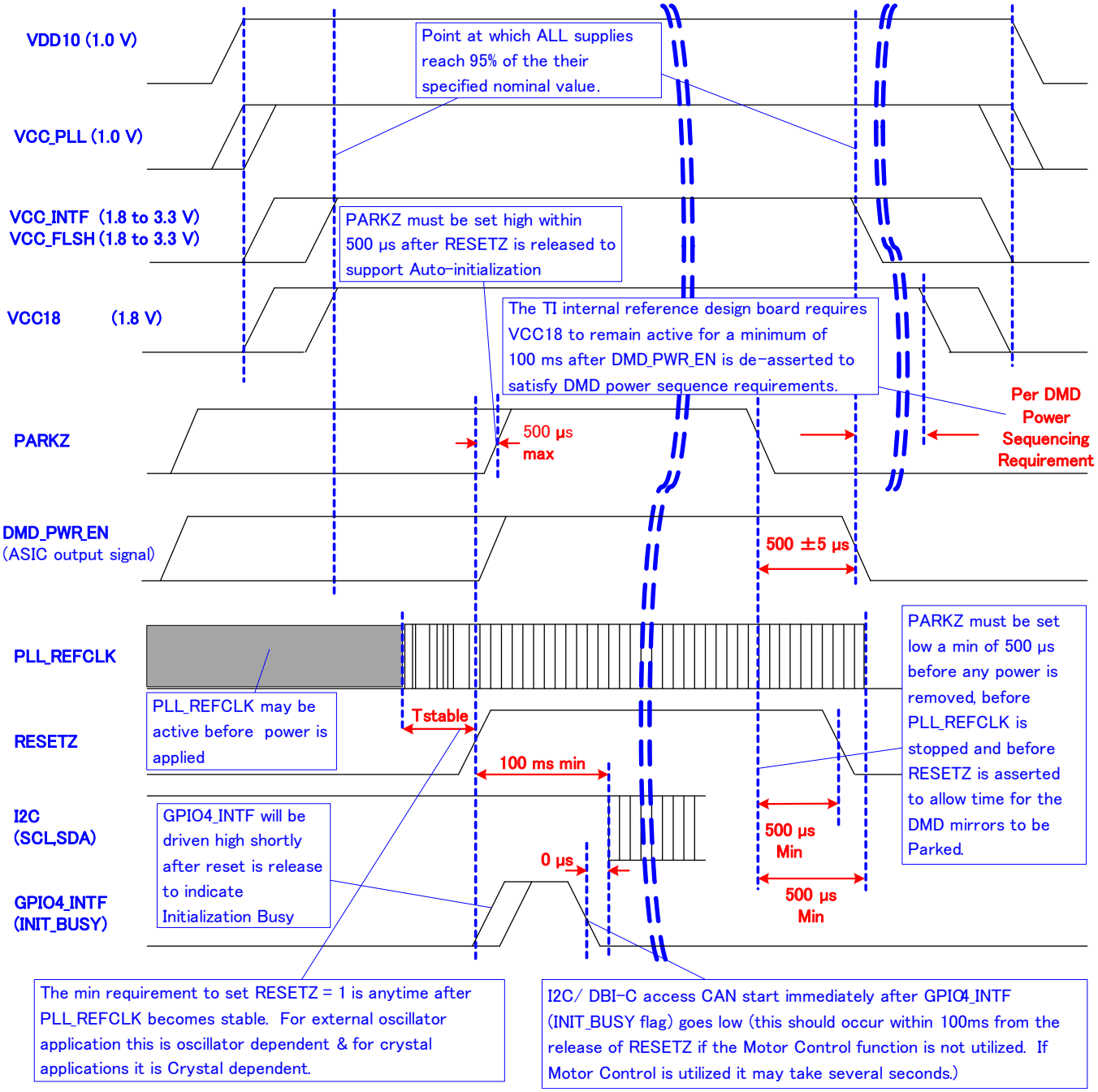


Figure 14. Power-Up and Power-Down Timing

System Power I/O State Considerations

Note that:

- If VCC18 I/O power is applied when VDD10 core power is not applied, then all mDDR (non-fail-safe) and non-mDDR (fail-safe) output signals associated with the VCC18 supply are in a high-impedance state.
- If VCC_INTF or VCC_FLSH I/O power is applied when VDD10 core power is not applied, then all output signals associated with these inactive I/O supplies are in a high-impedance state.
- If VDD10 core power is applied but VCC_INTF or VCC_FLSH I/O power is not applied, then all output signals associated with these inactive I/O supplies are in a high-impedance state.
- If VDD10 core power is applied but VCC18 I/O power is not applied, then all mDDR (non-fail-safe) and non-mDDR (fail-safe) output signals associated with the VCC18 I/O supply are in a high-impedance state; however, if driven high externally, only the non-mDDR (fail-safe) output signals remain in a high-impedance state, and the mDDR (non fail-safe) signals are shorted to ground through clamping diodes.

Power-Up Initialization Sequence

It is assumed that an external power monitor holds the DLPC2607 device in system reset during power-up. It must do this by driving RESET to a logic low state. It should continue to assert system reset until all ASIC voltages have reached minimum specified voltage levels, PARK is asserted high and input clocks are stable. During this time, most ASIC outputs are driven to an inactive state and all bidirectional signals are configured as inputs to avoid contention. ASIC outputs that are not driven to an inactive state are 3-stated, which includes DMD_PWR_EN, LEDDVR_ON, LED_SEL_0, LED_SEL_1, SPICLK, SPIDOUT, and SPICSZ0. After power is stable and the PLL_REFCLK clock input to the DLPC2607 device is stable, then RESET should be deactivated. (Set to a logic high). The DLPC2607 device then performs a power-up initialization routine that first locks its PLL, followed by loading self configuration data from the external flash. Upon release of RESET all DLPC2607 device I/Os become active. Immediately following the release of RESET the GPIO4_INTF signal is driven high to indicate that the auto initialization routine is in progress. Upon completion of the auto-initialization routine, the DLPC2607 device drives GPIO4_INTF low to signal INITIALIZATION DONE (also known as INIT DONE).

NOTE

The host processor can start sending standard I^2C commands after GPIO4 (INIT_DONE) goes low, or a 100-ms timer expires in the host processor, whichever is earlier, irrespective of whether the motor is enabled or not. However, before sending any compound I^2C commands at power-up, the host processor must wait until GPIO4 (INIT_DONE) goes low, irrespective of whether the motor control function is enabled or not. Due to motor movement, the worst-case time to wait for GPIO4 to go low when the motor control function is enabled is system dependent and may take several seconds.

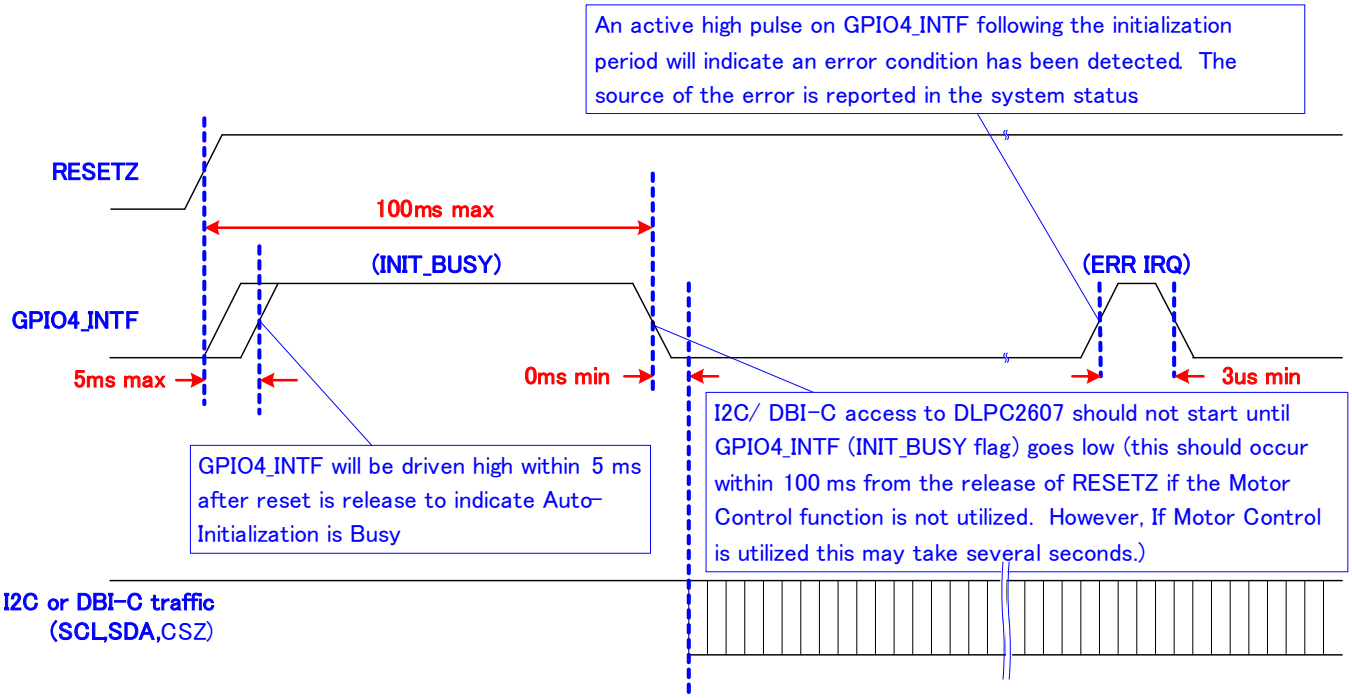


Figure 15. Initialization Timeline

Power-Good ($\overline{\text{PARK}}$) Support

The $\overline{\text{PARK}}$ signal is defined to be an early warning signal that should alert the controller 500 µs before DC supply voltages have dropped below specifications. This allows the controller time to park the DMD, ensuring the integrity of future operation. Note that the reference clock should continue to run and $\overline{\text{RESET}}$ should remain de-activated for at least 500 µs after $\overline{\text{PARK}}$ has been deactivated (set to a logic low) to allow the park operation to complete.

Hot-Plug Usage

Note that the DLPC2607 device provides fail-safe I/O on all host interface signals (signals powered by VCC_INTF). This allows these inputs to be driven high even when no I/O power is applied. Under this condition, the DLPC2607 device does not load the input signal, nor draw excessive current that could degrade ASIC reliability. For example, the I^2C bus from the host to other components would not be affected by powering off VCC_INTF to the DLPC2607 device. Note that TI recommends weak pullups or pulldowns on signals feeding back to the host to avoid floating inputs.

Maximum Signal Transition Time

Unless otherwise noted, the maximum recommended 20% to 80% rise and fall time to avoid input buffer oscillation is 10 ns. This applies to all DLPC2607 device input signals.

NOTE

The $\overline{\text{PARK}}$ input signal includes an additional small digital filter that ignores any input-buffer transitions caused by a slower rise and fall time for up to 150 ns.

Configuration Control

The primary configuration control mechanism for the DLPC2607 device is the I^2C interface. See the *DLPC2607 Software Programmer's Guide*, TI literature number DLPU004, for details on how to configure and control the DLPC2607.

White Point Correction Light Sensor

With the addition of a light-to-voltage light sensor (such as a phototransistor) and a voltage comparator circuit, the DLPC2607 device supports automatic White Point Correction and Power Control.

General PCB Recommendations

PCB Layout Guidelines for Internal ASIC PLL Power

TI recommends the following guidelines to achieve desired ASIC performance relative to the internal PLL. The DLPC2607 device contains one internal PLL, which has a dedicated analog supply (VDD_PLL, VSS_PLL). As a minimum, VDD_PLL power and VSS_PLL ground pins should be isolated using an RC-filter consisting of two 50-Ω series Ferrites and two shunt capacitors (to widen the spectrum of noise absorption). TI recommends that one capacitor be a 0.1-µf capacitor and the other be a 0.01-µf capacitor. All four components should be placed as close to the ASIC as possible, but it's especially important to keep the leads of the high frequency capacitors as short as possible. Note that both capacitors should be connected across VDD_PLL and VSS_PLL on the ASIC side of the ferrites.

The PCB layout is critical to PLL performance. It is important that the quiet ground and power are treated like analog signals. Therefore, VDD_PLL must be a single trace from the DLPC2607 device to both capacitors, and then through the series ferrites to the power source. The power and ground traces should be as short as possible, parallel to each other, and as close as possible to each other.

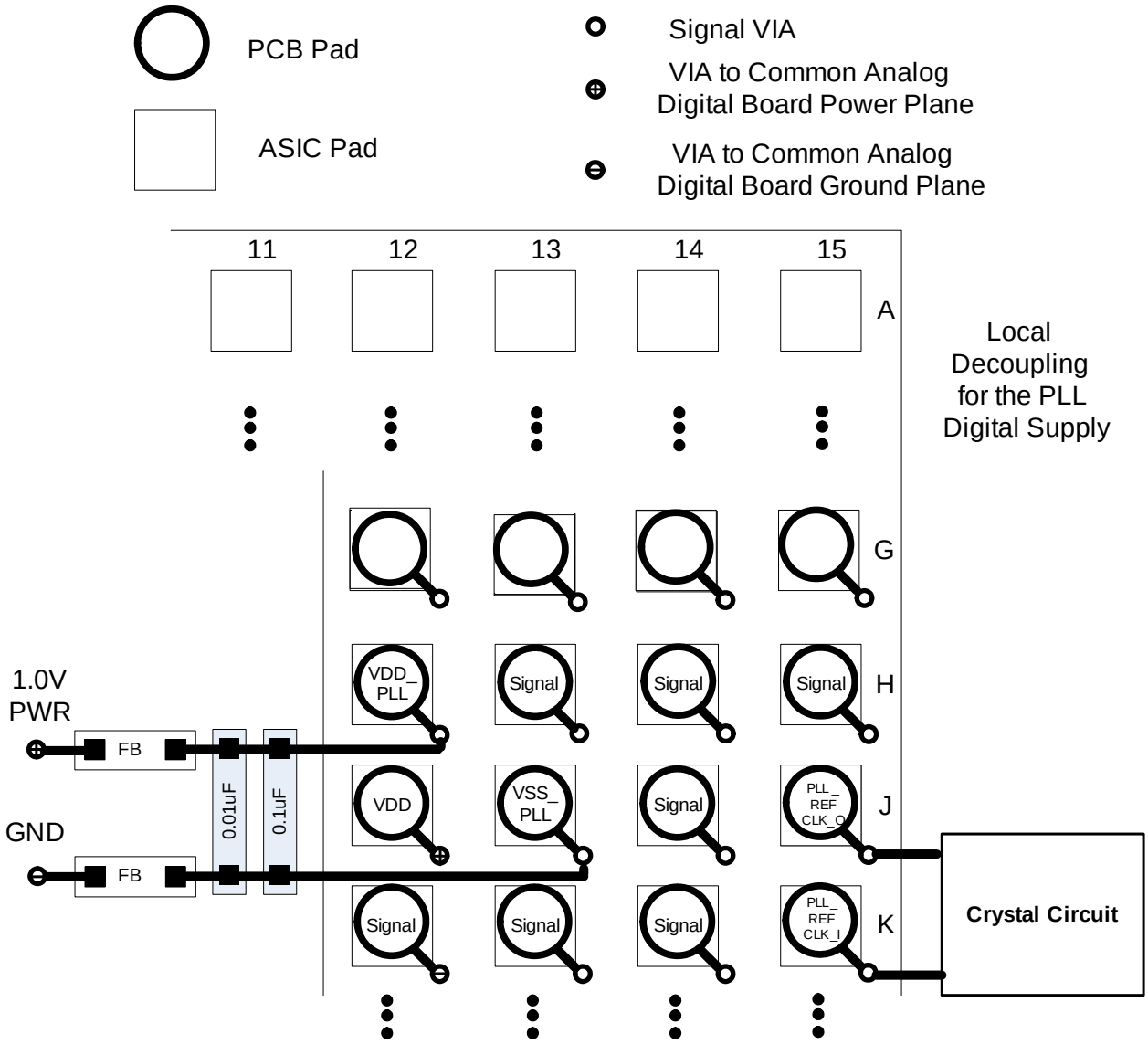


Figure 16. PLL Filter Layout

Reference Clock

The device requires an external reference clock to feed its internal PLL. This reference may be supplied via a crystal or oscillator. For flexibility, the DLPC2607 device accepts either of two reference clock frequencies (see Table 25), but both must have a maximum frequency variation of 200 ppm (including aging, temperature, and trim component variation). When a crystal is used, several discrete components are also required, as shown in Figure 17.

CL = Crystal load capacitance (Farads)
CL1 = 2 * (CL – Cstray_pll_refclk_i)
CL2 = 2 * (CL – Cstray_pll_refclk_o)

Where:
Cstray_pll_refclk_i = Sum of package and PCB srtay capacitance at the crystal pin associated with the ASIC pin pll_refclk_i.
Cstray_pll_refclk_o = Sum of package and PCB srtay capacitance at the crystal pin associated with the ASIC pin pll_refclk_o.

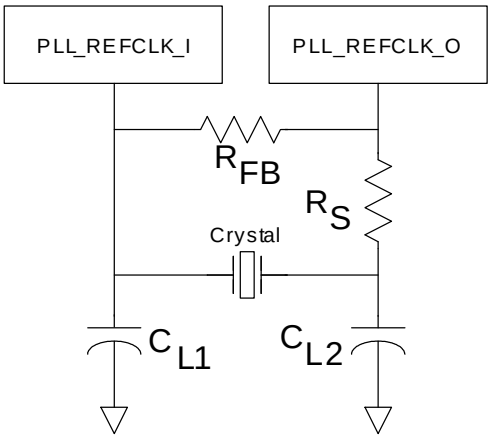


Figure 17. Recommended Crystal Oscillator Configuration

Table 25. Crystal Port Characteristics

PARAMETER	NOM	UNIT
PLL_REFCLK_I TO GND capacitance	4.5	pF
PLL_REFCLK_O TO GND capacitance	4.5	pF

Table 26. Recommended Crystal Configuration

PARAMETER	RECOMMENDED	UNIT
Crystal circuit configuration	Parallel resonant	
Crystal type	Fundamental (first harmonic)	
Crystal nominal frequency	16.667 or 8.333	MHz
Crystal frequency tolerance (including accuracy, temperature, aging and trim sensitivity)	± 200	PPM
Crystal drive level	100 max	uW
Crystal equivalent series resistance (ESR)	80 max	Ω
Crystal load	12	pF
R_S drive resistor (nominal)	100	Ω
R_{FB} feedback resistor (nominal)	1	MΩ
C_{L1} external crystal load capacitor	See Figure 17	pF
C_{L2} external crystal load capacitor	See Figure 17	pF
PCB layout	A ground isolation ring around the crystal is recommended	

If an external oscillator is used, then the oscillator output must drive the PLL_REFCLK_I pin on the DLPC2607 ASIC, and the PLL_REFCLK_O pins should be left unconnected. The benefit of an oscillator is that it can be made to provide a spread-spectrum clock that reduces EMI.

NOTE

The DLPC2607 device can only accept between 0% to –2% spreading (that is, down spreading only) with a modulation frequency between 20 and 65 kHz and a triangular waveform.

Similar to the crystal option, the oscillator input frequency is limited to 16.667 or 8.333 MHz. To configure the DLPC2607 device to accept the 8.333 MHz reference clock option, an external pullup resistor to VCC18 must be applied to the TSTPT (6) pin. To configure the DLPC2607 device to accept the 16.667 MHz reference clock option, the TSTPT (6) pin should be left unconnected.

It is assumed that the external crystal or oscillator stabilizes within 50 ms after stable power is applied.

General Handling Guidelines for Unused CMOS-Type Pins

To avoid potentially damaging current caused by floating CMOS input-only pins, TI recommends that unused ASIC input pins be tied through a pullup resistor to its associated power supply or a pulldown to ground. For ASIC inputs with internal pullup or pulldown resistors, it is unnecessary to add an external pullup or pulldown unless specifically recommended.

NOTE

Internal pullup and pulldown resistors are weak and should not be expected to drive the external line. The DLPC2607 device implements very few internal resistors and these are noted in the pin list.

Unused output-only pins should never be tied directly to power or ground but can be left open.

When possible, TI recommends that unused bidirectional I/O pins be configured to their output state such that the pin can be left open. If this control is not available and the pins may become an input, then they should be pulled-up (or pulled-down) using an appropriate, dedicated resistor.

Internal Processor Debug Support

The DLPC2607 device contains two internal 8051 microcontrollers, which share the same UART-like Debug port. This port only consists of two signals: UART Transmit Data (TXD) and UART Receive Data (RXD). When JTAGRSTZ is held low (that is, JTAG is held in reset), the JTAG, Serial Data In signal (JTAGTDI) can be re-used for RXD. Likewise the Debug Test signal TSTPT_0 signal can be used for TXD. To aid system bring-up and troubleshooting, auto-initialization software defaults operation such that this UART port is enabled and functionally connected to the Initialization and Command Processor (ICP).

Serial Flash Interface

The DLPC2607 device uses an external SPI serial flash memory device for configuration support. The minimum required size is dependent on the desired minimum number of sequences, CMT tables, and splash options while the maximum supported is 16 Mb. Table 27 provides the list of the configuration options.

Table 27. Serial Flash Support Features by Density(1)

Target Flash Density (Mbit)	Quantity of Features That can be Supported						
	Optical Test Splash Screens	Standard Splash Screens	Series Data Sector	Unit Data Sector	ODM Data Sector	DLP® Display Sequences (2)	CMT Tables per Sequence (3)
4M-bit	0	1	1	1	1	16	7
8M-bit	0	3	1	1	1	16	7
16M-bit	1	4	1	1	1	16	7

(1) All rows in this table have passed DVT at TI
(2) Assumes individual DLP® Display Sequences are limited to 5 KBytes each
(3) An equal number of CMT tables are require for each Sequence (CMT tables define the DeGamma Curve) The DLPC2607 device uses a single SPI interface, employing SPI mode 0 protocol, operating at a frequency of 33.3 MHz. It supports two independent SPI chip selects. However, the primary flash must be connected to SPI chip select 0 (SPICS0). This is because the Auto-Initialization routine is always executed from the device connected to this chip select. The Auto-initialization routine executed from flash consists of the following:
  (a) The DLPC2607 device first uploads the size and location of the Auto-Initialization routine from address range 0x0000 thru 0x0007 of the serial flash memory connected to SPICS0.
  (b) The DLPC2607 device then uploads the actual Auto-Initialization routine to its ICP program memory from the serial flash memory connected to SPICS0.
  (c) The DLPC2607 device then executes an Auto-Init routine which includes uploading default control parameter values, uploading mailbox memory contents, turning on the Sequence and LEDs and then enabling the display.
  (d) Upon completion of the Auto-Initialization routine, the DLPC2607 signals INIT DONE via GPIO4_INTF

The DLPC2607 device should support any flash device that is compatible with these modes of operation. However, the DLPC2607 device does not support the Normal (slow) Read Opcode, and thus cannot automatically adapt protocol and clock rate based on the flash's electronic signature ID. The flash instead uses a fixed SPI clock and assumes certain attributes of the flash have be ensured by PCB design. The DLPC2607 device also assumes the flash supports address auto-incrementing for all read operations. The specific Instruction OpCode and Timing Compatibility requirements for a DLPC2607 device compatible flash are listed in Table 28 and Table 29.

Table 28. SPI Flash Instruction OpCode and Timing Compatibility Requirements

SPI Flash Command	OPCODE (hex)	Address Bytes	Dummy Bytes	Min Clock Rate
Fast READ (Single Output)	0x0B	3	1	33.3 MHz
All others	can vary	can vary	can vary	33.3 MHz

Table 29. SPI Flash Key Timing Parameter Compatibility Requirements

SPI Flash Timing Parameter	MIN	MAX
Minimum Chip Select High Time		300 ns
Minimum Output Hold Time	0 ns	
Maximum Output Valid Time		9 ns
Minimum Data In Setup Time		5 ns
Minimum Data In Hold Time		5 ns

The DLPC2607 device does not have any specific page, block, or sector size requirements, except that programming via the I^2C interface requires the use of page mode programming. However, if the user would like to use a portion of the serial flash for storing external data (such as calibration data) via the I^2C interface, then the minimum sector size needs to be considered as it drives minimum erase size. Note that use of serial flash for storing external data may impact the number of features that can be supported.

NOTE

The DLPC2607 device does not drive the $\overline{\text{HOLD}}$ (active low hold) or $\overline{\text{WP}}$ (active low Write Protect) pins on the flash device; thus, these pins should be tied to a logic high on the PCB via an external pullup.

The DLPC2607 device supports 1.8, 2.5, or 3.3-V serial flash devices. To do so, VCC_FLSH must be supplied with the corresponding voltage. Table 30 contains a list of 1.8, 2.5, and 3.3-V compatible SPI serial flash devices supported by the DLPC2607 device.

Table 30.

DVT(1)	Density (M-bits)	Vendor	Part Number(2)	Supply Voltage Supported(3)	Min Chip Select High Time (t_{CSH})	Max Fast Read Freq(4)	OpCode and Timing CompatibleTable 28
1.8-V Compatible Devices							
Yes	4M-bit	Macronix	MX25U4035	1.65 to 2 V	30 ns	40 MHz	Yes
Yes	8M-bit	Macronix	MX25U8035	1.65 to 2 V	30 ns	40 MHz	Yes
2.5-V (and 3.3-V) Compatible Devices							
No	4M-bit	Winbond	W25X40BLxxxx	2.3 to 3.6 V	100 ns	50 MHz	Yes
Yes	16M-bit	Winbond	W25Q16BLxxxx	2.3 to 3.6 V	100 ns	50 MHz	Yes
No	16M-bit	Winbond	W25X16ALxxxx (5)	2.3 to 3.6 V	100 ns	50 MHz	Yes
Additional 3.3-V Only Compatible Devices							
Yes	8M-bit	Macronix	MX25L8005ZUx-xxG	2.7 to 3.6 V	100 ns	66 MHz	Yes

(1) These flash devices appear compatible with the DLPC2607 device, but only those marked with "yes" in the DVT column have been validated on a TI internal reference design board. Those marked with "no" can be used at the ODM's own risk.
(2) Lower case 'x' is used as a wild card placeholder and indicates an option that is selectable by the user. Note that the use of an upper case 'X' is part of the actual part number.
(3) The flash supply voltage must match VCC_FLSH on the DLPC2607 device. 1.8 and 2.5-V SPI device options are limited. Take care when ordering devices to be sure the desired supply voltage is attained, as multiple voltage options are often available under the same base part number.
(4) Max supported Fast Read Frequency at the min supported supply voltage.
(5) The manufacturer has issued an upcoming end of life notice on this device.

Serial Flash Programming

The flash can be programmed through the DLPC2607 device over I^2C (for directions, see the DLPC2607 Software Programmer's Guide, DLPU013) or by driving the SPI pins of the flash directly while the DLPC2607 device I/O are 3-stated. SPICLK, SPIDOUT, and SPICZ0 I/O can be 3-stated by holding $\overline{\text{RESET}}$ in a logic low state while power is applied. Note that SPICSZ1 is not 3-stated by this same action.

SPI Signal Routing

The DLPC2607 device is designed to support two SPI slave devices; specifically a serial flash and the PMD1000. Given this requires routing associated SPI signals to two locations while attempting to operate at 33.3 MHz, take care to ensure that reflections do not compromise signal integrity. TI recommends the following:

- The SPICLK PCB signal trace from the DLPC2607 source to each slave device should be split into separate routes as close to the DLPC2607 device as possible. In addition, the SPICLK trace length to each device should be equal in total length.
- The SPIDOUT PCB signal trace from the DLPC2607 source to each slave device should be split into separate routes as close to the DLPC2607 device as possible. In addition, the SPIDOUT trace length to each device should be equal in total length (that is, use the same strategy as SPICLK).
- The SPIDIN PCB signal trace from each slave device to the point where they intersect on their way back to the DLPC2607 device should be made equal in length and as short as possible. They should then share a common trace back to the DLPC2607 device.
- SPICSZ0 and SPICSZ1 need no special treatment as they are dedicated signals which drive only one device.

Mobile-DDR DRAM Compatibility

The following are the basic SDRAM compatibility requirements for the DLPC2607 SDRAM:

- SDRAM Memory Type: mobile-DDR (mDDR)
- Size: 128 Mbit minimum
- Organization: N × 16-bits wide × 4 banks
- Speed Grade t_{CK}: 6-ns max
- CAS Latency (CL), t_{RCD},t_{RP} parameters (Clocks): 3, 3, 3
- Burst Length options to include: Burst of 4
- Refresh period (full device): ≥ 64 ms

The following mobile-DDR DRAM devices are recommended for use with the DLPC2607 device:

Table 31. Compatible mobile DDR DRAM Device Options(1)(2)

DVT(3)	Vendor	Part Number	Size	Organization	Speed Grade t_{CK} (4)	C_L, t_{RCD}, t_{RP}(Clocks)
No	Elpida	EDK1216CFBJ-60-F (5)	128 Mbit	8 M × 16	6 ns	3, 3, 3
Yes	Elpida	EDD25163HBH-6ELS-F	256 Mbit	16 M × 16	6 ns	3, 3, 3
No	Samsung	K4X56163PL-FGC6 (6)	256 Mbit	16 M × 16	6 ns	3, 3, 3
Yes	Samsung	K4X56163PN-FGC6	256 Mbit	16 M × 16	6 ns	3, 3, 3
Yes	Micron	MT46H16M16LFBF-6IT:H	256 Mbit	16 M × 16	6 ns	3, 3, 3
Yes	Hynix	H5MS2562JFR-J3M	256 Mbit	16 M × 16	6 ns	3, 3, 3

(1) The DLPC2607 device does not use partial array self-refresh or temperature compensated self-refresh options.
(2) These part numbers reflect Pb-free package.
(3) All the SDRAM devices above appear compatible with the DLPC2607 device, but only those marked with “yes” in the DVT column have been validated on a TI internal reference design board. Those marked with “no” can be used at the ODM’s own risk.
(4) A 6-ns speed grade corresponds to a 166-MHz mDDR device.
(5) These devices are EOL and no replacement with the same footprint. They should not be used in new designs.
(6) The manufacturer has issued an upcoming end of life notice on this device.

Mobile-DDR Memory and DMD Interface Considerations

High-speed interface waveform quality and timing on the DLPC2607 ASIC (that is, the Mobile DDR Memory I/F and the DMD Interface) are dependent on the total length of the interconnect system, the spacing between traces, the characteristic impedance, etch losses, and how well matched the lengths are across the interface. Thus, ensuring positive timing margin requires attention to many factors.

As an example, the DMD interface system timing margin can be calculated as follows:

Setup Margin = (DLPC2607 output setup) – (DMD input setup) – (PCB routing mismatch) – (PCB SI degradation)

Hold-time Margin = (DLPC2607 output hold) – (DMD input hold) – (PCB routing mismatch) – (PCB SI degradation)

Where PCB SI degradation is signal integrity degradation due to PCB affects, which includes such things as simultaneously switching output (SSO) noise, cross-talk, and inter-symbol interference (ISI) noise.

The DLPC2607 device I/O timing parameters, as well as Mobile-DDR and DMD I/O timing parameters, can be found in their corresponding data sheets. Similarly, PCB routing mismatch can be easily budgeted and met via controlled PCB routing. However, PCB SI degradation is not so straight forward.

In an attempt to minimize the signal integrity analysis that would otherwise be required, the following PCB design guidelines are provided as a reference of an interconnect system that satisfies both waveform quality and timing requirements (accounting for both PCB routing mismatch and PCB SI degradation). Variation from these recommendations may also work but should be confirmed with PCB signal integrity analysis or lab measurements.

PCB Design:

o Configuration:	Asymmetric Dual Stripline
o Etch Thickness (T):	0.5 oz copper
o Single-Ended Signal Impedance	50 Ω (±10%)
o Differential Signal Impedance:	100 Ω differential (± 10%)

PCB Design:

o Reference plane 1 is assumed to be a ground plane for proper return path	
o Reference plane 2 is assumed to be the I/O power plane or ground	
o Dielectric FR4, (Er):	4.2 (nominal)
o Signal trace distance to reference plane 1 (H1)	5 mil (nominal)
o Signal trace distance to reference plane 2 (H2)	34.2 mil (nominal)

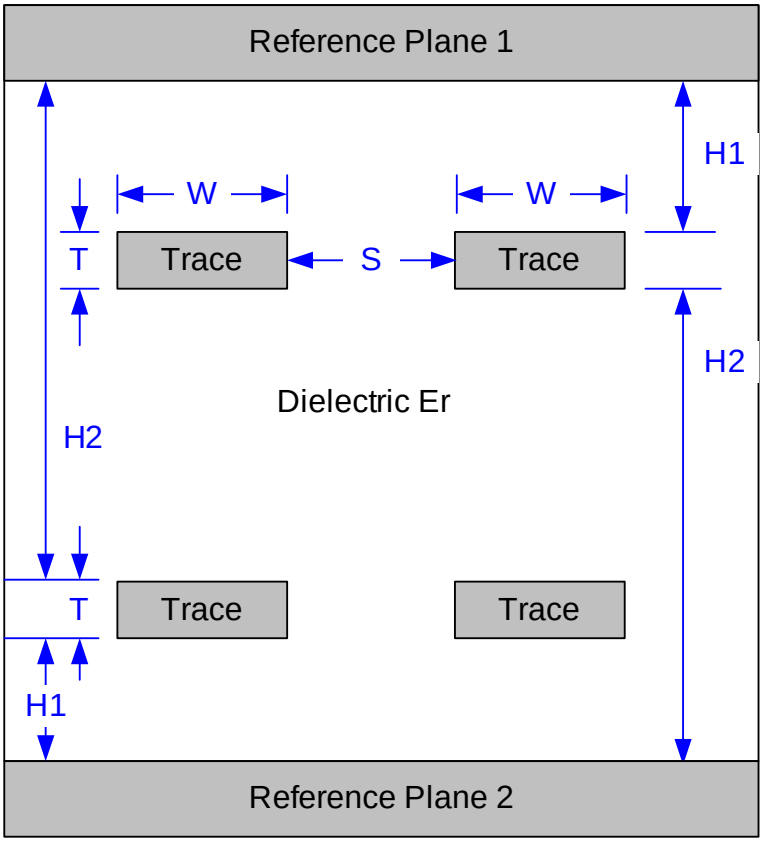


Figure 18. PCB Stacking Geometries

General PCB Routing (Applies to All Corresponding PCB Signal)

Table 32. PCB Line and Spacing Recommendations(1)(2)(3)

Parameter	Application	Single Ended Signals	Differential Pairs	Unit
Line width (W)	Escape routing in ball field	3 (0.762)	3 (0.762)	mil (mm)
	PCB Etch – Outer layer Data or Control	7.25 (0.184)	4.5 (0.114)	mil (mm)
	PCB Etch - Inner layer Data or Control	4.5 (0.114)	4.5 (0.114)	mil (mm)
	PCB Etch Clocks	4.5 (0.114)	4.5 (0.114)	mil (mm)
Differential signal pair spacing (S)	PCB Etch Data or Control	N/A	7.75 [1] (0.305)	mil (mm)
	PCB Etch Clocks	N/A	7.75 [1] (0.305)	mil (mm)

(1) Spacing may vary to maintain differential impedance requirements.
(2) The DLPC2607 device only includes one differential signal pair – MEM0_CK_P/ MEM0_CK_N.
(3) These values are merely recommendations to achieve good signal integrity. The OEM is free to apply their own rules as long as they maintain good signal integrity.

Table 32. PCB Line and Spacing Recommendations(1)(2)(3) (continued)

Parameter	Application	Single Ended Signals	Differential Pairs	Unit
Minimum Line spacing to other signals (S)	Escape routing in ball field	3 (0.762)	3 (0.762)	mil (mm)
	PCB Etch – Outer layer Data or Control	7.25 (0.184)	4.5 (0.114)	mil (mm)
	PCB Etch - Inner layer Data or Control	4.5 (0.114)	4.5 (0.114)	mil (mm)
	PCB Etch Clocks	11 (0.279)	11 (0.279)	mil (mm)
Maximum Differential pair P-to-N length mismatch	Total Clock	N/A	25 (0.635)	mil (mm)

These PCB design guidelines are purposefully conservative in order to minimize potential signal integrity issues. Given this device is targeted for low-cost, handheld application, there is a need to be more aggressive with these best practices. TI highly recommends that a full board level signal integrity analysis be performed, if these guidelines cannot be followed. The DLPC2607 IBIS models are available for such analysis.

Maximum, Pin-to-Pin, PCB Interconnects Etch Lengths:

Table 33. Max Pin-to-Pin PCB Interconnect Recommendations(1)(2)

Bus	Signal Interconnect Topology		Unit
	Single Board Signal Routing Length	Multi-Board Signal Routing Length	
DMD			
DMD_D(14:0), DMD_DCLK, DMD_TRC, DMD_SCTRL, DMD_LOADB, DMD_OEZ DMD_DAD_STRB, DMD_DAD_BUS, DMD_SAC_CLK and DMD_SAC_BUS	4 max (101.5 max)	3.5 max (88.91 max)	inch (mm)
Mobile DDR			
MEM0_DQ(15:8), MEM0_UDM and MEM0_UDQS	1.5 max 38.1 max	NA	inch (mm)
Mobile DDR			
MEM0_DQ(7:0), MEM0_LDM and MEM0_LDQS	1.5 max (38.1 max)	NA	inch (mm)
Mobile DDR			
MEM0_CK_P, MEM0_CK_N, MEM0_A(12:0), MEM0_BA(1:0), MEM0_CKE, MEM0_CSZ, MEM0_RASZ, MEM0_CASZ and MEM0_WEZ	2.5 max (63.5 max)	N/A	inch (mm)

(1) Max signal routing length includes escape routing.
(2) Multi-board DMD routing length is more restricted due to the impact of the connector.

I/F Specific PCB Routing:

Table 34. High Speed PCB Signal Routing Matching Requirements(1)(2)(3)

Signal Interconnect Topology				
IF	**Single Group**	**Reference Signal**	**Max Mismatch**	**Unit**
DMD	DMD_D(14:0), DMD_TRC, DMD_SCTRL, DMD_LOADB, DMD_OEZ	DMD_DCLK	± 500 (± 12.7)	mil (mm)
	DMD_DAD_STRB, DMD_DAD_BUS	DMD_DCLK	± 750 (± 19.05)	mil (mm)
	DMD_SAC_BUS	DMD_SAC_CLK	± 750 (± 19.05)	mil (mm)
	DMD_SAC_CLK	DMD_DCLK	± 500 (± 12.7)	mil (mm)
Mobile DDR:	MEM0_CLK_P	MEM0_CLK_N	± 150 (± 3.81)	mil (mm)
	Read/ Write Data Lower Byte: MEM0_LDM and MEM0_DQ(7:0) 38.1 max	MEM0_LDQS	± 300 (± 7.62)	mil (mm)
	Read/ Write Data Upper Byte: MEM0_UDM and MEM0_DQ(15:8)	MEM0_UDQS	± 300 (± 7.62)	mil (mm)
	Address and Control: MEM0_A(12:0), MEM0_BA(1:0), MEM0_RASZ , MEM0_CASZ, MEM0_WEZ, MEM0_CSZ, MEM0_CKE	MEM0_CLK_P/ MEM0_CLK_N	± 1000 (± 25.4)	mil (mm)
	Data Strobes: MEM0_LDQS and MEM0_UDQS	MEM0_CLK_P/ MEM0_CLK_N	± 300 (± 7.62)	mil (mm)

(1) These values apply to PCB routing only. They do not include any internal package routing mismatch associated with the DLPC2607 device, DMD, or mDDR memory.
(2) DMD data and control lines are double data rate, whereas DMD_SAC and DMD_DAD lines are single data rate. Matching of the double data rate lines is more critical and should take precedence over matching single data rate lines.
(3) Mobile DDR data, mask, and strobe lines are double data rate, whereas address and control are single data rate. Matching of the double data rate lines is more critical and should take precedence over matching single data rate lines.

Number of layer changes:

- Single-ended signals: Minimize the number of layer changes.
- Differential signals: Individual differential pairs can be routed on different layers but the signals of a given pair should not change layers.

Stubs:

- Stubs should be avoided.

Termination Requirements:

DMD I/F

All DMD I/F signals, with the exception of DMD_OEZ (specifically DMD_D(14:0), DMD_DCLK, DMD_TRC, DMD_SCTRL, DMD_LOADB, DMD_DAD_STRB, DMD_DAD_BUS, DMD_SAC_CLK, and DMD_SAC_BUS), should be terminated at the source with a 10 to 30-Ω series resistor. A 30-Ω series resistor is recommended for most applications as this minimizes overshoot, undershoot, and reduces EMI; however, for systems that must operate below –20°C, it may be necessary to reduce this series resistance in order to avoid narrowing the data eye too much under worse case PVT conditions. IBIS simulations are recommended for this worse case scenarios.

Mobile DDR Memory I/F

mDDR differential Clock	Specifically MEM0_CK(P:N), each line should be terminated at the source with a 30-Ω series resistor. The pair should also be terminated with an external 100-Ω differential termination across the two signals as close to the DRAM as possible. (It may be possible to use a 200-Ω differential termination at the DRAM to save power while still providing sufficient signal integrity, but this has not been validated.)
mDDR Data, Strobe and Mask	Specifically MEM0_DQ(15:0), MEM0_LDM, MEM0_UDM, MEM0_LDQS and MEM0_UDQS should be terminated with a 30-Ω series resistor located midway between the two devices.
mDDR Address and Control	Specifically MEM0_A(12:0), MEM0_BA(1:0), MEM0_CKE, MEM0_CSZ, MEM0_RASZ, MEM0_CASZ, and MEM0_WEZ should be terminated at the source with a 30-Ω series resistor.

For applications where the routed distance of the mDDR or DMD signal can be kept less than 0.75 inches, this signal is short enough not be considered a transmission line and should not need a series terminating resistor.

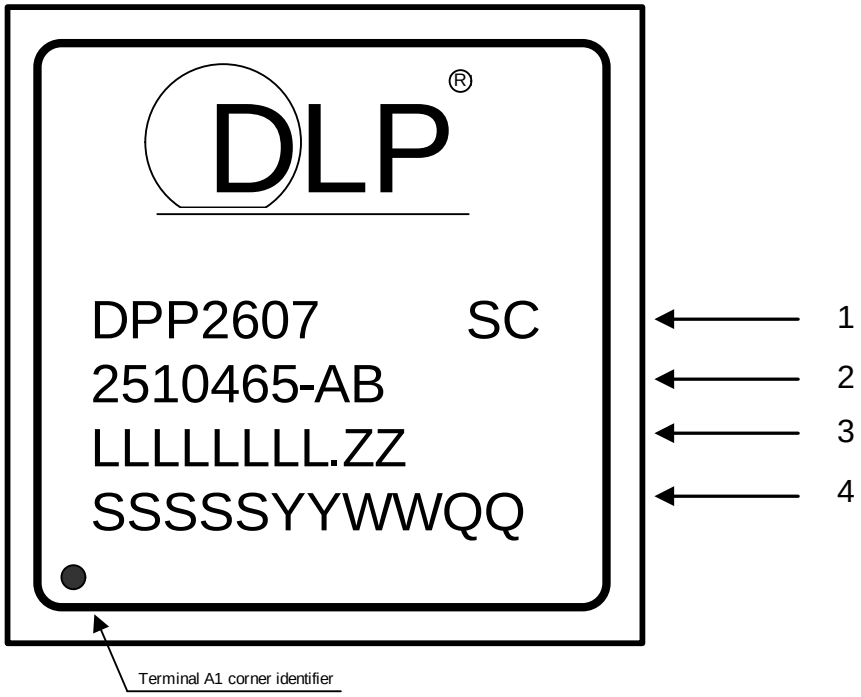
Functional Limitations

There are several function limitations in the DLPC2607 device that should be noted. Table 35 is a summary of those limitations along with associated recommendations:

Table 35.

Topic	Limitation	Recommendation
Interlaced Video	Interlaced video is only supported via BT.656 port configuration (Only 16-bit 4:2:2 YCrCb is supported via this I/F).	
YCrCb	The DLPC2607 device does not support any source with an odd number of active pixels per line if the source is configured to a YCrCb format (that is, landscape 853 × 480 and 427 × 240).	Use 852 × 480 or 854 × 480 source in its place
Unsupported Source or Display	The DLPC2607 device cannot display a QWVGA portrait source in a non-rotated orientation on a WVGA or VGA DMD.	Can support a rotated display that fills the screen

Device Marking



Marking Definitions:

1. DLP Device Name

   SC: Solder ball Composition

   e1: indicates lead-free solder balls consisting of SnAgCu

   G8: indicates lead-free solder balls consisting of tin-silver-copper (SnAgCu) with silver content less than or equal to 1.5% and that the mold compound meets TI's definition of “green”

2. TI Part Number

   AB (1 or 2 alpha-numeric) = ‘A’ corresponds to the TI device dash number. ‘B’ is reserved for unqualified device marking. All unqualified device, including prototypes and skew lot samples, are labeled with the letter “X” in the ‘B’ marking location (following the TI part number). ‘B’ is left blank for qualified devices.

3. LLLLLLLL.ZZ Foundry Lot Code for Semiconductor Wafers and Lead-free Solder Ball Marking

   LLLLLLLL: Manufacturing Lot code

   ZZ: Lot Split Number

4. SSSSSYYWWQQ Package and Assembly information

   SSSSS: Manufacturing Site

   YYWW: Date Code (YY = Year :: WW = Week)

   QQ: Qualification level Option – Engineering samples are marked in this field with an “ES” suffix.

   For example, KOREA0914ES would be engineering samples built in Korea the 14th week of 2009

Qualification Limits

At this time, this device is qualified for use for only a subset of functionality defined earlier in this specification. Full qualification will be completed at a later date. The following qualification limits apply:

Table 36. Qualification Limits

Function or Attribute	Qualification Limits	Notes
Command I/F	I^2C only	DBI-C is not supported for commands.
Reference Clock source	8.33-MHz or 16.67-MHz crystal, or oscillator without spread spectrum	There are no plans to qualify oscillator with spread spectrum operation.

REVISION HISTORY

Changes from Original (December 2013) to Revision A **Page**

- Corrected columns for I_{OH} and I_{OL} in Table 13 13
- Updated B38 I/O Type value for V_{OH} (min) in Table 13 13
- Added additional table notes to Table 13 13
- Added table note to Table 14 13
- Corrected device reference to DLPC2607 in the notes for Table 23 24

Changes from Revision A (December 2013) to Revision B **Page**

- Removed product preview banner 1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLPC2607ZVB	ACTIVE	NFBGA	ZVB	176	260	TBD	Call TI	Call TI			Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

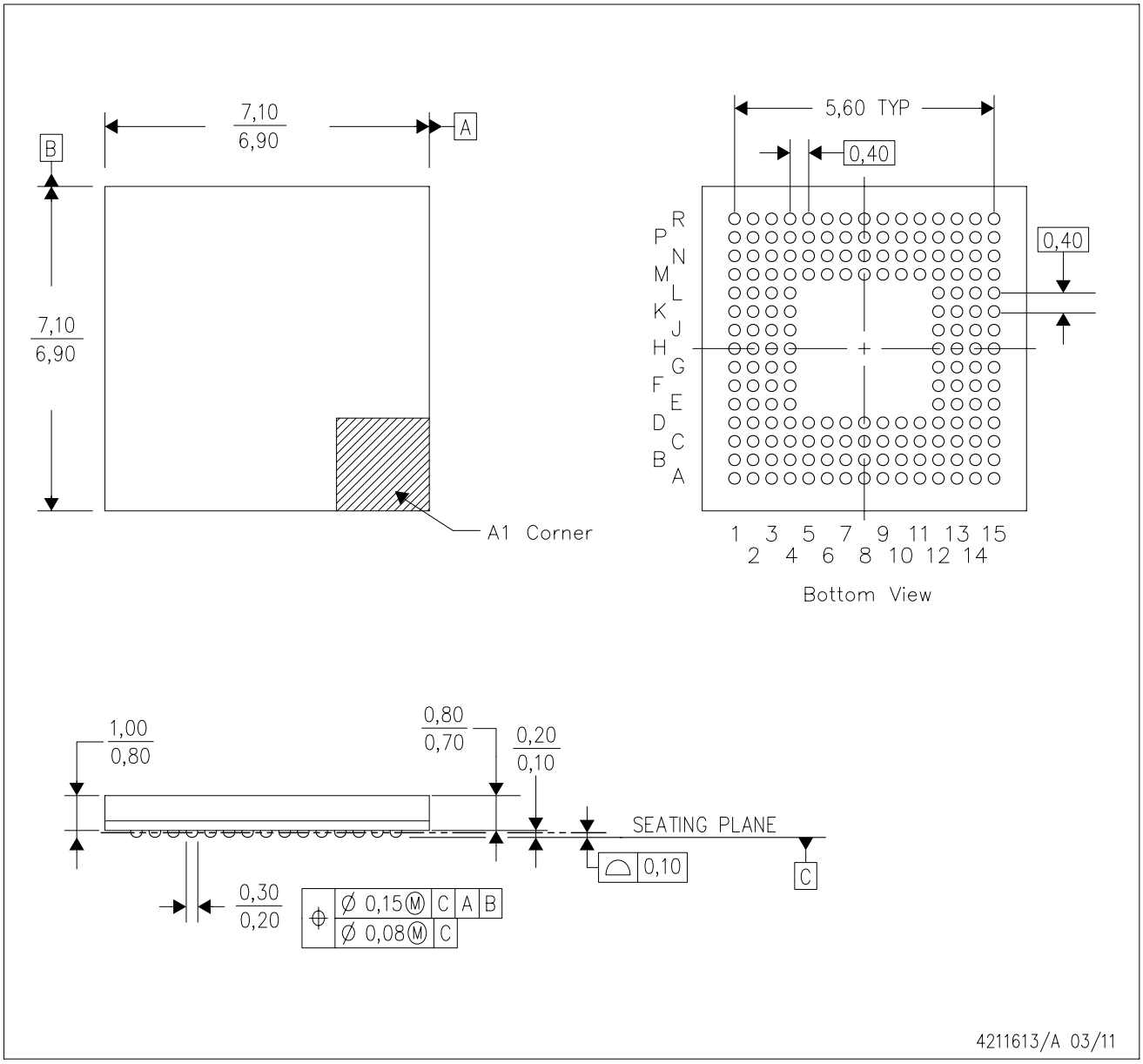
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

ZVB (S–PBGA–N176) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This package is Pb–free.

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