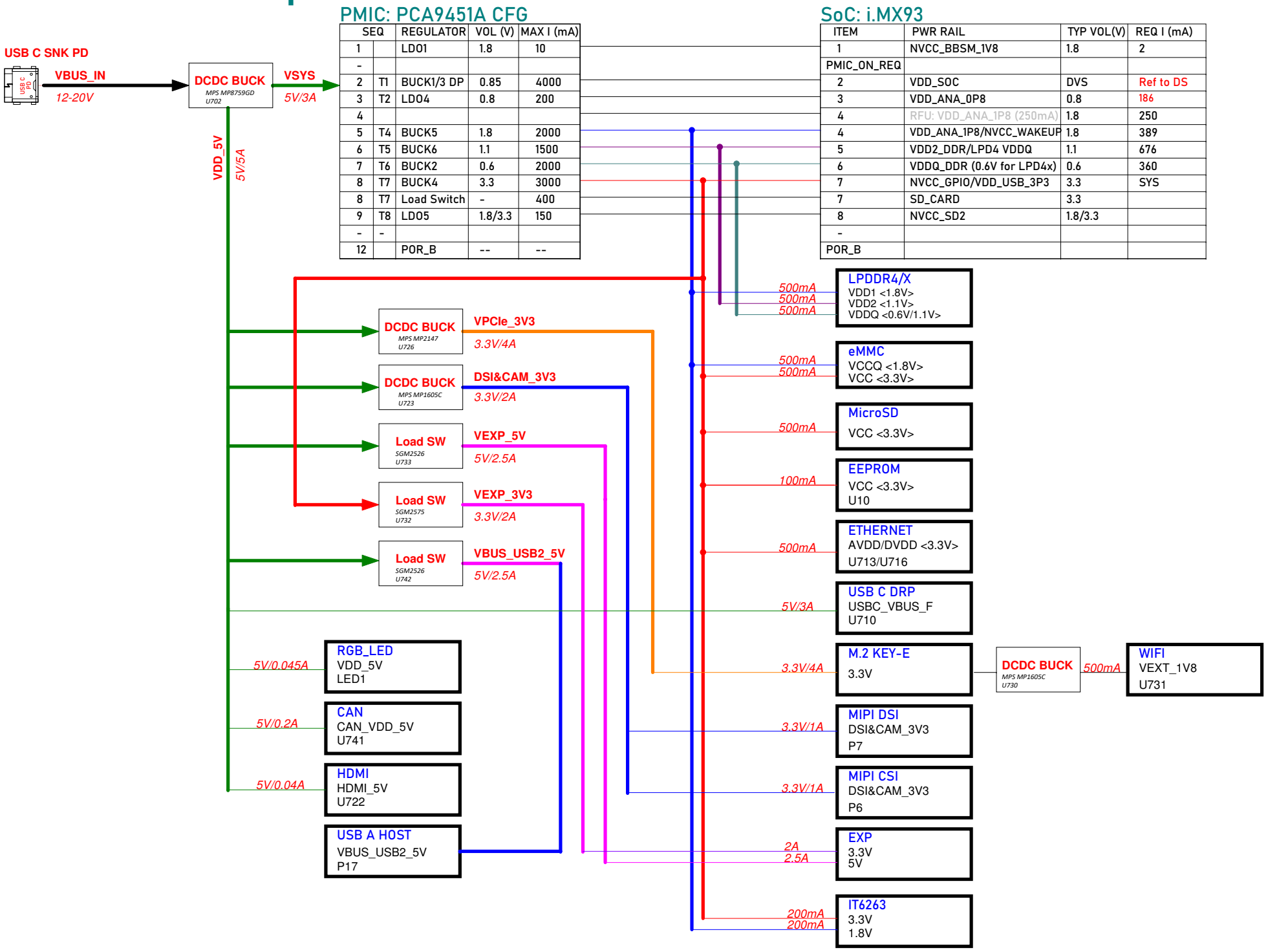
FRDM-i.MX 93 Development Board



PMIC: PCA9451A CFG

SEQ		REGULATOR	VOL (V)	MAX I (mA)
1		LDO1	1.8	10
-				
2	T1	BUCK1/3 DP	0.85	4000
3	T2	LDO4	0.8	200
4				
5	T4	BUCK5	1.8	2000
6	T5	BUCK6	1.1	1500
7	T6	BUCK2	0.6	2000
8	T7	BUCK4	3.3	3000
8	T7	Load Switch	-	400
9	T8	LDO5	1.8/3.3	150
-	-			
12		POR_B	--	--

SoC: i.MX93

ITEM	PWR RAIL	TYP VOL(V)	REQ I (mA)
1	NVCC_BBSM_1V8	1.8	2
PMIC_ON_REQ			
2	VDD_SOC	DVS	Ref to DS
3	VDD_ANA_0P8	0.8	186
4	RFU: VDD_ANA_1P8 (250mA)	1.8	250
4	VDD_ANA_1P8/NVCC_WAKEUP	1.8	389
5	VDD2_DDR/LPD4 VDDQ	1.1	676
6	VDDQ_DDR (0.6V for LPD4x)	0.6	360
7	NVCC_GPIO/VDD_USB_3P3	3.3	SYS
7	SD_CARD	3.3	
8	NVCC_SD2	1.8/3.3	
-			
POR_B			

FRDM-i.MX 93 Development Board

Table of Content

1. Interrupted lines coded with the same letter or letter combinations are electrically connected.

2. Device type number is for reference only. The number varies with the manufacturer.

3. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

4. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

Preliminary - Subject to Change without Notice!

This board was designed for maximum flexibility in software development and demonstrates multiple functions possible with i.MX processors. Although best design practices have been applied, some areas may not be suitable for a mass-production design.

Revision History

Rev. Code	Date	By	Description
A	*2024-05-16*	*FORLINX*	*Initial version.*
B	*2024-06-19*	*FORLINX*	*P13 power supply network VSD3V3 reconnected.* *PHYL_LED1_CFG_LDO0 Network Dropdown.* *Correct VDD_3V to VDD_3V3.* *Modify the default up and down status of ENET1 and ENET2 indicator lights.* *I2C3 multiplexing pin modified to GPIO_IO28 and GPIO_IO29.* *Assemble R2832, R2834, R2836, R2838 and remove R2833, R2835, R2837, R2839.* *Correct U719 IT6263 P14 network name to PCADR.* *U732 changed from SGM2526 to SGM2575.* *U733 P4 VCP pulled up to VIN through a 10K resistor.* *Assemble R2585 and change R2588 to a 20K.* *R3042, R3043 changed to 1MΩ.*
B1	*2024-10-10*	*NXP*	*Send to release.*

Microcontroller Product Group
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Classification: X

Designer: FORLINX	Drawing Title: **FRDM-IMX93**		
Drawn by: FORLINX	Page Title: **Title and Rev History**		
Approved: NXP SE	Size C	Document Number SCH-94611 PDF: SPF-94611	Rev B1
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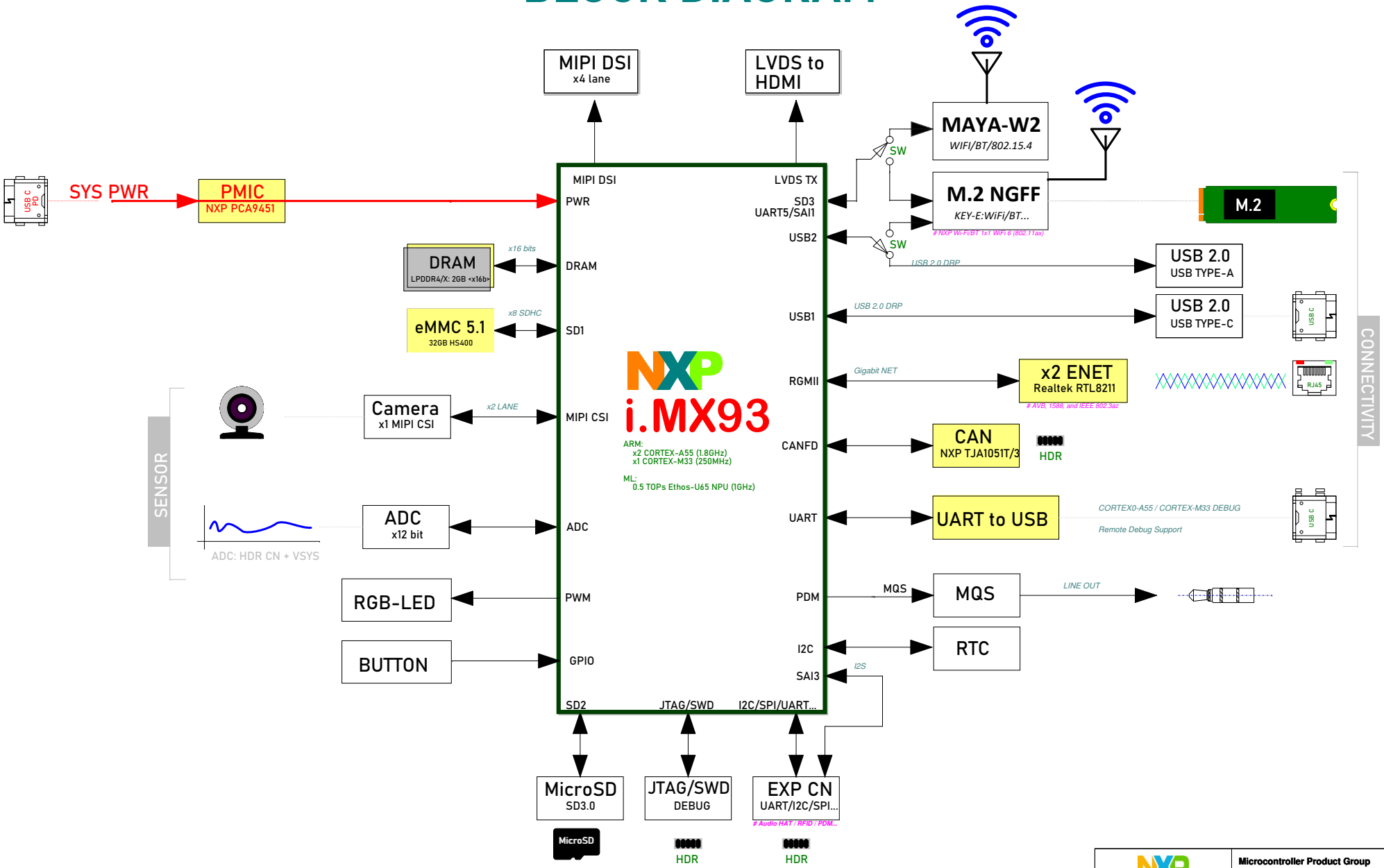
BLOCK DIAGRAM



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Classification: X		
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Drawn by: FORLINX	Page Title: Block Diagram	
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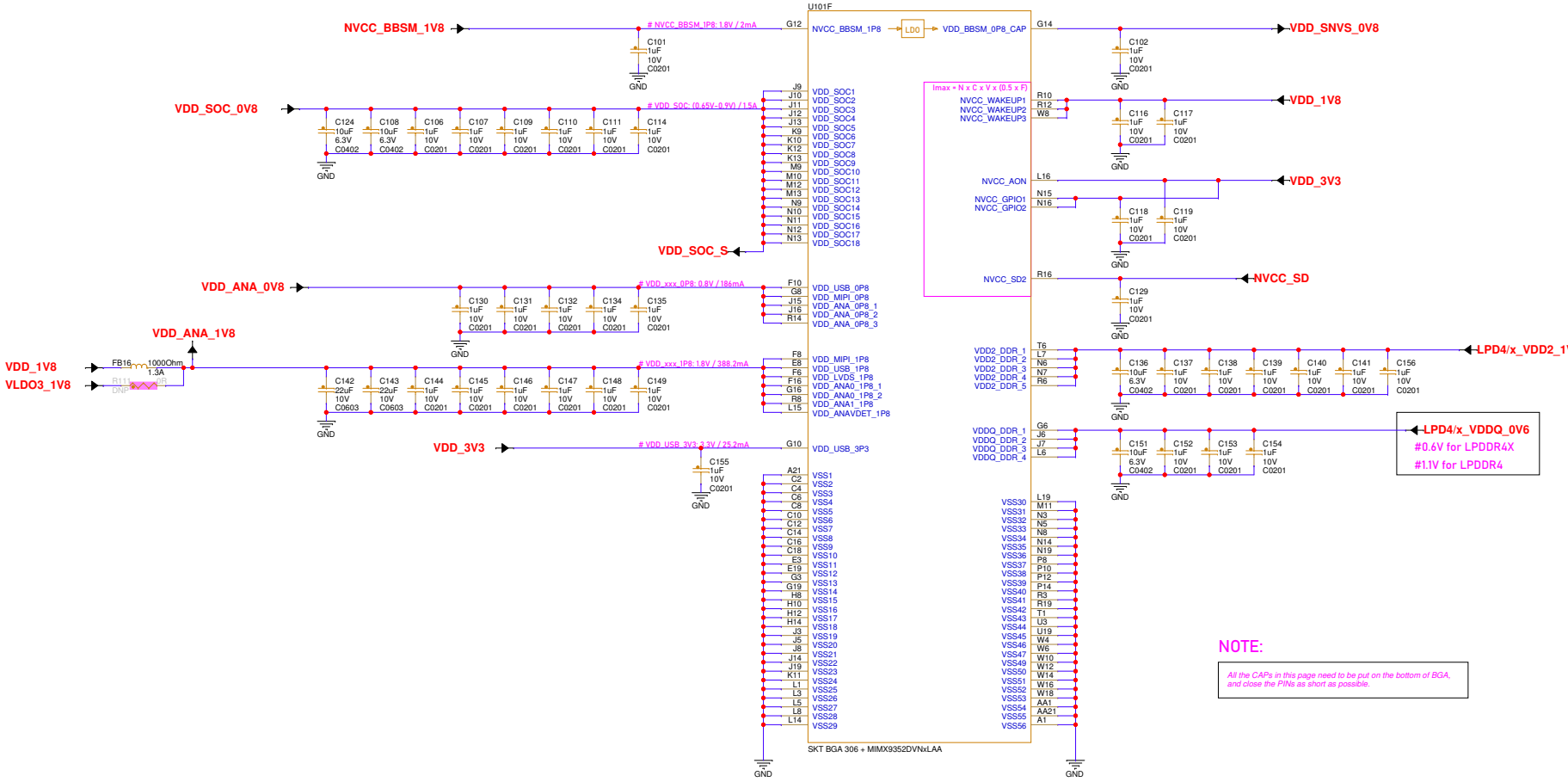
i.MX93 PWR



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Classification: <FCP> A <PUBI>

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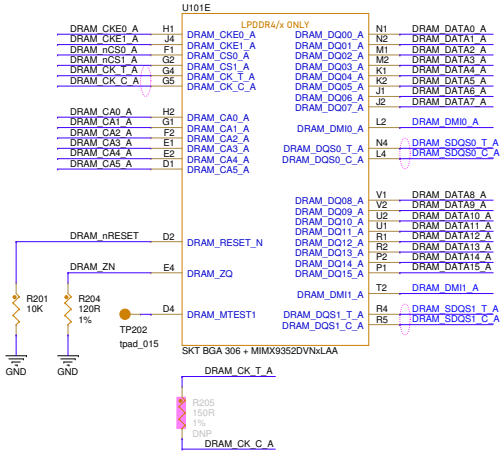
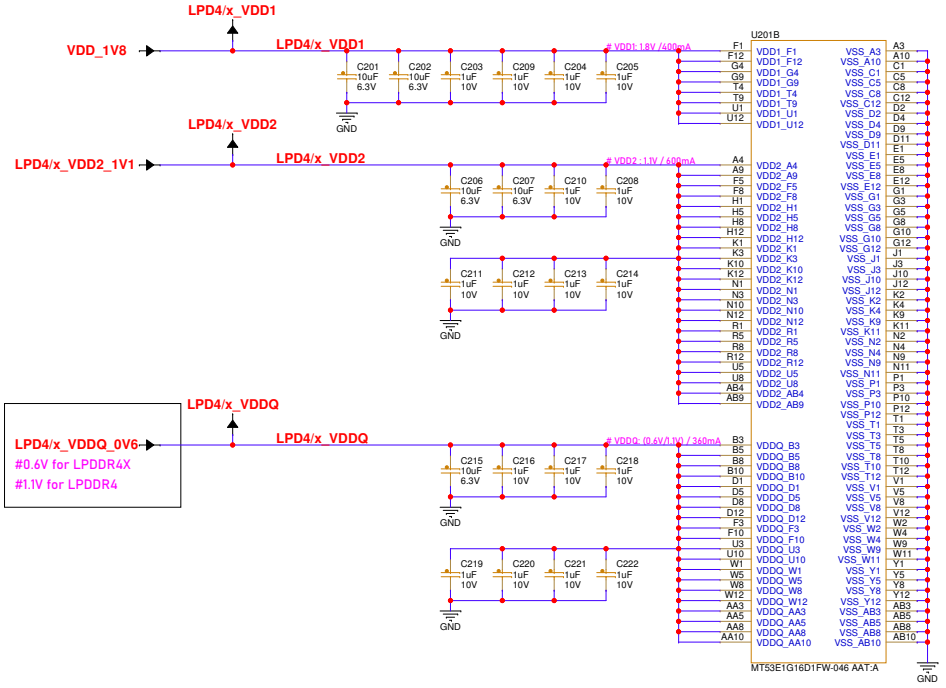
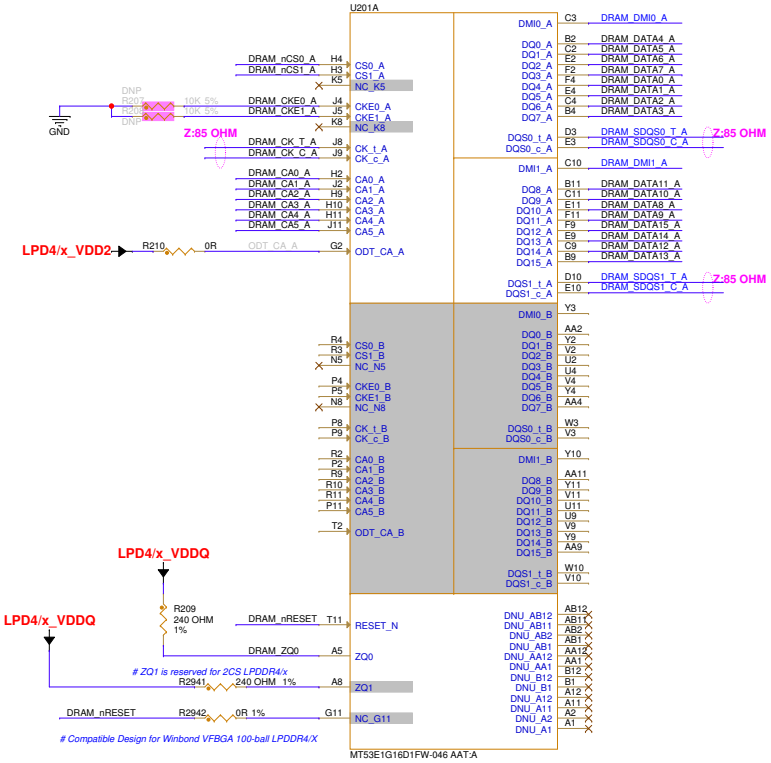
LPDDR4/X





LPDDR4X: 2GB (x16)



Power Supply Voltage Sequence:

RESET_n is held LOW.
VDD1 >= VDD2
VDD2 >= VDDQ-200mV

Power ramp duration tINIT0 (Tb-Ta) must not exceed 20ms.

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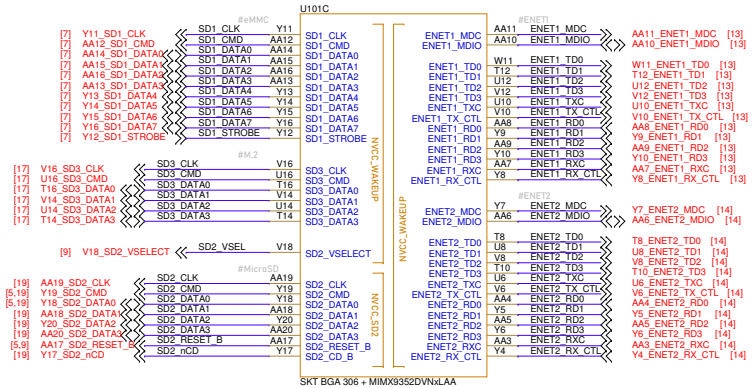
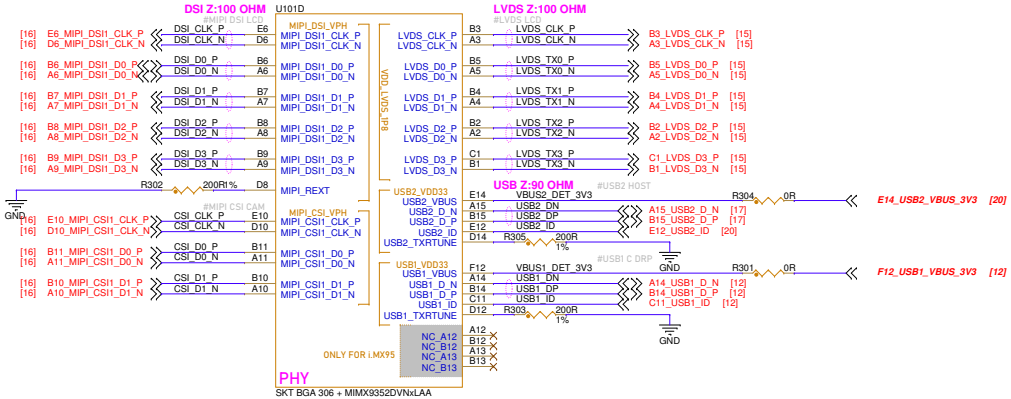
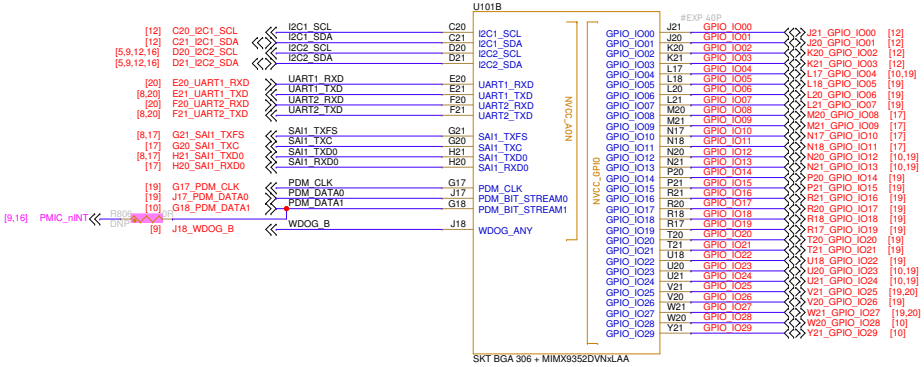
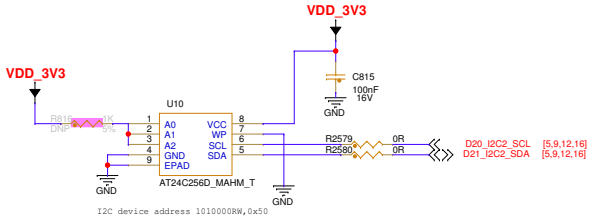
i.MX93 IO/PHY









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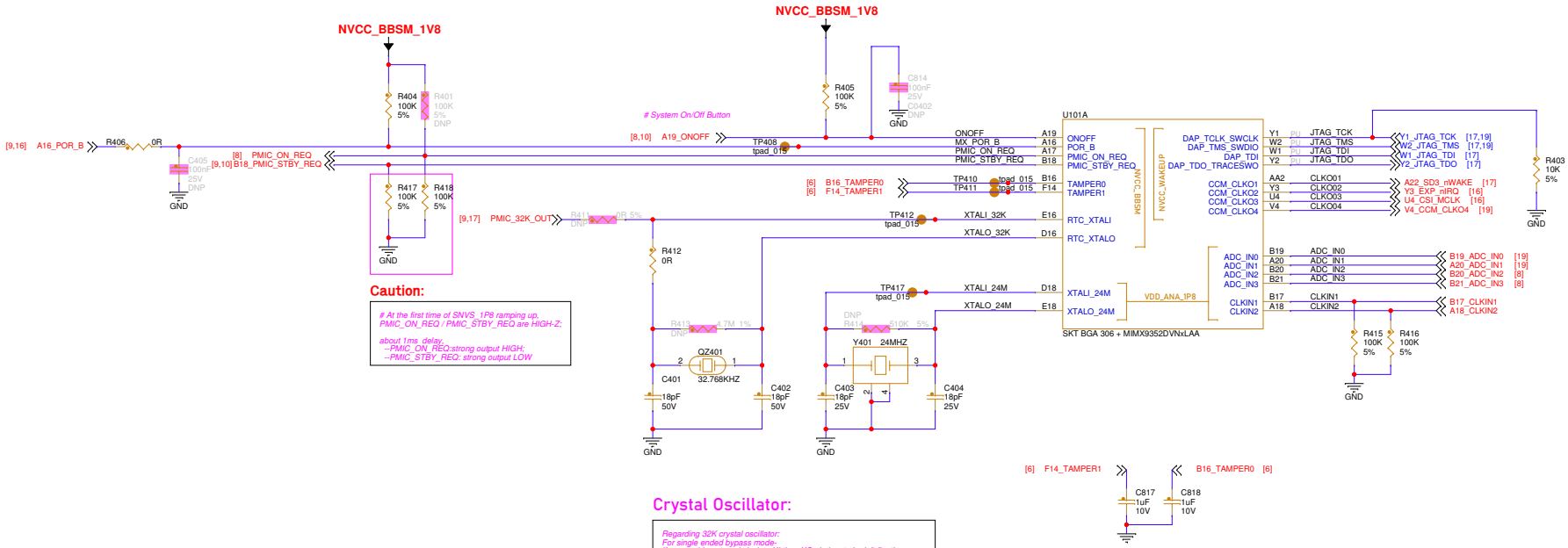
i.MX93 MISC



Caution:

 # At the first time of SNVS_1P8 ramping up,
PMIC_ON_REQ / PMIC_STBY_REQ are HIGH-Z;

about 1ms delay,
--PMIC_ON_REQ:strong output HIGH;
--PMIC_STBY_REQ: strong output LOW

Crystal Oscillator:

Regarding 32K crystal oscillator:
For single ended bypass mode-
If we provide external clock to XI then XO pin has to be left floating (this node will be internally biased by IP). The external clock source should be of the of full voltage swing i.e. (0/avdd) level. Any board capacitance connected XI and XO required by crystal should be de-populated.

Regarding 24MHz crystal oscillator:
Bypass mode need to be selected. In this mode, the crystal oscillator amplifier is off with "cosc_en_lv", "osc_comp_enable_lv" and "pwd_lv" deasserted (logic 0). Only rail to rail input signal at extal (XI) is needed with xtal (XO) could be either floating or ground.

Bypass mode configuration is provide in both FXOSC and SXOSC block guides.

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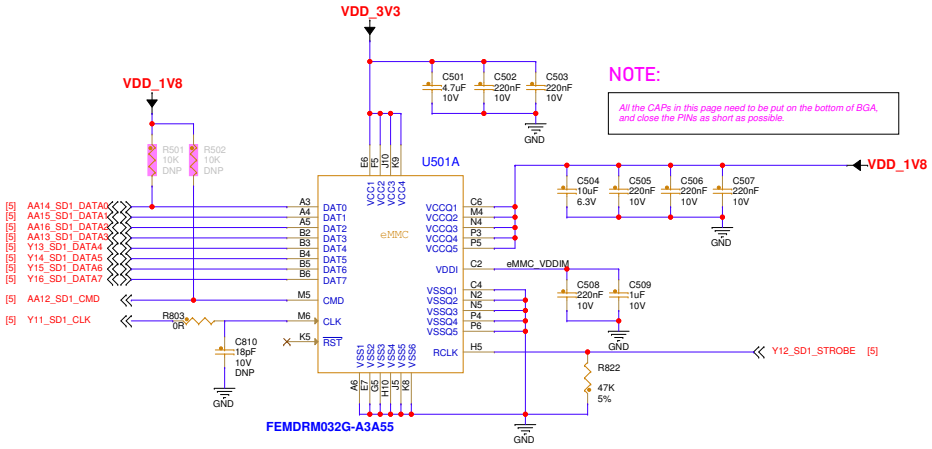
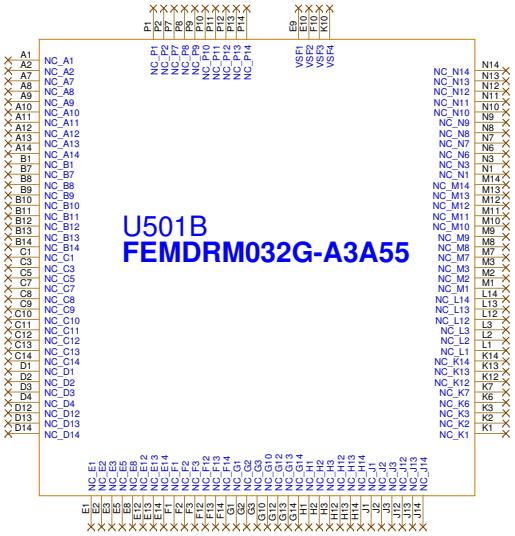
FLASH: eMMC <5.1>





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Classification: <FCP> A <PUBI>

Designer: FORLINX	Drawing Title: FRDM-IMX93		
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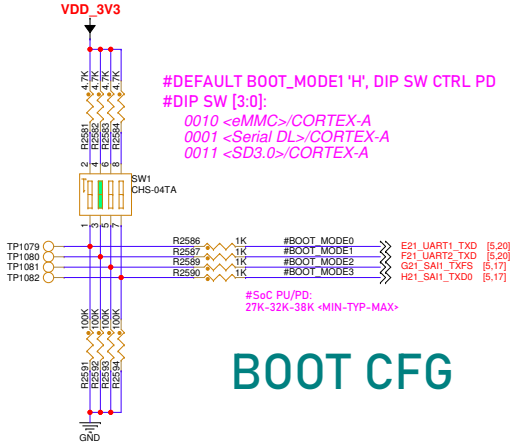
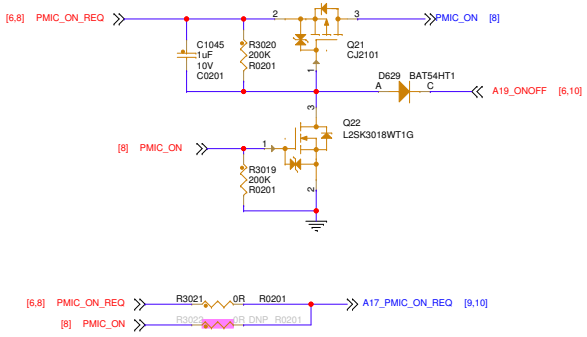
Boot Mode and CFG Switch

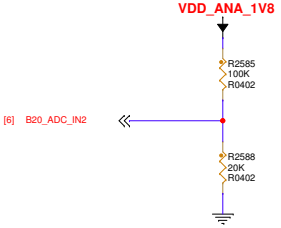
i.MX93 BOOT MODE

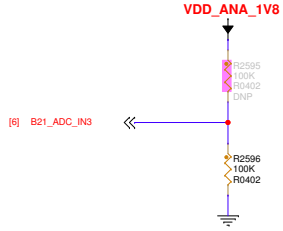
BOOT_MODE[3:0]	BOOT CORE	BOOT DEVICE	COMMENT
0000	Cortex-A55	From internal fuses	
0001	Cortex-A55	Serial Downloader	USB1/2
0010	Cortex-A55	USDHC1 8-bit eMMC 5.1	
0011	Cortex-A55	USDHC2 4-bit SD3.0	
0100	Cortex-A55	FlexSPI Serial NOR	with SFDP (JESD-216) discoverable parameters
0101	Cortex-A55	FlexSPI Serial NAND 2K page	
0110	Cortex-A55	Infinite Loop	
0111	Cortex-A55	Test Mode	
1000	Cortex-M33	From internal fuses	
1001	Cortex-M33	Serial Downloader	USB1
1010	Cortex-M33	USDHC1 8-bit eMMC 5.1	
1011	Cortex-M33	USDHC2 4-bit SD3.0	
1100	Cortex-M33	FlexSPI Serial NOR	with SFDP (JESD-216) discoverable parameters
1101	Cortex-M33	FlexSPI Serial NAND 2K page	
1110	Cortex-M33	Infinite Loop	
1111	Cortex-M33	Test Mode	



BOOT CFG







For example, when Vn.x=0.3V, Vx.n=0.3V, and then board id is V2.1

Board ID Vn.x

Item	Rup	Rdown	ADC	VOL	VERSION
LEVEL1	DNP	100K	0	0V	VAx
LEVEL2	100K	20K	682	0.3V	VBx
LEVEL3	100K	51K	1365	0.6V	VCx
LEVEL4	100K	100K	2047	0.9V	VDx
LEVEL5	100K	200K	2730	1.2V	VEx
LEVEL6	100K	499K	3412	1.5V	VFx
LEVEL7	100K	DNP	4095	1.8V	VGx

Board ID Vx.n

Item	Rup	Rdown	ADC	VOL	VERSION
LEVEL1	DNP	100K	0	0V	Vx
LEVEL2	100K	20K	682	0.3V	Vx1
LEVEL3	100K	51K	1365	0.6V	Vx2
LEVEL4	100K	100K	2047	0.9V	Vx3
LEVEL5	100K	200K	2730	1.2V	Vx4
LEVEL6	100K	499K	3412	1.5V	Vx5
LEVEL7	100K	DNP	4095	1.8V	Vx6

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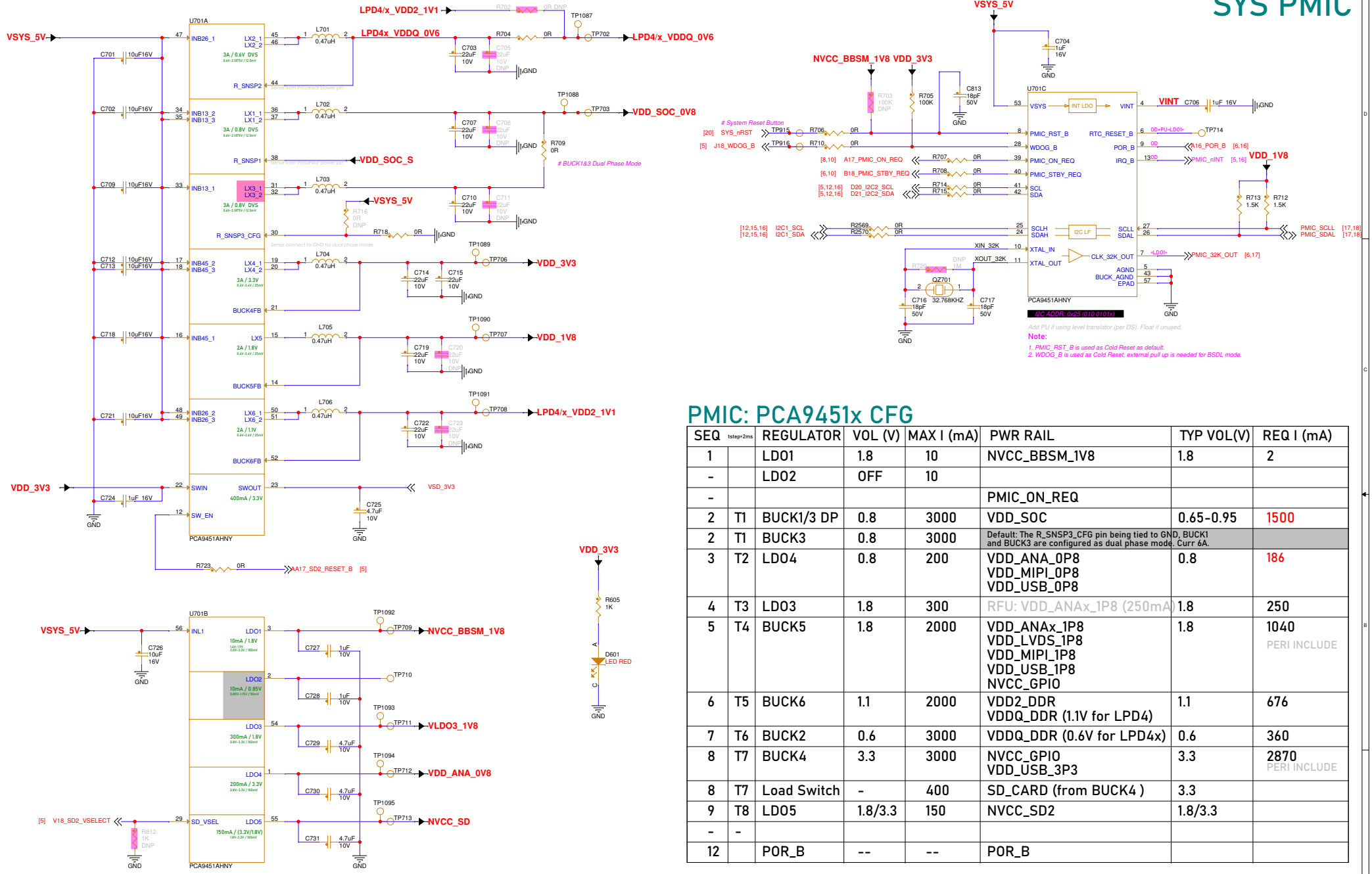
SYS PMIC



PMIC: PCA9451x CFG

SEQ	tstep=2ms	REGULATOR	VOL (V)	MAX I (mA)	PWR RAIL	TYP VOL(V)	REQ I (mA)
1		LDO1	1.8	10	NVCC_BBSM_1V8	1.8	2
-		LDO2	OFF	10			
-					PMIC_ON_REQ		
2	T1	BUCK1/3 DP	0.8	3000	VDD_SOC	0.65-0.95	1500
2	T1	BUCK3	0.8	3000	Default: The R_SNSP3_CFG pin being tied to GND, BUCK1 and BUCK3 are configured as dual phase mode. Curr 6A.		
3	T2	LDO4	0.8	200	VDD_ANA_0P8 VDD_MIPI_0P8 VDD_USB_0P8	0.8	186
4	T3	LDO3	1.8	300	RFU: VDD_ANAx_1P8 (250mA)	1.8	250
5	T4	BUCK5	1.8	2000	VDD_ANAx_1P8 VDD_LVDS_1P8 VDD_MIPI_1P8 VDD_USB_1P8 NVCC_GPIO	1.8	1040 PERI INCLUDE
6	T5	BUCK6	1.1	2000	VDD2_DDR VDDQ_DDR (1.1V for LPD4)	1.1	676
7	T6	BUCK2	0.6	3000	VDDQ_DDR (0.6V for LPD4x)	0.6	360
8	T7	BUCK4	3.3	3000	NVCC_GPIO VDD_USB_3P3	3.3	2870 PERI INCLUDE
8	T7	Load Switch	-	400	SD_CARD (from BUCK4)	3.3	
9	T8	LDO5	1.8/3.3	150	NVCC_SD2	1.8/3.3	
-	-						
12		POR_B	--	--	POR_B		

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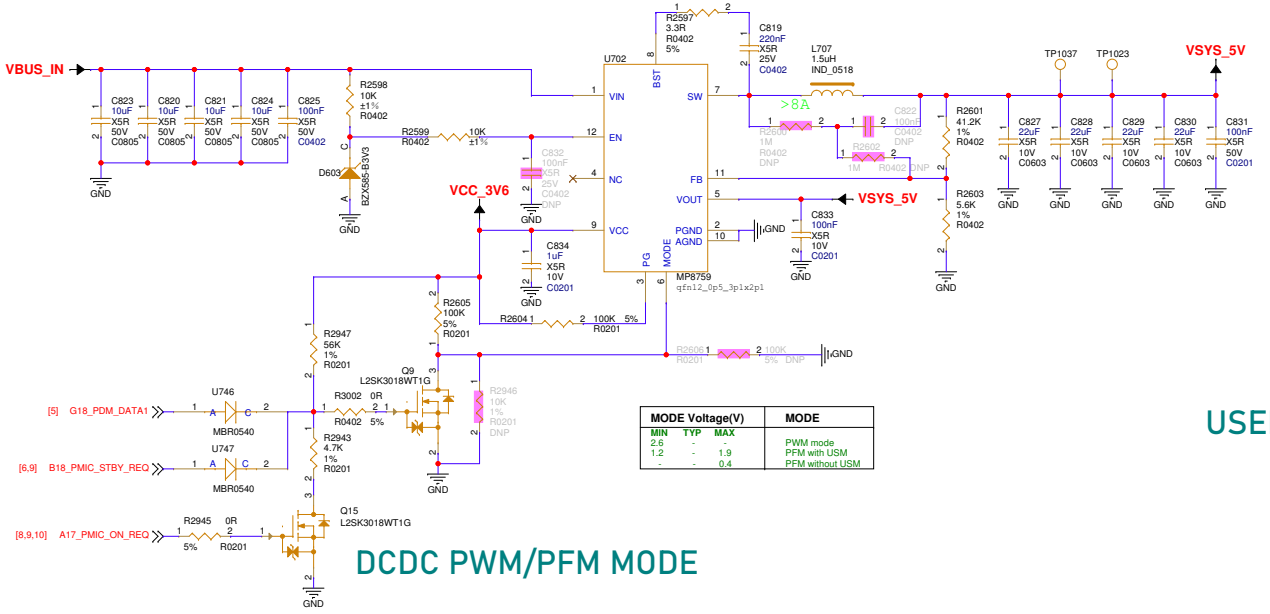
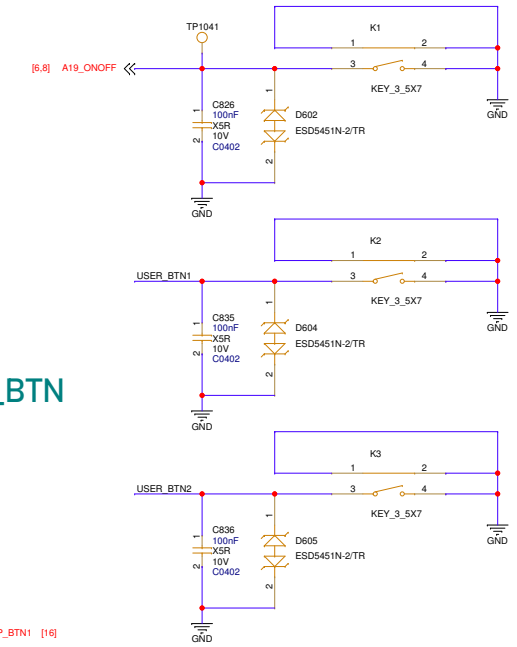
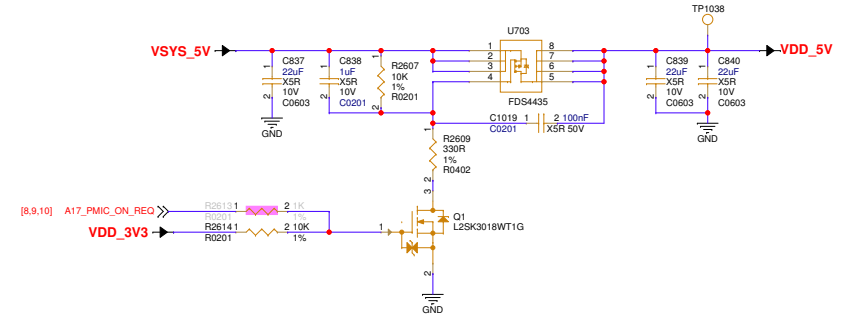
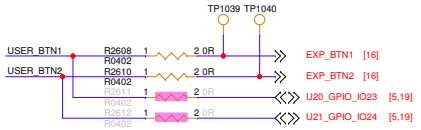


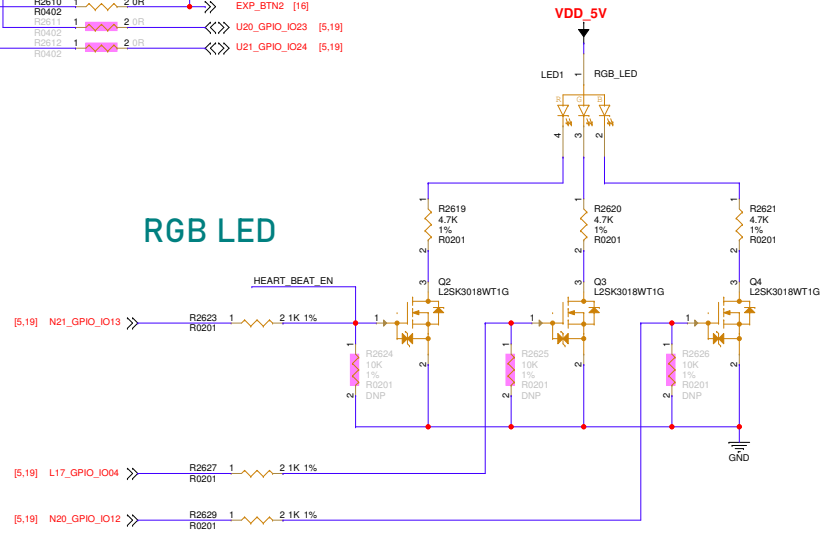
DCDC PWM/PFM MODE



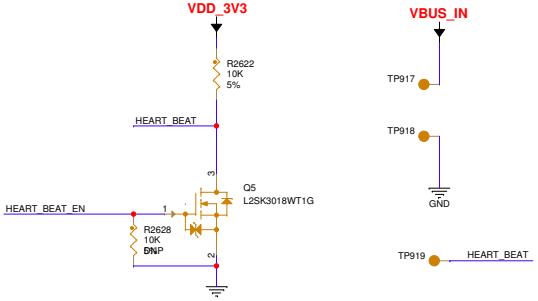
USER_BTN







RGB LED



RESERVE

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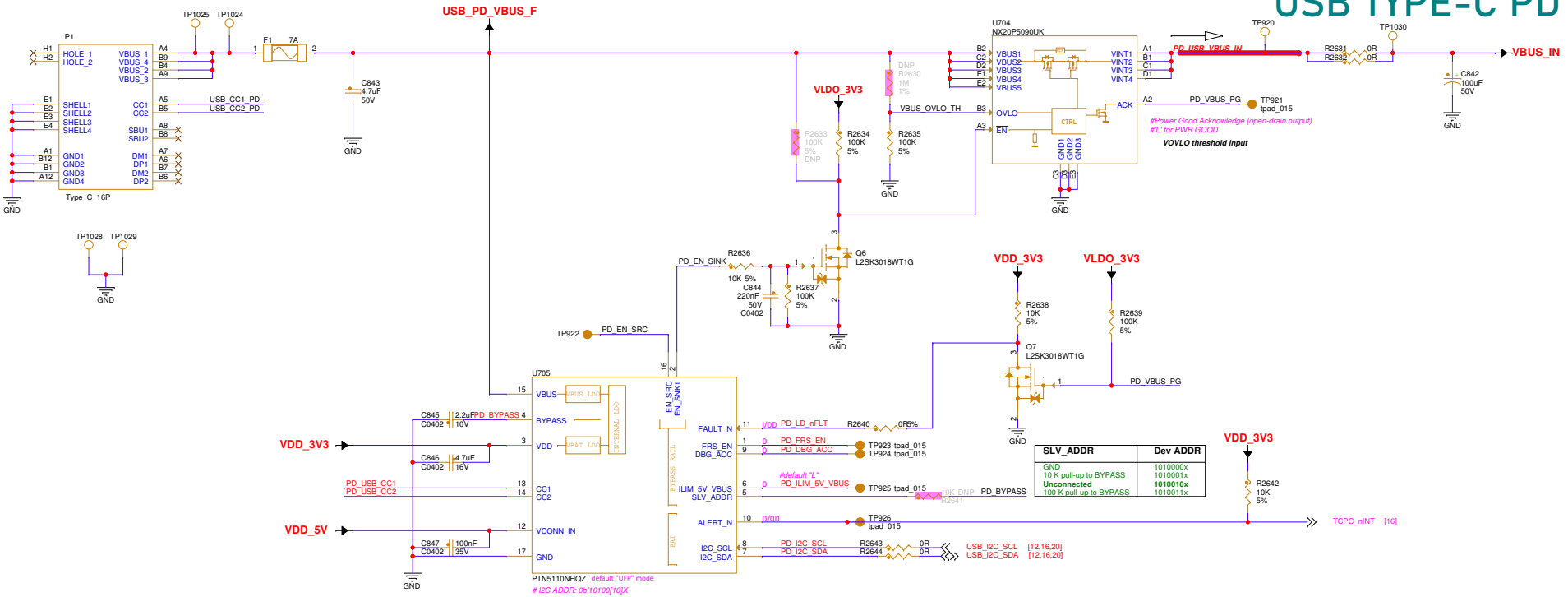
USB TYPE-C PD



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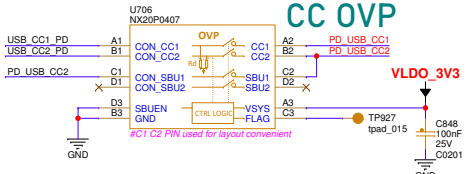
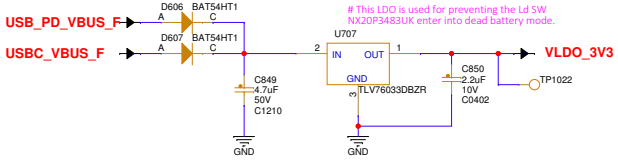
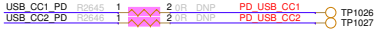


Always ON LDO





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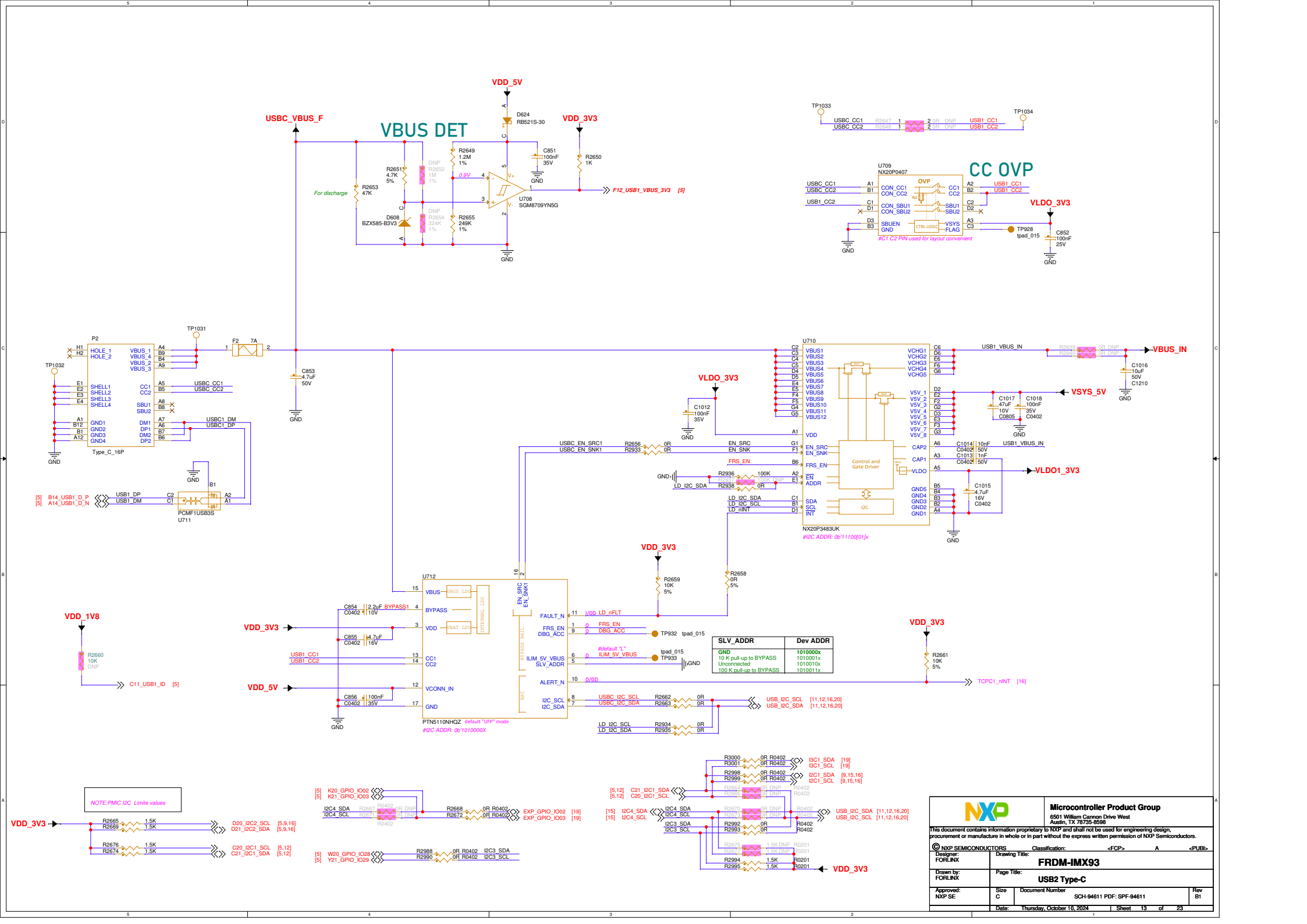
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VDD_3V3
VLDO_3V3
VLDO1_3V3
VSYS_5V
VBUS_IN
VDD_1V8
D624
RB521S-30
R2649
1.2M
1%
C851
100nF
35V
R2650
1K
R2651
4.7K
5%
R2653
47K
For discharge
D608
BZX585-B3V3
R2655
249K
1%
U708
SGM8709YN5G
F12_USB1_VBUS_3V3 [5]
TP1033
TP1034
USBC_CC1
USBC_CC2
USB1_CC1
USB1_CC2
U709
NX20P0407
OVP
CTRL LOGIC
#C1 C2 PIN used for layout convenient
TP928
tpad_015
C852
100nF
25V
P2
Type_C_16P
TP1031
TP1032
F2
7A
C853
4.7uF
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A14_USB1_D_N [5]
PCMF1USB3S
U711
U710
NX20P3483UK
#I2C ADDR: 0b'1110[01]x
C1012
100nF
35V
USBC_EN_SRC1
USBC_EN_SNK1
R2656
R2933
EN_SRC
EN_SNK
FRS_EN
R2936
100K
LD_I2C_SDA
R2938
LD_I2C_SCL
LD_nINT
Control and Gate Driver
I2C
C1014
C1013
C1017
47uF
10V
C0805
C1018
100nF
35V
C0402
C1016
10uF
50V
C1210
C1015
4.7uF
16V
R2939
R2940
USB1_VBUS_IN
U712
PTN5110NHQZ
default "UFP" mode
#I2C ADDR: 0b'1010000X
C854
2.2uF
BYPASS1
C855
4.7uF
16V
C856
100nF
35V
USB1_CC1
USB1_CC2
VBUS
BYPASS
VDD
CC1
CC2
VCONN_IN
GND
FAULT_N
FRS_EN
DBG_ACC
ILIM_5V_VBUS
SLV_ADDR
ALERT_N
I2C_SCL
I2C_SDA
R2659
10K
5%
R2658
0R
5%
TP932
TP933
R2660
10K
DNP
C11_USB1_ID [5]
R2661
10K
5%
TCPC1_nINT [16]
SLV_ADDR
Dev ADDR
GND
1010000x
10 K pull-up to BYPASS
1010001x
Unconnected
1010010x
100 K pull-up to BYPASS
1010011x
USB_I2C_SCL [11,12,16,20]
USB_I2C_SDA [11,12,16,20]
R2662
R2663
R2934
R2935
NOTE:PMIC I2C Limite values
R2665
R2669
R2676
R2674
1.5K
D20_I2C2_SCL [5,9,16]
D21_I2C2_SDA [5,9,16]
C20_I2C1_SCL [5,12]
C21_I2C1_SDA [5,12]
K20_GPIO_IO02 [5]
K21_GPIO_IO03 [5]
W20_GPIO_IO28 [5]
Y21_GPIO_IO29 [5]
I2C4_SDA
I2C4_SCL
I2C3_SDA
R2667
R2671
R2668
R2672
R2988
R2990
EXP_GPIO_IO02 [19]
EXP_GPIO_IO03 [19]
R3000
R3001
R2998
R2999
I3C1_SDA [19]
I3C1_SCL [19]
I2C1_SDA [9,15,16]
I2C1_SCL [9,15,16]
C21_I2C1_SDA [5,12]
C20_I2C1_SCL [5,12]
R2664
R2666
R2670
R2673
R2992
R2993
R2675
R2677
R2994
R2995
USB_I2C_SDA [11,12,16,20]
USB_I2C_SCL [11,12,16,20]
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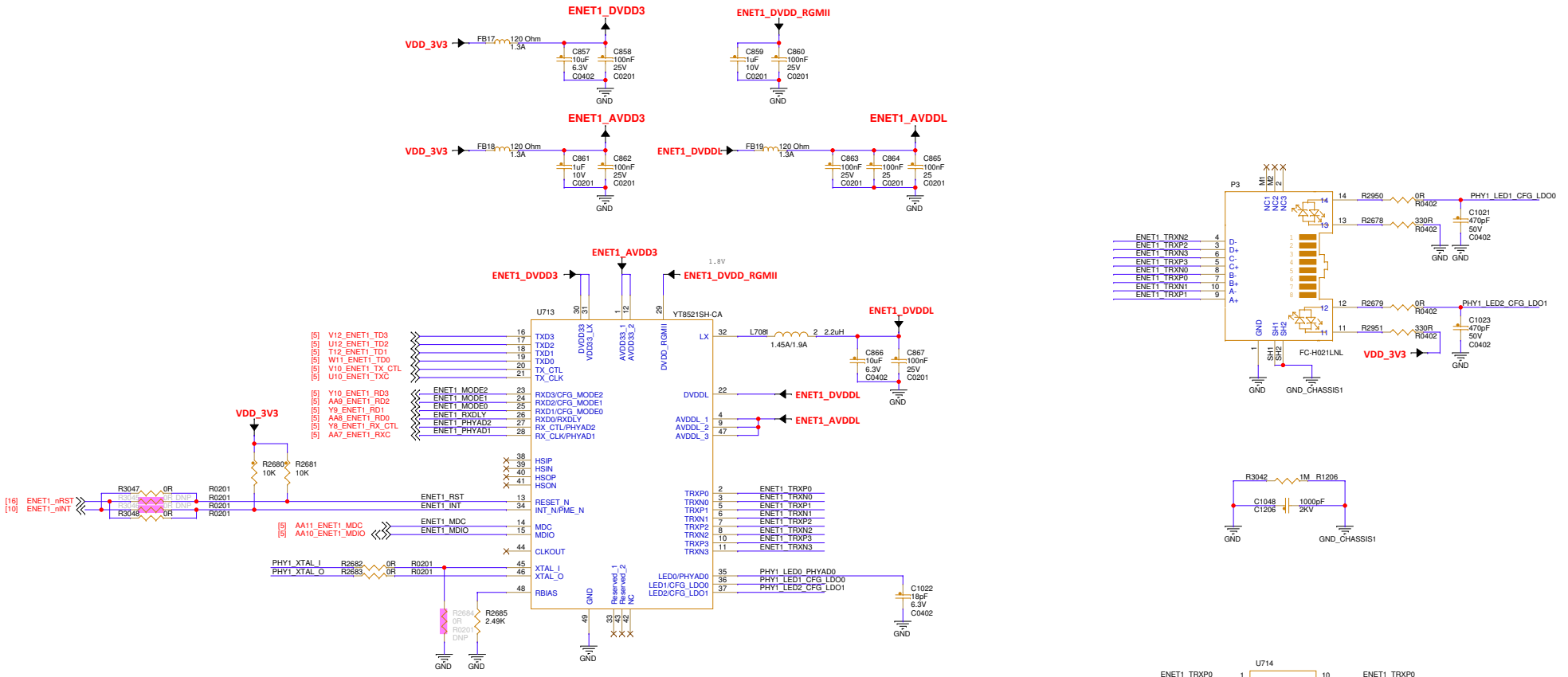
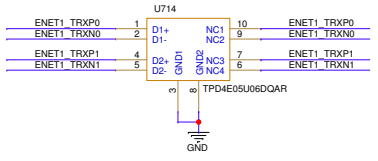
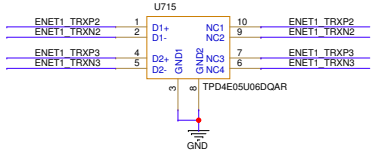
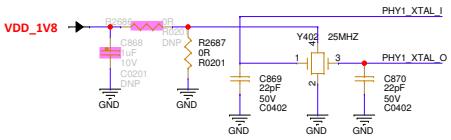
Classification: <FCP> A <PUBI>
Designer: FORLINX
Drawing Title: FRDM-IMX93
Drawn by: FORLINX
Page Title: USB2 Type-C
Approved: NXP SE
Size C
Document Number SCH-94611 PDF: SPF-94611
Rev B1
Date: Thursday, October 10, 2024
Sheet 13 of 23

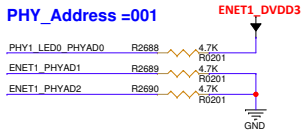


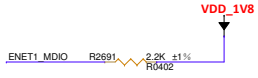






PHY_Address =001

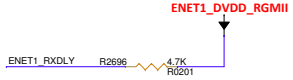




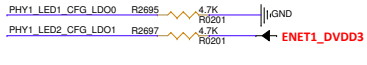
Mode "000" = 000 UTP<-> RGMII

Add 2ns delay to RX_CLK

	RXDLY
YT8521SH-CA	Pull up to add 2ns delay to RXC for RXD latching.
RTL8211FSI-CG	Pull up to add 2ns delay to RXC for RXD latching.



RGMII IO 1.8V



	CFG_LDO[1:0]			
YT8521SH-CA	2'b00: 3.3V	2'b01: 2.5V	2'b10: 1.8V	*2b'11: 1.8V*
RTL8211FSI-CG	2'b00: 3.3V	2'b01: 2.5V	2'b10: 1.8V	*2b'11: 1.5V*

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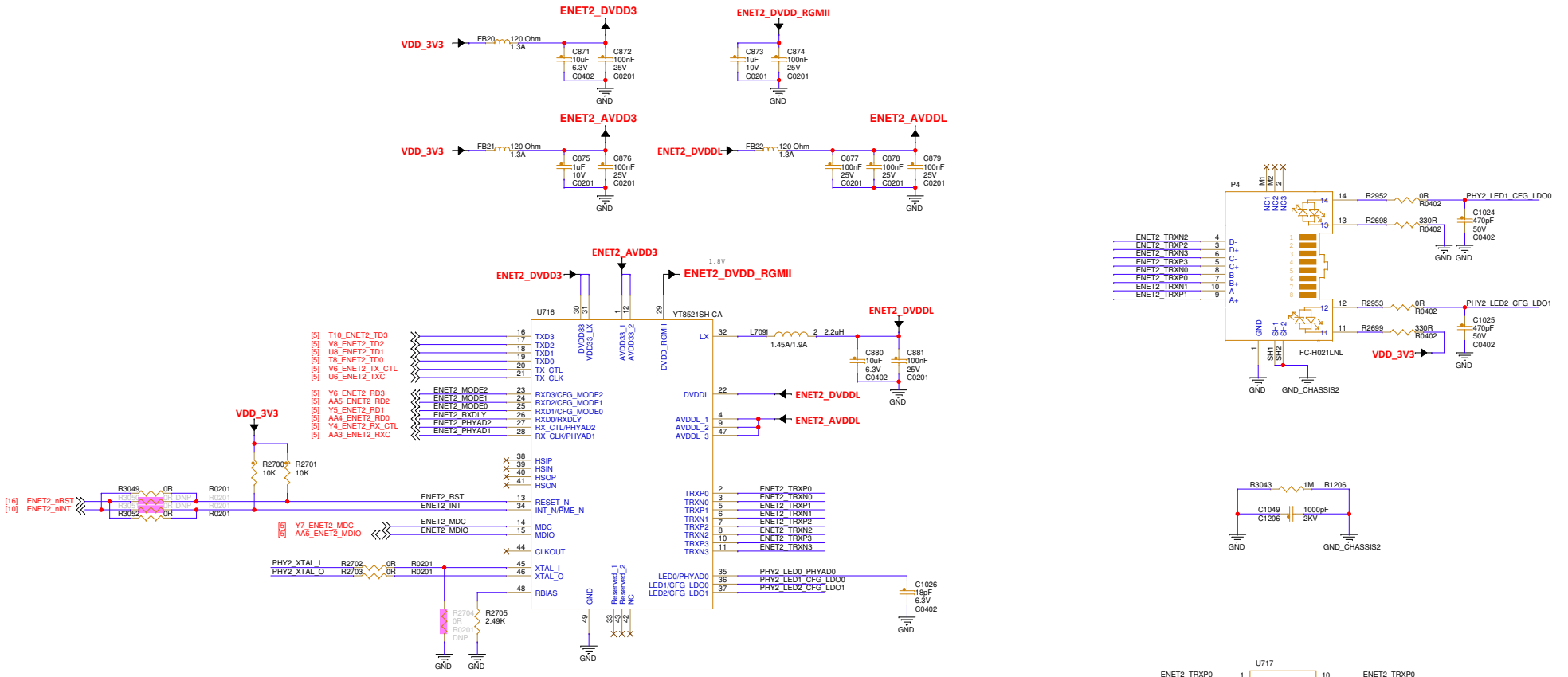
Approved: NXP SE	Size C	Document Number SCH-94611 PDF: SPF-94611	Rev B1
	Date: Thursday, October 10, 2024	Sheet 14 of 23	



	RXDLY
YT8521SH-CA	Pull up to add 2ns delay to RXC for RXD latching.
RTL8211FSI-CG	Pull up to add 2ns delay to RXC for RXD latching.

	CFG_LDO[1:0]			
YT8521SH-CA	2'b00: 3.3V	2'b01: 2.5V	2'b10: 1.8V	*2'b'11: 1.8V*
RTL8211FSI-CG	2'b00: 3.3V	2'b01: 2.5V	2'b10: 1.8V	*2'b'11: 1.5V*

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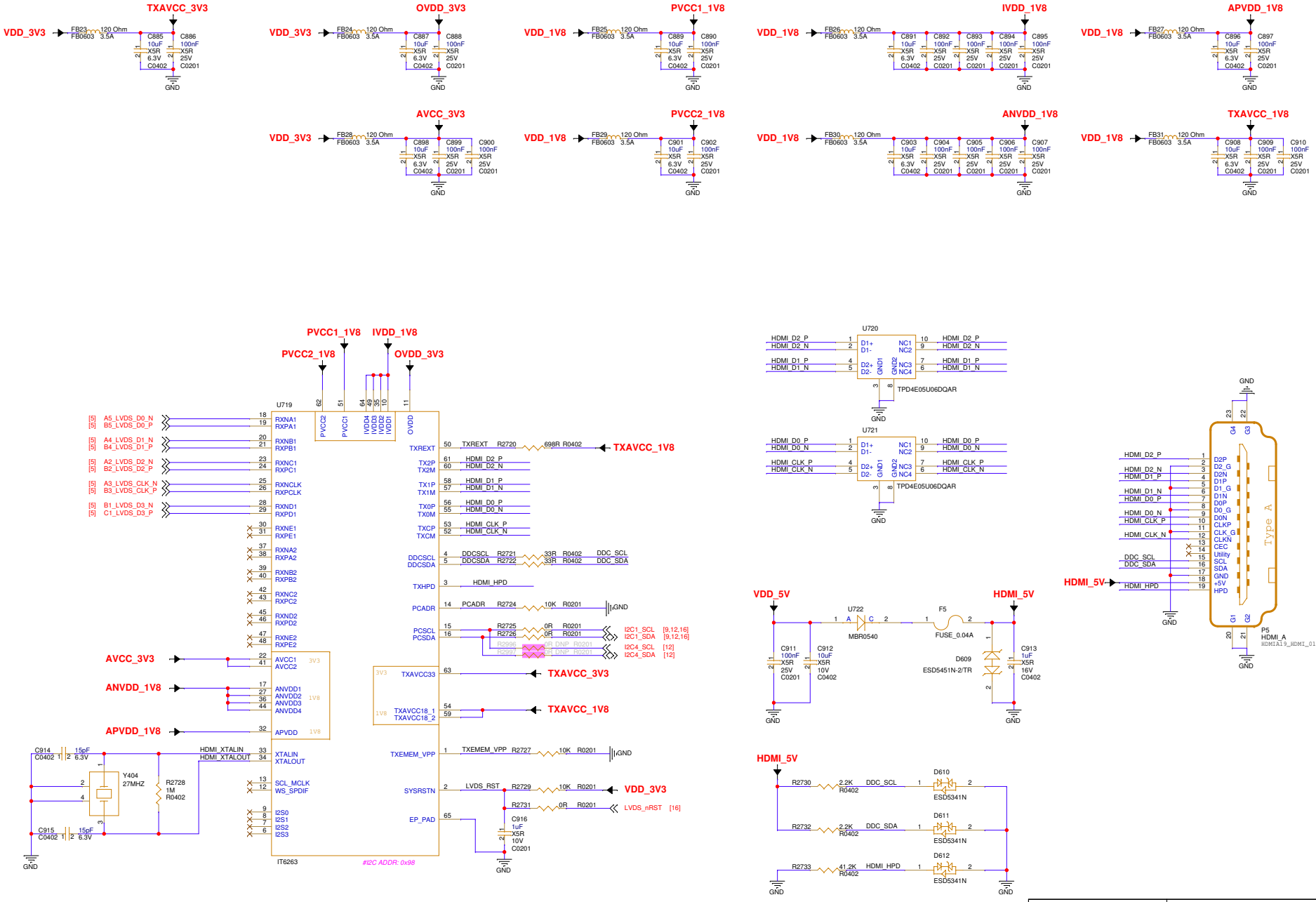
Approved: NXP SE	Size C	Document Number SCH-94611 PDF: SPF-94611	Rev B1
	Date: Thursday, October 10, 2024	Sheet 15 of 23	



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Approved: NXP SE	Size C	Document Number SCH-94611 PDF: SPF-94611	Rev B1
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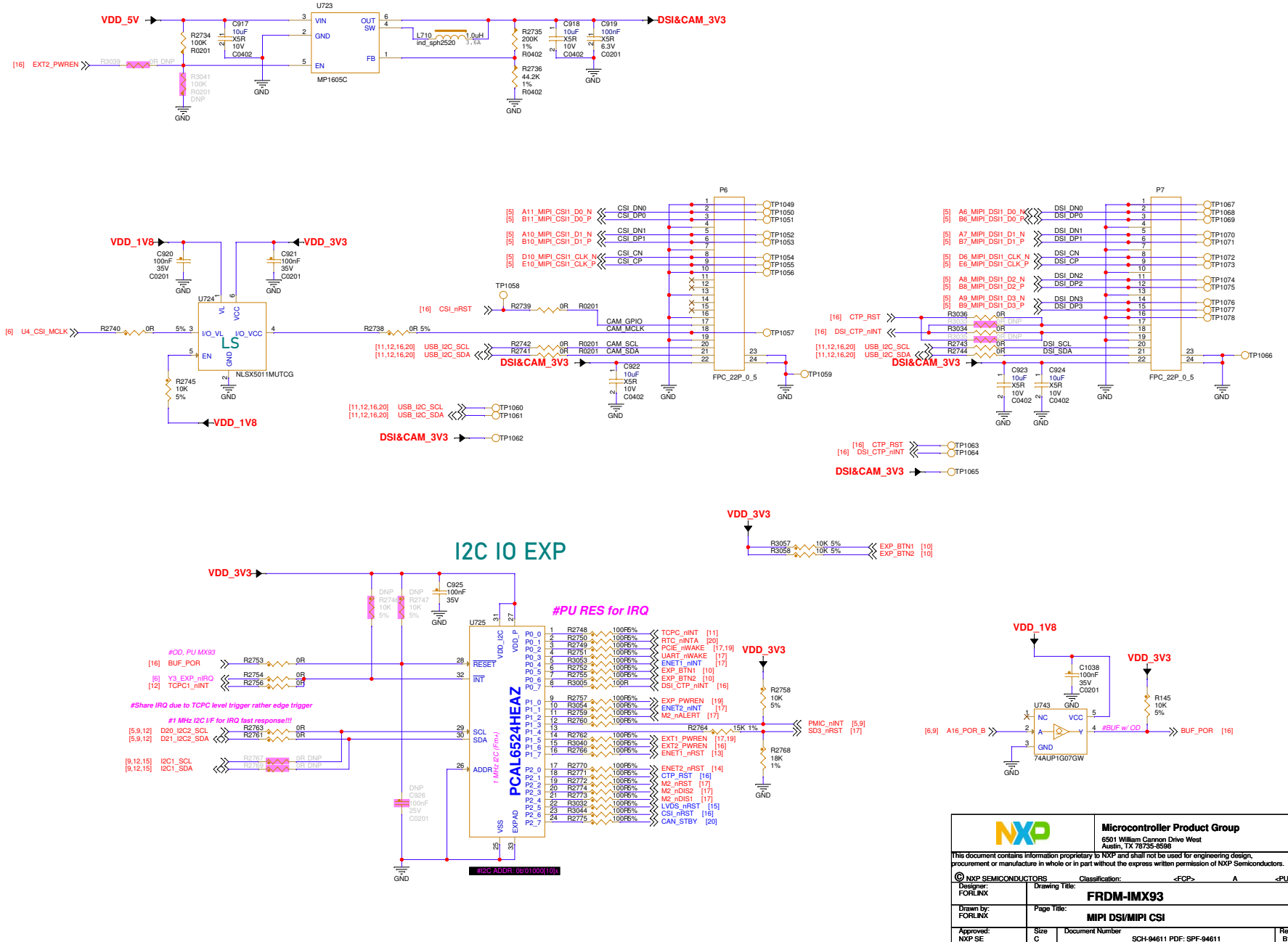

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Drawn by: FORLINX	Page Title: MIPI DSI/MIPI CSI		
Approved: NXP SE	Size C	Document Number SCH-94611 PDF: SPF-94611	Rev B1
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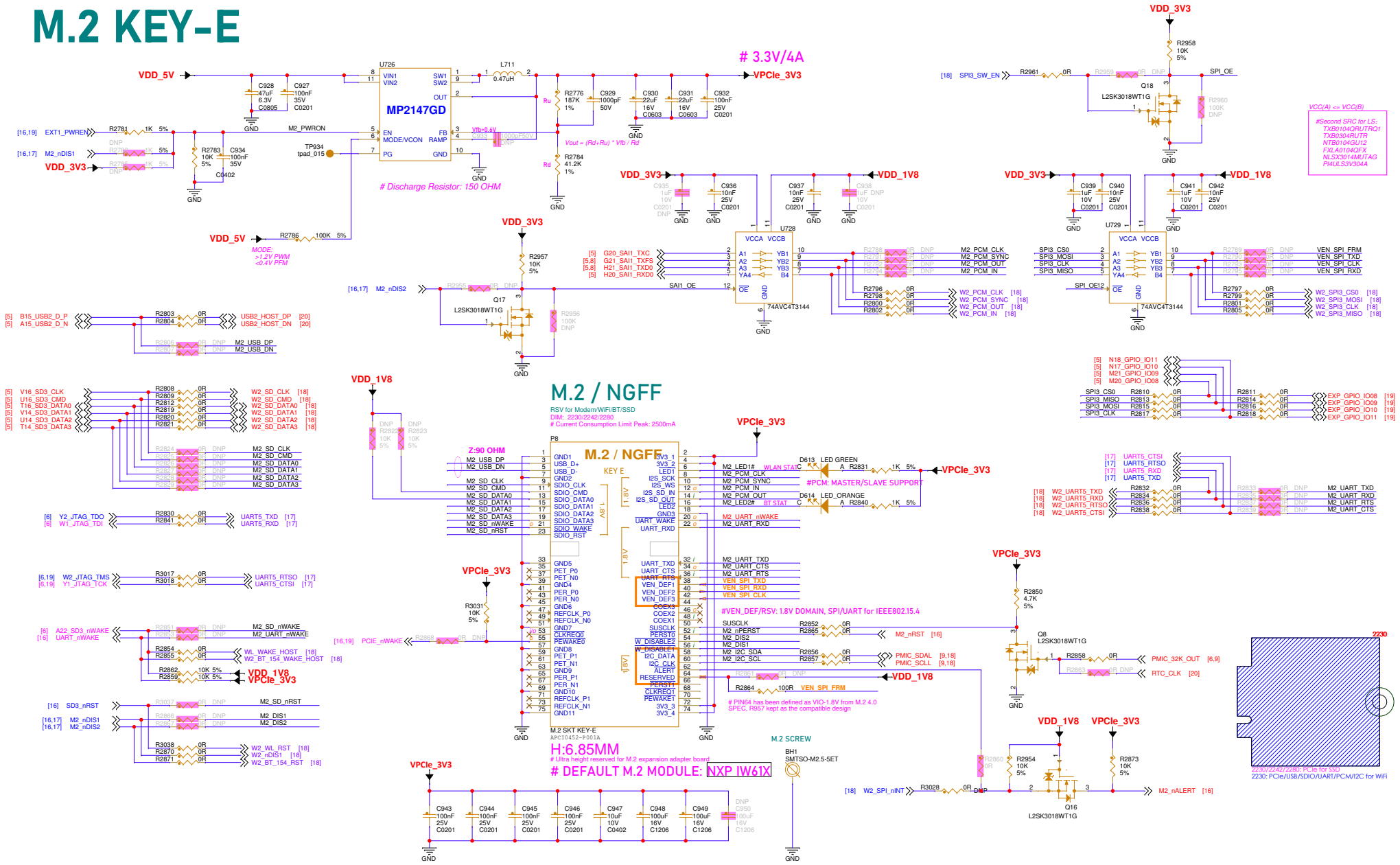
M.2 KEY-E



Key ID	Pin	Interface	Key Definition
A	8-15	2x PCIe x1 / USB 2.0 / I2C / DP x4	Display Port Based Connectivity
B	12-19	PCIe x2 / SATA / USB 2.0 / USB 3.1 Gen1 / HSIC / SSIC / Audio / UIM / I2C / SMBus	WWAN/SSD/Others Primary Key
C	16-23	PCIe/M-PCIe / USB 2.0 / USB 3.1 Gen1 / SSIC / I2C-SlimBUS / UIM / ANTCTL	WWAN Key
D	20-27	Reserved for Future Use (RFU)	RFU
E	24-31	2x PCIe x1 / USB 2.0 / I2C / SDIO / UART / PCM	SDIO Based Connectivity
F	28-35	Future Memory Interface (FMI)	Future Memory Interface
G	39-46	Not Used for M.2; for Custom/Non-Standard Apps	Generic (Not used for M.2)
H	43-50	Reserved for Future Use (RFU)	RFU
J	47-54	Reserved for Future Use (RFU)	RFU
K	51-58	Reserved for Future Use (RFU)	RFU
L	55-62	Reserved for Future Use (RFU)	RFU
M	59-66	PCIe x4 / SATA / SMBus	SSD 4 Lane PCIe

i.MX93 GPIO8-11

#GPIO_IO08	#SPI3_CS	#UART7_TXD
#GPIO_IO09	#SPI3_MISO	#UART7_RXD
#GPIO_IO10	#SPI3_MOSI	#UART7_CTS <I>
#GPIO_IO11	#SPI3_CLK	#UART7_RTS <O>

IW61X GPIO12-15

#GPIO_IO15	#SPI_TXD	#UART2_SOUT
#GPIO_IO14	#SPI_RXD	#UART2_SIN
#GPIO_IO13	#SPI_FRM	#UART2_RTS <O>
#GPIO_IO12	#SPI_CLK	#UART2_CTS <I>

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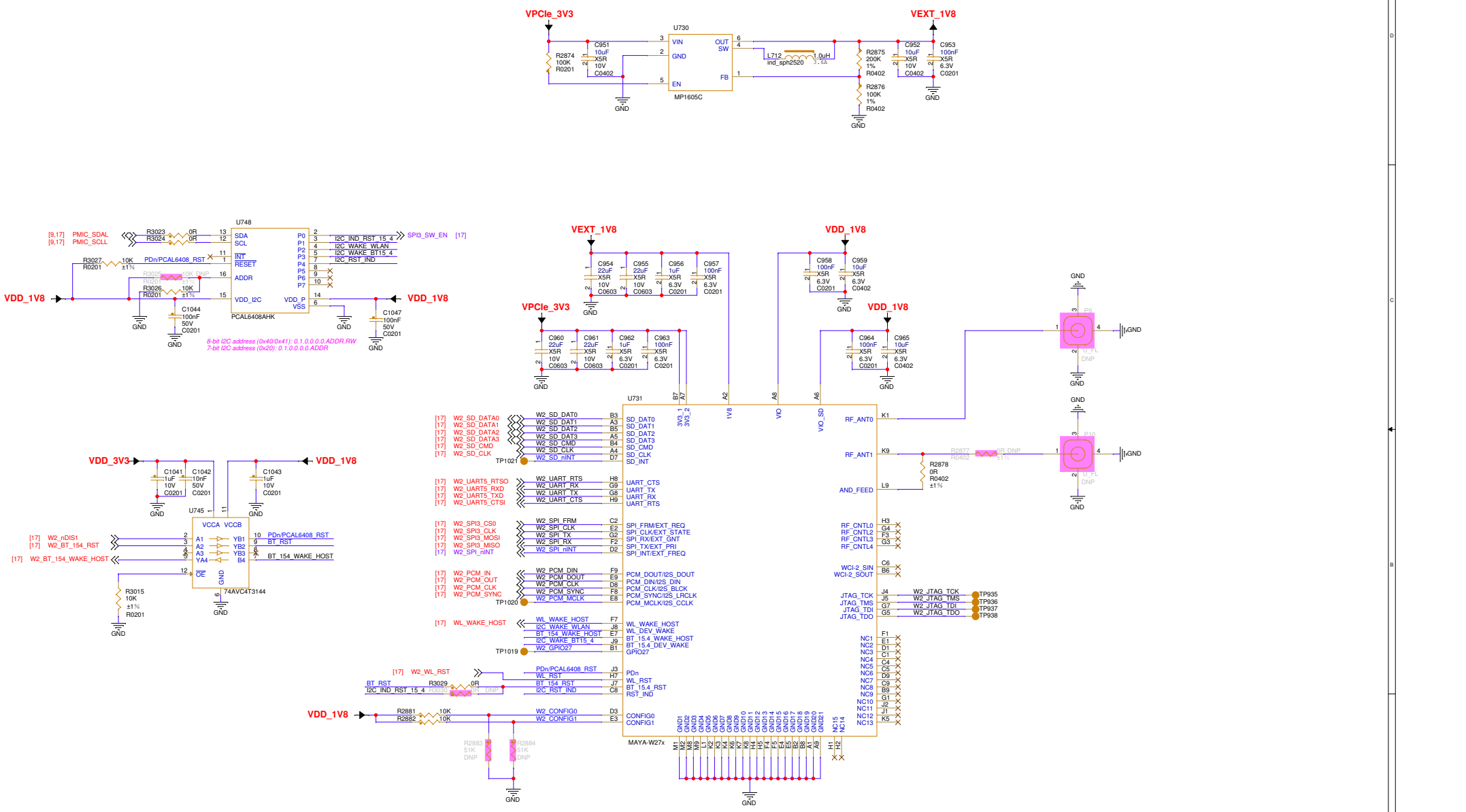
Approved: NXP SE	Size C	Document Number SCH-94611 PDF: SPF-94611	Rev B1
	Date: Thursday, October 10, 2024	Sheet 18 of 23	



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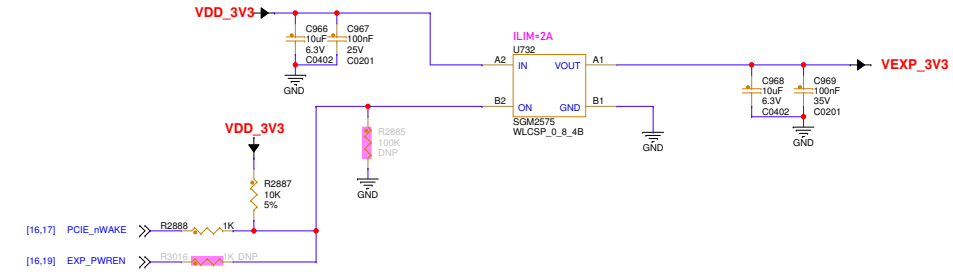
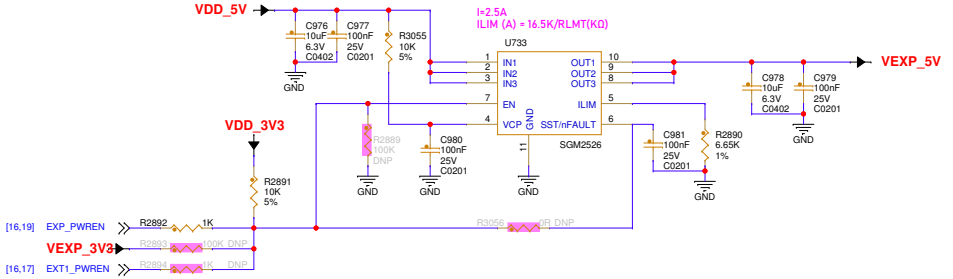
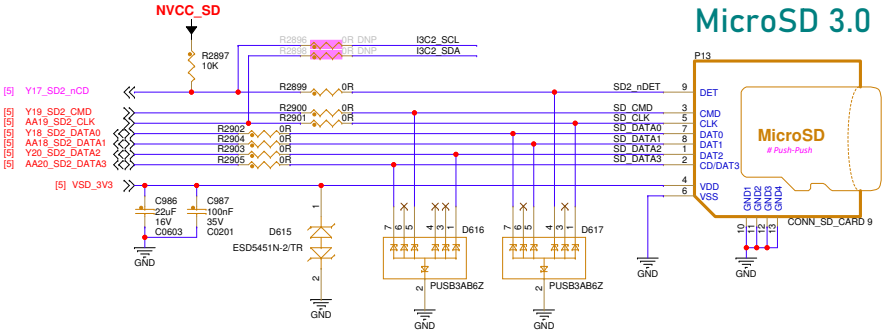
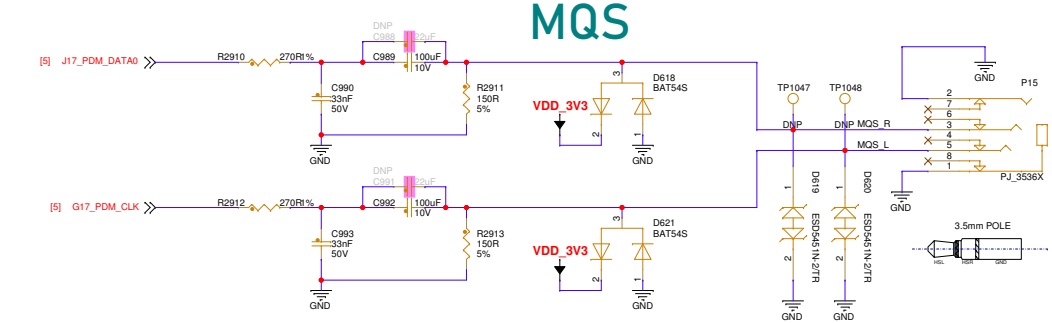
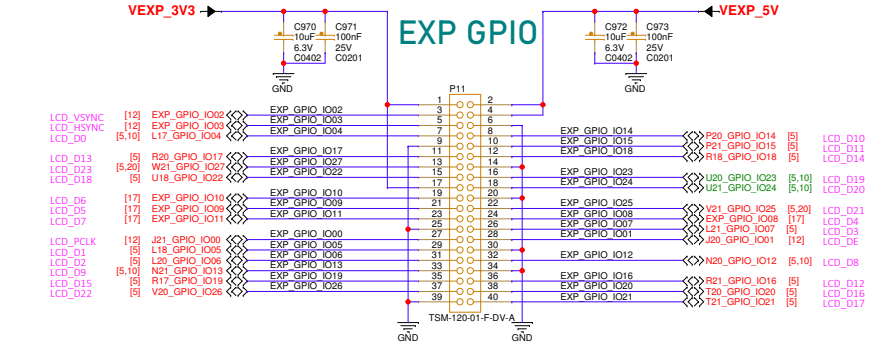
Drawn by: FORLINX	Page Title: WIFI/BT/802.15.4	
Approved: NXP SE	Size C / Document Number SCH-94611 PDF: SPF-94611 / Rev B1	
	Date: Thursday, October 10, 2024 / Sheet 19 of 23	

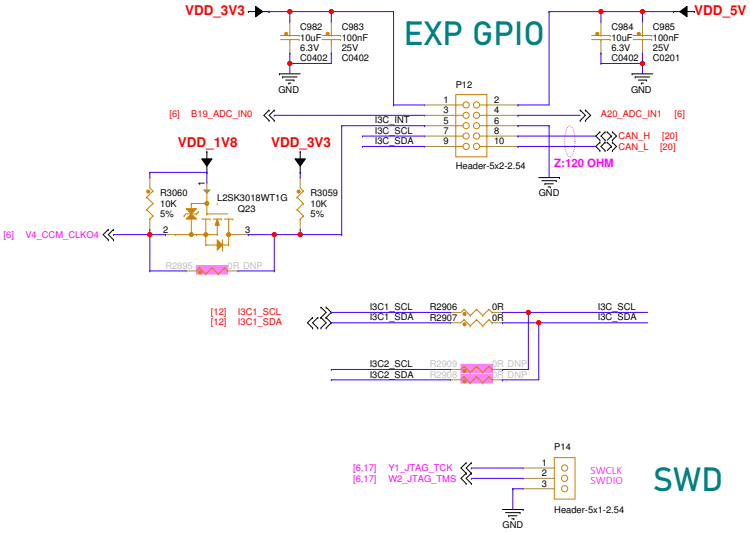


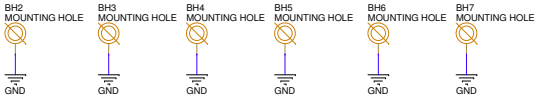












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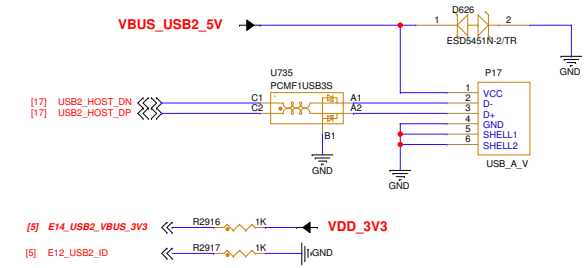
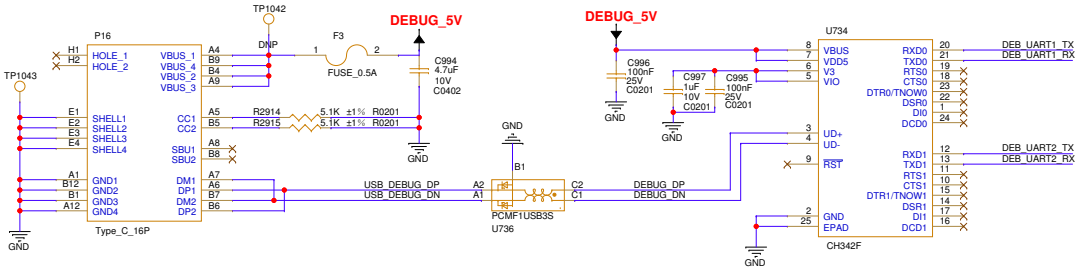
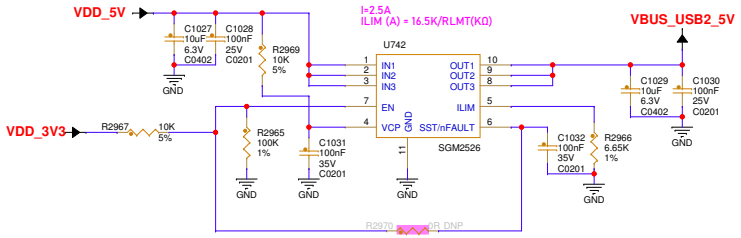
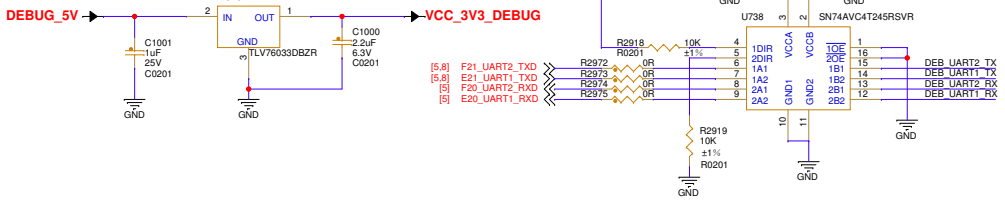
USB2.0

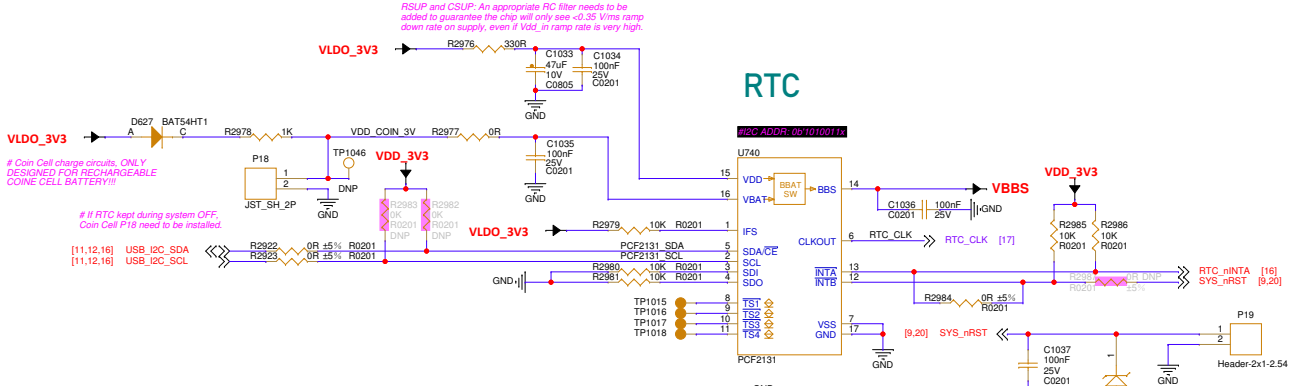


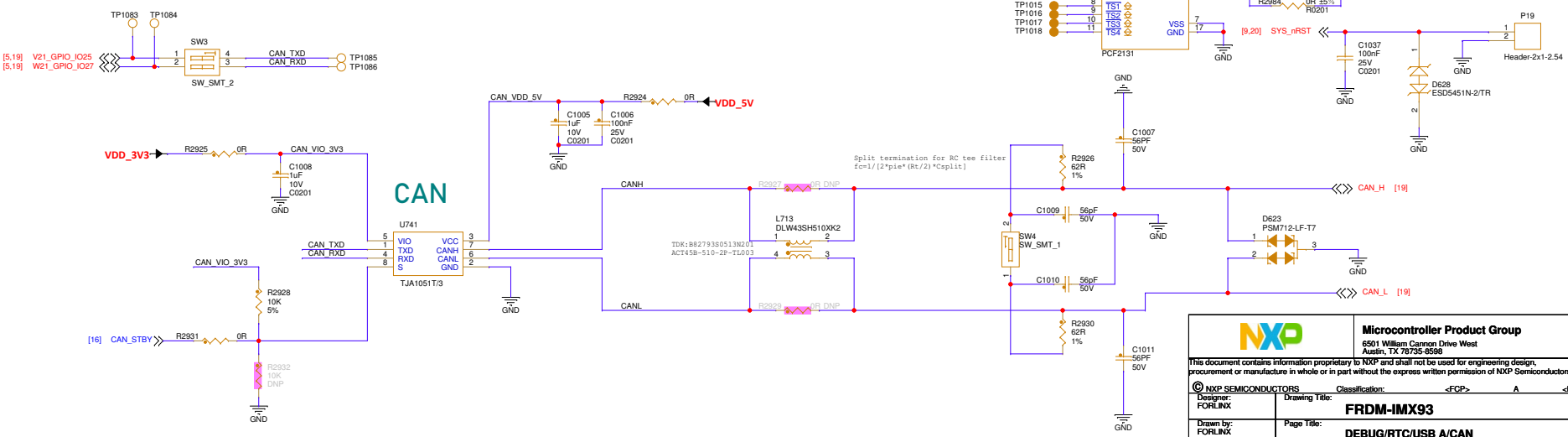
Debug











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Designer: FORLINX	Drawing Title: FRDM-IMX93		
Drawn by: FORLINX	Page Title: DEBUG/RTC/USB A/CAN		
Approved: NXP SE	Size: C	Document Number: SCH-94611 PDF: SPF-94611	Rev: B1
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NOTE:

I2C DEV TABLE

BOARD	PART	DEVICE	I2C ADDR <7bit>	PORT	SPEED	VOL	DESCRIPTION
	U719	IT6263	0x4C (0b'1001100x)	I2C1 /I2C4	1MHz Fm+	3.3V	**LVDS to HDMI**
	P8			I2C1	400KHz	1.8V	M.2 / NGFF KEY-E
	U748	PCAL6408AHK	0x20 (0b'0100000x)	I2C1	1MHz Fm+	1.8V	IO EXP for IRQ/OUTPUT
	U701	PCA9451AHN	0x25 (0b'0100101x)	I2C2	1MHz Fm+	3.3V	PMIC
	U725	PCAL6524HEAZ	0x22 (0b'01000[10]x)	I2C2 /I2C1	1MHz Fm+	3.3V	**IO EXP for IRQ/OUTPUT**
	U10	AT24C256D	0x50 (0b'1010000x)	I2C2	1MHz Fm+	3.3V	**EEPROM**
	U712	PTN5110NHQZ	0x50 (0b'10100[00]x)	I2C3 /I2C1/4	1MHz Fm+	3.3V	USB C PD PHY
	U705	PTN5110NHQZ	0x52 (0b'10100[10]x)	I2C3 /I2C1/4	1MHz Fm+	3.3V	USB C PD PHY
	U710	NX20P3483UK	0x71 (0b'11100[01]x)	I2C3 /I2C1/4	1MHz Fm+	3.3V	USB Load Switch
	U740	PCF2131TF	0x53 (0b'1010011x)	I2C3 /I2C1/4	400KHz	3.3V	Ext RTC
	P6			I2C3 /I2C1/4	400KHz	3.3V	MIPI CSI Camera
	P7			I2C3 /I2C1/4	400KHz	3.3V	CTP/LCD <MIPI DSI>

- M.2 / NGFF KEY-E
  - IO EXP: PCAL6408AEX1Z — 0x20 (0b'0100000x)
- MIPI CSI Camera
  - Camera: AR1335 — 0x36 (0b'0110110x)
  - Camera: AR0144 — 0x10 (0b'0010000x)
  - Ext ISP: AP1302 — 0x3C (0b'0111100x)
  - IO EXP: ADP5585ACPZ-01-R7 — 0x34 (0b'0110100x)
- CTP/LCD <MIPI DSI>
  - Display panel — 0x45 (0b'1000101x)
  - Touch: GT911 — 0x14 (0b'0010100x)

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	Date: Thursday, October 10, 2024	Sheet 22 of 23

i.MX93 IOMUX:

IOPAD	Alt0	Alt1	Alt2	Alt3	Alt4	Alt5	Alt6	Alt7	DEF MUX	PS	PE	IS	IO
RTC_XTALI	bbsmmix.RTC								bbsmmix.RTC				
RTC_XTALO													
PMIC_STBY_REQ	bbsmmix.PMIC_STBY_REQ								ccmsrcgpcmix.PMIC_STBY_REQ				
PMIC_ON_REQ	bbsmmix.PMIC_ON_REQ								bbsmmix.PMIC_ON_REQ				
ONOFF	bbsmmix.ONOFF								bbsmmix.ONOFF				
POR_B	bbsmmix.POR_B								bbsmmix.POR_B				
TAMPER0	bbsmmix.TAMPER0								bbsmmix.TAMPER0				
TAMPER1	bbsmmix.TAMPER1								bbsmmix.TAMPER1				
GPIO_IO00	gpio2.IO[0]	i2c3.SDA	isi.PCLK	lcdif.PCLK	spi6.PCS0	uart5.TX	i2c5.SDA	flexio1.FLEXIO[0]	gpio2.IO[0]				
GPIO_IO01	gpio2.IO[1]	i2c3.SCL	isi.D[0]	lcdif.DE	spi6.SIN	uart5.RX	i2c5.SCL	flexio1.FLEXIO[1]	gpio2.IO[1]				
GPIO_IO02	gpio2.IO[2]	i2c4.SDA	isi.FRAME_VALID	lcdif.VSYNC	spi6.SOUT	uart5.CTS_B	i2c6.SDA	flexio1.FLEXIO[2]	gpio2.IO[2]				
GPIO_IO03	gpio2.IO[3]	i2c4.SCL	isi.LINE_VALID	lcdif.HSYNC	spi6.SCK	uart5.RTS_B	i2c6.SCL	flexio1.FLEXIO[3]	gpio2.IO[3]				
GPIO_IO04	gpio2.IO[4]	tpm3.CH0	pdm.CLK	lcdif.D[0]	spi7.PCS0	uart6.TX	i2c6.SDA	flexio1.FLEXIO[4]	gpio2.IO[4]				
GPIO_IO05	gpio2.IO[5]	tpm4.CH0	pdm.BIT_STREAM[0]	lcdif.D[1]	spi7.SIN	uart6.RX	i2c6.SCL	flexio1.FLEXIO[5]	gpio2.IO[5]				
GPIO_IO06	gpio2.IO[6]	tpm5.CH0	pdm.BIT_STREAM[1]	lcdif.D[2]	spi7.SOUT	uart6.CTS_B	i2c7.SDA	flexio1.FLEXIO[6]	gpio2.IO[6]				
GPIO_IO07	gpio2.IO[7]	spi3.PCS1	isi.D[1]	lcdif.D[3]	spi7.SCK	uart6.RTS_B	i2c7.SCL	flexio1.FLEXIO[7]	gpio2.IO[7]				
GPIO_IO08	gpio2.IO[8]	spi3.PCS0	isi.D[2]	lcdif.D[4]	tpm6.CH0	uart7.TX	i2c7.SDA	flexio1.FLEXIO[8]	gpio2.IO[8]				
GPIO_IO09	gpio2.IO[9]	spi3.SIN	isi.D[3]	lcdif.D[5]	tpm3.EXTCLK	uart7.RX	i2c7.SCL	flexio1.FLEXIO[9]	gpio2.IO[9]				
GPIO_IO10	gpio2.IO[10]	spi3.SOUT	isi.D[4]	lcdif.D[6]	tpm4.EXTCLK	uart7.CTS_B	i2c8.SDA	flexio1.FLEXIO[10]	gpio2.IO[10]				
GPIO_IO11	gpio2.IO[11]	spi3.SCK	isi.D[5]	lcdif.D[7]	tpm5.EXTCLK	uart7.RTS_B	i2c8.SCL	flexio1.FLEXIO[11]	gpio2.IO[11]				
GPIO_IO12	gpio2.IO[12]	tpm3.CH2	pdm.BIT_STREAM[2]	lcdif.D[8]	spi8.PCS0	uart8.TX	i2c8.SDA	sai3.RX_SYNC	gpio2.IO[12]				
GPIO_IO13	gpio2.IO[13]	tpm4.CH2	pdm.BIT_STREAM[3]	lcdif.D[9]	spi8.SIN	uart8.RX	i2c8.SCL	flexio1.FLEXIO[13]	gpio2.IO[13]				
GPIO_IO14	gpio2.IO[14]	uart3.TX	isi.D[6]	lcdif.D[10]	spi8.SOUT	uart8.CTS_B	uart4.TX	flexio1.FLEXIO[14]	gpio2.IO[14]				
GPIO_IO15	gpio2.IO[15]	uart3.RX	isi.D[7]	lcdif.D[11]	spi8.SCK	uart8.RTS_B	uart4.RX	flexio1.FLEXIO[15]	gpio2.IO[15]				
GPIO_IO16	gpio2.IO[16]	sai3.TX_BCLK	pdm.BIT_STREAM[2]	lcdif.D[12]	uart3.CTS_B	spi4.PCS2	uart4.CTS_B	flexio1.FLEXIO[16]	gpio2.IO[16]				
GPIO_IO17	gpio2.IO[17]	sai3.MCLK	isi.D[8]	lcdif.D[13]	uart3.RTS_B	spi4.PCS1	uart4.RTS_B	flexio1.FLEXIO[17]	gpio2.IO[17]				
GPIO_IO18	gpio2.IO[18]	sai3.RX_BCLK	isi.D[9]	lcdif.D[14]	spi5.PCS0	spi4.PCS0	tpm5.CH2	flexio1.FLEXIO[18]	gpio2.IO[18]				
GPIO_IO19	gpio2.IO[19]	sai3.RX_SYNC	pdm.BIT_STREAM[3]	lcdif.D[15]	spi5.SIN	spi4.SIN	tpm6.CH2	sai3.TX_DATA[0]	gpio2.IO[19]				
GPIO_IO20	gpio2.IO[20]	sai3.RX_DATA[0]	pdm.BIT_STREAM[0]	lcdif.D[16]	spi5.SOUT	spi4.SOUT	tpm3.CH1	flexio1.FLEXIO[20]	gpio2.IO[20]				
GPIO_IO21	gpio2.IO[21]	sai3.TX_DATA[0]	pdm.CLK	lcdif.D[17]	spi5.SCK	spi4.SCK	tpm4.CH1	sai3.RX_BCLK	gpio2.IO[21]				
GPIO_IO22	gpio2.IO[22]	usdhc3.CLK	spdif1.IN	lcdif.D[18]	tpm5.CH1	tpm6.EXTCLK	i2c5.SDA	flexio1.FLEXIO[22]	gpio2.IO[22]				
GPIO_IO23	gpio2.IO[23]	usdhc3.CMD	spdif1.OUT	lcdif.D[19]	tpm6.CH1		i2c5.SCL	flexio1.FLEXIO[23]	gpio2.IO[23]				
GPIO_IO24	gpio2.IO[24]	usdhc3.DATA0		lcdif.D[20]	tpm3.CH3	dap.TDO_TRACESWO	spi6.PCS1	flexio1.FLEXIO[24]	gpio2.IO[24]				
GPIO_IO25	gpio2.IO[25]	usdhc3.DATA1	can2.TX	lcdif.D[21]	tpm4.CH3	dap.TCLK_SWCLK	spi7.PCS1	flexio1.FLEXIO[25]	gpio2.IO[25]				
GPIO_IO26	gpio2.IO[26]	usdhc3.DATA2	pdm.BIT_STREAM[1]	lcdif.D[22]	tpm5.CH3	dap.TDI	spi8.PCS1	sai3.TX_SYNC	gpio2.IO[26]				
GPIO_IO27	gpio2.IO[27]	usdhc3.DATA3	can2.RX	lcdif.D[23]	tpm6.CH3	dap.TMS_SWDIO	spi5.PCS1	flexio1.FLEXIO[27]	gpio2.IO[27]				
GPIO_IO28	gpio2.IO[28]	i2c3.SDA						flexio1.FLEXIO[28]	gpio2.IO[28]				
GPIO_IO29	gpio2.IO[29]	i2c3.SCL						flexio1.FLEXIO[29]	gpio2.IO[29]				
CCM_CLKO1	ccmsrcgpcmix.CLKO1				flexio1.FLEXIO[26]	gpio3.IO[26]			ccmsrcgpcmix.CLKO1				
CCM_CLKO2	ccmsrcgpcmix.CLKO2				flexio1.FLEXIO[27]	gpio3.IO[27]			ccmsrcgpcmix.CLKO2				
CCM_CLKO3	ccmsrcgpcmix.CLKO3				flexio2.FLEXIO[28]	gpio4.IO[28]			gpio4.IO[28]				
CCM_CLKO4	ccmsrcgpcmix.CLKO4				flexio2.FLEXIO[29]	gpio4.IO[29]			gpio4.IO[29]				
DAP_TDI	dap.TDI	mqs2.LEFT		can2.TX	flexio2.FLEXIO[30]	gpio3.IO[28]	uart5.RX		dap.TDI				
DAP_TMS_SWDIO	dap.TMS_SWDIO				flexio2.FLEXIO[31]	gpio3.IO[29]	uart5.RTS_B		dap.TMS_SWDIO				
DAP_TCLK_SWCLK	dap.TCLK_SWCLK				flexio1.FLEXIO[30]	gpio3.IO[30]	uart5.CTS_B		dap.TCLK_SWCLK				
DAP_TDO_TRACESWO	dap.TDO_TRACESWO	mqs2.RIGHT		can2.RX	flexio1.FLEXIO[31]	gpio3.IO[31]	uart5.TX		dap.TDO_TRACESWO				
ENET1_MDC	enet_qos.MDC	uart3.DCB_B	i3c2.SCL	usb1.OTG_ID	flexio2.FLEXIO[0]	gpio4.IO[0]			gpio4.IO[0]				
ENET1_MDIO	enet_qos.MDIO	uart3.RIN_B	i3c2.SDA	usb1.OTG_PWR	flexio2.FLEXIO[1]	gpio4.IO[1]			gpio4.IO[1]				
ENET1_TD3	enet_qos.RGMII_TD3		can2.TX	usb2.OTG_ID	flexio2.FLEXIO[2]	gpio4.IO[2]			gpio4.IO[2]				
ENET1_TD2	enet_qos.RGMII_TD2	enet_qos.TX_CLK/.ENET_REF_CLK_ROOT	can2.RX	usb2.OTG_OC	flexio2.FLEXIO[3]	gpio4.IO[3]			gpio4.IO[3]				
ENET1_TD1	enet_qos.RGMII_TD1	uart3.RTS_B	i3c2.PUR	usb1.OTG_OC	flexio2.FLEXIO[4]	gpio4.IO[4]	i3c2.PUR_B		gpio4.IO[4]				
ENET1_TD0	enet_qos.RGMII_TD0	uart3.TX			flexio2.FLEXIO[5]	gpio4.IO[5]			gpio4.IO[5]				
ENET1_TX_CTL	enet_qos.RGMII_TX_CTL	uart3.DTR_B			flexio2.FLEXIO[6]	gpio4.IO[6]			gpio4.IO[6]				
ENET1_TXC	enet_qos.RGMII_TXC	enet_qos.TX_ER			flexio2.FLEXIO[7]	gpio4.IO[7]			gpio4.IO[7]				
ENET1_RX_CTL	enet_qos.RGMII_RX_CTL	uart3.DSR_B		usb2.OTG_PWR	flexio2.FLEXIO[8]	gpio4.IO[8]			gpio4.IO[8]				
ENET1_RXC	enet_qos.RGMII_RXC	enet_qos.RX_ER			flexio2.FLEXIO[9]	gpio4.IO[9]			gpio4.IO[9]				
ENET1_RD0	enet_qos.RGMII_RD0	uart3.RX			flexio2.FLEXIO[10]	gpio4.IO[10]			gpio4.IO[10]				
ENET1_RD1	enet_qos.RGMII_RD1	uart3.CTS_B		lptmr2.ALT1	flexio2.FLEXIO[11]	gpio4.IO[11]			gpio4.IO[11]				
ENET1_RD2	enet_qos.RGMII_RD2			lptmr2.ALT2	flexio2.FLEXIO[12]	gpio4.IO[12]			gpio4.IO[12]				
ENET1_RD3	enet_qos.RGMII_RD3		wakeupmix.flexspi_usdhc_tester_trigger	lptmr2.ALT3	flexio2.FLEXIO[13]	gpio4.IO[13]			gpio4.IO[13]				
ENET2_MDC	enet2.MDC	uart4.DCB_B	sai2.RX_SYNC		flexio2.FLEXIO[14]	gpio4.IO[14]			gpio4.IO[14]				
ENET2_MDIO	enet2.MDIO	uart4.RIN_B	sai2.RX_BCLK		flexio2.FLEXIO[15]	gpio4.IO[15]			gpio4.IO[15]				
ENET2_TD3	enet2.RGMII_TD3		sai2.RX_DATA[0]		flexio2.FLEXIO[16]	gpio4.IO[16]			gpio4.IO[16]				
ENET2_TD2	enet2.RGMII_TD2	enet2.TX_CLK/ENET_REF_CLK_ROOT	sai2.RX_DATA[1]		flexio2.FLEXIO[17]	gpio4.IO[17]			gpio4.IO[17]				
ENET2_TD1	enet2.RGMII_TD1	uart4.RTS_B	sai2.RX_DATA[2]		flexio2.FLEXIO[18]	gpio4.IO[18]			gpio4.IO[18]				
ENET2_TD0	enet2.RGMII_TD0	uart4.TX	sai2.RX_DATA[3]		flexio2.FLEXIO[19]	gpio4.IO[19]			gpio4.IO[19]				
ENET2_TX_CTL	enet2.RGMII_TX_CTL	uart4.DTR_B	sai2.TX_SYNC		flexio2.FLEXIO[20]	gpio4.IO[20]			gpio4.IO[20]				
ENET2_TXC	enet2.RGMII_TXC	enet2.TX_ER	sai2.TX_BCLK		flexio2.FLEXIO[21]	gpio4.IO[21]			gpio4.IO[21]				
ENET2_RX_CTL	enet2.RGMII_RX_CTL	uart4.DSR_B	sai2.TX_DATA[0]		flexio2.FLEXIO[22]	gpio4.IO[22]			gpio4.IO[22]				
ENET2_RXC	enet2.RGMII_RXC	enet2.RX_ER	sai2.TX_DATA[1]		flexio2.FLEXIO[23]	gpio4.IO[23]			gpio4.IO[23]				
ENET2_RD0	enet2.RGMII_RD0	uart4.RX	sai2.TX_DATA[2]		flexio2.FLEXIO[24]	gpio4.IO[24]			gpio4.IO[24]				
ENET2_RD1	enet2.RGMII_RD1	spdif1.IN	sai2.TX_DATA[3]		flexio2.FLEXIO[25]	gpio4.IO[25]			gpio4.IO[25]				
ENET2_RD2	enet2.RGMII_RD2	uart4.CTS_B	sai2.MCLK	mqs2.RIGHT	flexio2.FLEXIO[26]	gpio4.IO[26]			gpio4.IO[26]				
ENET2_RD3	enet2.RGMII_RD3	spdif1.OUT	spdif1.IN	mqs2.LEFT	flexio2.FLEXIO[27]	gpio4.IO[27]			gpio4.IO[27]				
SD1_CLK	usdhc1.CLK				flexio1.FLEXIO[8]	gpio3.IO[8]			gpio3.IO[8]				
SD1_CMD	usdhc1.CMD				flexio1.FLEXIO[9]	gpio3.IO[9]			gpio3.IO[9]				
SD1_DATA0	usdhc1.DATA0				flexio1.FLEXIO[10]	gpio3.IO[10]			gpio3.IO[10]				
SD1_DATA1	usdhc1.DATA1				flexio1.FLEXIO[11]	gpio3.IO[11]	ccmsrcgpcmix.INT_BOOT		gpio3.IO[11]				
SD1_DATA2	usdhc1.DATA2				flexio1.FLEXIO[12]	gpio3.IO[12]	ccmsrcgpcmix.PMIC_READY		gpio3.IO[12]				
SD1_DATA3	usdhc1.DATA3	flexspi.A_SS1_B			flexio1.FLEXIO[13]	gpio3.IO[13]			gpio3.IO[13]				
SD1_DATA4	usdhc1.DATA4	flexspi.A_DATA[4]			flexio1.FLEXIO[14]	gpio3.IO[14]			gpio3.IO[14]				
SD1_DATA5	usdhc1.DATA5	flexspi.A_DATA[5]	usdhc1.RESET_B		flexio1.FLEXIO[15]	gpio3.IO[15]			gpio3.IO[15]				
SD1_DATA6	usdhc1.DATA6	flexspi.A_DATA[6]	usdhc1.CD_B		flexio1.FLEXIO[16]	gpio3.IO[16]			gpio3.IO[16]				
SD1_DATA7	usdhc1.DATA7	flexspi.A_DATA[7]	usdhc1.WP		flexio1.FLEXIO[17]	gpio3.IO[17]			gpio3.IO[17]				
SD1_STROBE	usdhc1.STROBE	flexspi.A_DQS			flexio1.FLEXIO[18]	gpio3.IO[18]			gpio3.IO[18]				
SD2_VSELECT	usdhc2.VSELECT	usdhc2.WP	lptmr2.ALT3		flexio1.FLEXIO[19]	gpio3.IO[19]	ccmsrcgpcmix.EXT_CLK1		gpio3.IO[19]				
SD3_CLK	usdhc3.CLK	flexspi.A_SCLK			flexio1.FLEXIO[20]	gpio3.IO[20]			gpio3.IO[20]				
SD3_CMD	usdhc3.CMD	flexspi.A_SS0_B			flexio1.FLEXIO[21]	gpio3.IO[21]			gpio3.IO[21]				
SD3_DATA0	usdhc3.DATA0	flexspi.A_DATA[0]			flexio1.FLEXIO[22]	gpio3.IO[22]			gpio3.IO[22]				
SD3_DATA1	usdhc3.DATA1	flexspi.A_DATA[1]			flexio1.FLEXIO[23]	gpio3.IO[23]			gpio3.IO[23]				
SD3_DATA2	usdhc3.DATA2	flexspi.A_DATA[2]			flexio1.FLEXIO[24]	gpio3.IO[24]			gpio3.IO[24]				
SD3_DATA3	usdhc3.DATA3	flexspi.A_DATA[3]			flexio1.FLEXIO[25]	gpio3.IO[25]			gpio3.IO[25]				
SD2_CD_B	usdhc2.CD_B	enet_qos.1588_EVENT0_IN	i3c2.SCL		flexio1.FLEXIO[0]	gpio3.IO[0]	ccmsrcgpcmix.TESTER_ACK		gpio3.IO[0]				
SD2_CLK	usdhc2.CLK	enet_qos.1588_EVENT0_OUT	i3c2.SDA		flexio1.FLEXIO[1]	gpio3.IO[1]	ccmsrcgpcmix.OBSERVE0		gpio3.IO[1]				
SD2_CMD	usdhc2.CMD	enet2.1588_EVENT0_IN	i3c2.PUR	i3c2.PUR_B	flexio1.FLEXIO[2]	gpio3.IO[2]	ccmsrcgpcmix.OBSERVE1		gpio3.IO[2]				
SD2_DATA0	usdhc2.DATA0	enet2.1588_EVENT0_OUT	can2.TX		flexio1.FLEXIO[3]	gpio3.IO[3]	ccmsrcgpcmix.OBSERVE2		gpio3.IO[3]				
SD2_DATA1	usdhc2.DATA1	enet2.1588_EVENT1_IN	can2.RX		flexio1.FLEXIO[4]	gpio3.IO[4]	ccmsrcgpcmix.WAIT		gpio3.IO[4]				
SD2_DATA2	usdhc2.DATA2	enet2.1588_EVENT1_OUT	mqs2.RIGHT		flexio1.FLEXIO[5]	gpio3.IO[5]	ccmsrcgpcmix.STOP		gpio3.IO[5]				
SD2_DATA3	usdhc2.DATA3	lptmr2.ALT1	mqs2.LEFT		flexio1.FLEXIO[6]	gpio3.IO[6]	ccmsrcgpcmix.EARLY_RESET		gpio3.IO[6]				
SD2_RESET_B	usdhc2.RESET_B	lptmr2.ALT2			flexio1.FLEXIO[7]	gpio3.IO[7]	ccmsrcgpcmix.SYSTEM_RESET		gpio3.IO[7]				
I2C1_SCL	i2c1.SCL	i3c1.SCL	uart1.DCB_B	tpm2.CH0		gpio1.IO[0]			gpio1.IO[0]				
I2C1_SDA	i2c1.SDA	i3c1.SDA	uart1.RIN_B	tpm2.CH1		gpio1.IO[1]			gpio1.IO[1]				
I2C2_SCL	i2c2.SCL	i3c1.PUR	uart2.DCB_B	tpm2.CH2	sai1.RX_SYNC	gpio1.IO[2]	i3c1.PUR_B		gpio1.IO[2]				
I2C2_SDA	i2c2.SDA		uart2.RIN_B	tpm2.CH3	sai1.RX_BCLK	gpio1.IO[3]			gpio1.IO[3]				
UART1_RXD	uart1.RX	seco.RX	spi2.SIN	tpm1.CH0		gpio1.IO[4]			gpio1.IO[4]				
UART1_TXD	uart1.TX	seco.TX	spi2.PCS0	tpm1.CH1		gpio1.IO[5]/ccmsrcgpcmix.BOOT_MODE[0]			gpio1.IO[5]/ccmsrcgpcmix.BOOT_MODE[0]				
UART2_RXD	uart2.RX	uart1.CTS_B	spi2.SOUT	tpm1.CH2	sai1.MCLK	gpio1.IO[6]			gpio1.IO[6]				
UART2_TXD	uart2.TX	uart1.RTS_B	spi2.SCK	tpm1.CH3		gpio1.IO[7]/ccmsrcgpcmix.BOOT_MODE[1]			gpio1.IO[7]/ccmsrcgpcmix.BOOT_MODE[1]				
PDM_CLK	pdm.CLK	mqs1.LEFT			lptmr1.ALT1	gpio1.IO[8]	can1.TX		gpio1.IO[8]				
PDM_BIT_STREAM0	pdm.BIT_STREAM[0]	mqs1.RIGHT	spi1.PCS1	tpm1.EXTCLK	lptmr1.ALT2	gpio1.IO[9]	can1.RX		gpio1.IO[9]				
PDM_BIT_STREAM1	pdm.BIT_STREAM[1]	m33.NMI	spi2.PCS1	tpm2.EXTCLK	lptmr1.ALT3	gpio1.IO[10]	ccmsrcgpcmix.EXT_CLK1		gpio1.IO[10]				
SAI1_TXFS	sai1.TX_SYNC	sai1.TX_DATA[1]	spi1.PCS0	uart2.DTR_B	mqs1.LEFT	gpio1.IO[11]/ccmsrcgpcmix.BOOT_MODE[2]			gpio1.IO[11]/ccmsrcgpcmix.BOOT_MODE[2]				
SAI1_TXC	sai1.TX_BCLK	uart2.CTS_B	spi1.SIN	uart1.DSR_B	can1.RX	gpio1.IO[12]			gpio1.IO[12]				
SAI1_TXD0	sai1.TX_DATA[0]	uart2.RTS_B	spi1.SCK	uart1.DTR_B	can1.TX	gpio1.IO[13]/ccmsrcgpcmix.BOOT_MODE[3]			gpio1.IO[13]/ccmsrcgpcmix.BOOT_MODE[3]				
SAI1_RXD0	sai1.RX_DATA[0]	sai1.MCLK	spi1.SOUT	uart2.DSR_B	mqs1.RIGHT	gpio1.IO[14]			gpio1.IO[14]				
WDOG_ANY	wdog1.WDOG_ANY					gpio1.IO[15]			gpio1.IO[15]				
CLKIN1	anamix.CLKIN1	anamix.esd_diode											
CLKIN2	anamix.CLKIN2	anamix.atx											
XTALI_24M	anamix.xtali_24M												
XTALO_24M	anamix.xtalo_24M												
ADC_IN0	anamix.adc_in0												
ADC_IN1	anamix.adc_in1												
ADC_IN2	anamix.adc_in2												
ADC_IN3	anamix.adc_in3												

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