		Standard Mode		Fast Mode	
Parameter	Description	Min	Max	Min	Max
Vih	high level input voltage	See DS	See DS	See DS	See DS
Vil	low level input voltage	See DS	See DS	See DS	See DS
Fscl	scl clock freq	0.0	100.0	0.0	400.0
Thd;sta	hold time @ start cond.	4.0	-	0.9	-
Tlow	Low period of the SCL clk	4.7	-	1.3	-
Thigh	High period of the SCL clk	4.0	-	0.6	-
Tsu;sta	setup time @ start cond.	4.7	-	0.9	-
Thd;dat	data hold time	See spec	See spec	See spec	See spec
Tsu;dat	data setup time	250.0	-	See spec	-
Tr;sda	sda rising time	-	1000.0	See spec	300.0
Tf;sda	sda falling time	-	300.0	See spec	300.0
Tr;scl	scl rising time	-	1000.0	See spec	300.0
Tf;scl	scl falling time	-	300.0	See spec	300.0
Tsu;sto	setup time @ stop cond.	4.0	-	0.9	-
Tbuf	bus free time bw start & stop	4.7	-	1.3	-
Tvd;dat	data valid time	No spec	No spec	No spec	No spec
Tvd;ack	data acknowledge time	No spec	No spec	No spec	No spec

Units
V
V
kHz
us
us
us
us
ns
ns
ns
ns
ns
us
us