Some high pulse is confirmed on high-order bit like this when SDIN, BCKI, LRCKI was low. This looks like the some DC level was output from SDOUT though SDIN is Low.

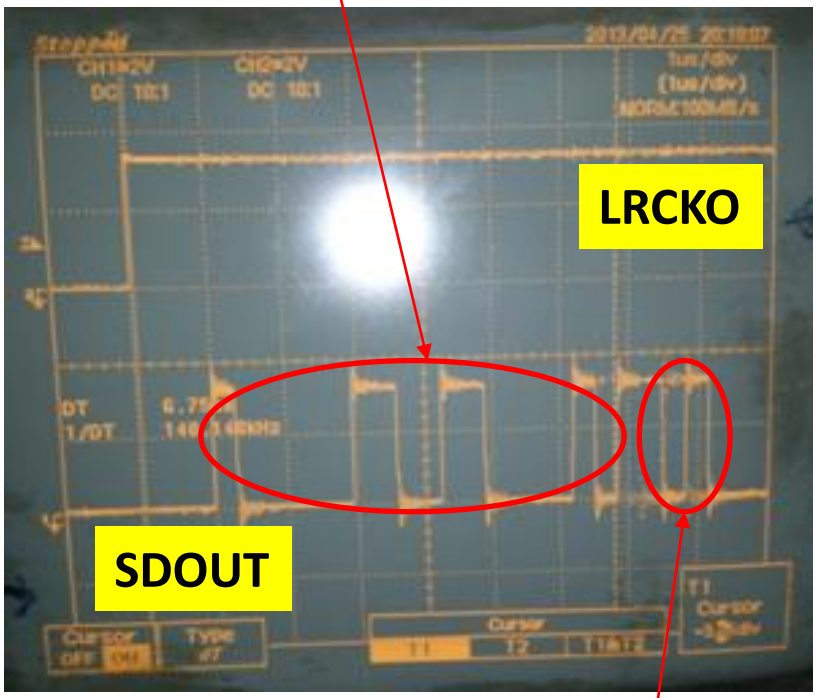
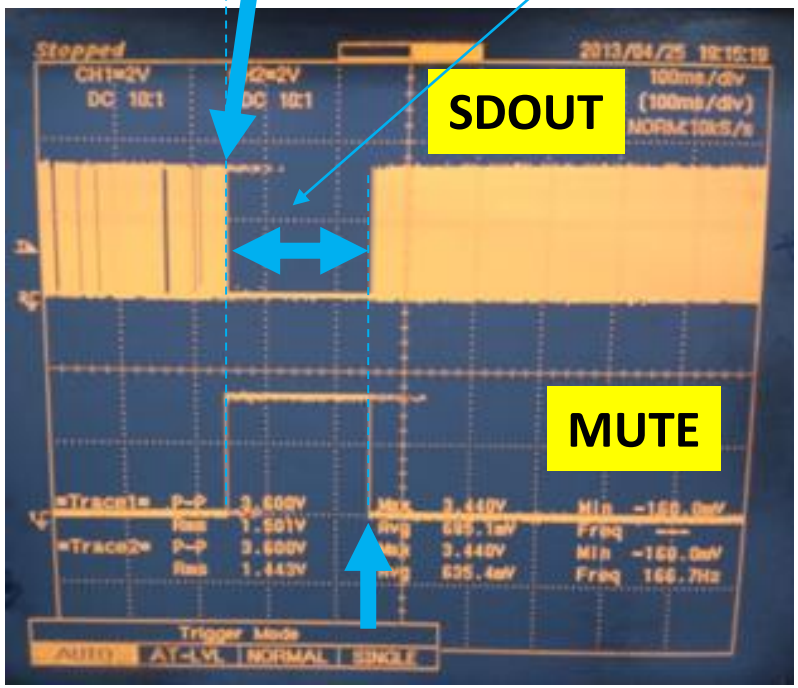


Fig.1

LRCKI,BCLI was input, and MUTE was High by /RDY output

SDOUT was remained Low during MUTE was High



SDIN was input

Fig.2

They confirmed that the pulse on low-order bit was dither because it was removed when bypass mode was enabled.

Fig.1

- No SDIN, BCKI, LRCKI
- Some high pulse is confirmed on high-order bit when SDIN, BCKI, LRCKI is low.
- MUTE was Low

Fig.2

- MUTE was gone High when LRCKI,BCLI was input, and after that MUTE was gone Low when SDIN was input.
- SDOUT was stayed Low during MUTE was Low

Updated information in Red

Additional information

1. There is no dither signal and pulse on high-order bit when LRCKI and BCLI was input and no SDIN after a reset at start-up.
2. When SDIN, LRCKI and BCLI were input and after that these input was gone to Low (No input and CLK condition), dither signal and pulse on high-order bit were confirmed.
3. After the #2 above, pulse on high-order bit was removed when LRCKI and BCLI were input. This is cause of pop noise in their system, so they need to know how to not output this pulse on high-order bit.

Question

1. Can you clarify how many bits are applied for dither signal? (e.g., Is it applied by low order 3 or 4 bits)
2. Is following operation normal operation? (Asking about #1 and 2 above)
   - There is no dither signal and pulse on high-order bit when LRCKI and BCLI was input and no SDIN after a reset at start-up.
   - When SDIN, LRCKI and BCLI were input and after that these input was gone to Low (No input and CLK condition), dither signal and pulse on high-order bit were confirmed.
3. Is following operation normal operation? (Asking about #3 above)
   - The pulse on high-order bit was removed when LRCKI and BCLI were input.

1. Can you give us advice to remove the pulse on high-order bit? They need to remove it because this is caused of pop noise in their system when pulse on high-order bit is stopped after LRCKI and BCLI were input. Should they need to set MUTE pin to High at no LRCKI and BCLI condition?