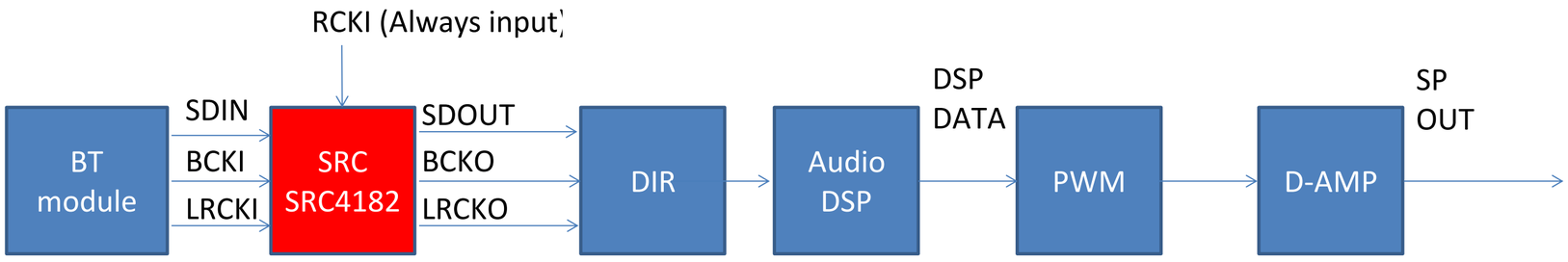
Simplified signal flow



Good case (No data on high-order bit of SDOUT at no LRCKI, BCKI and SDIN input)

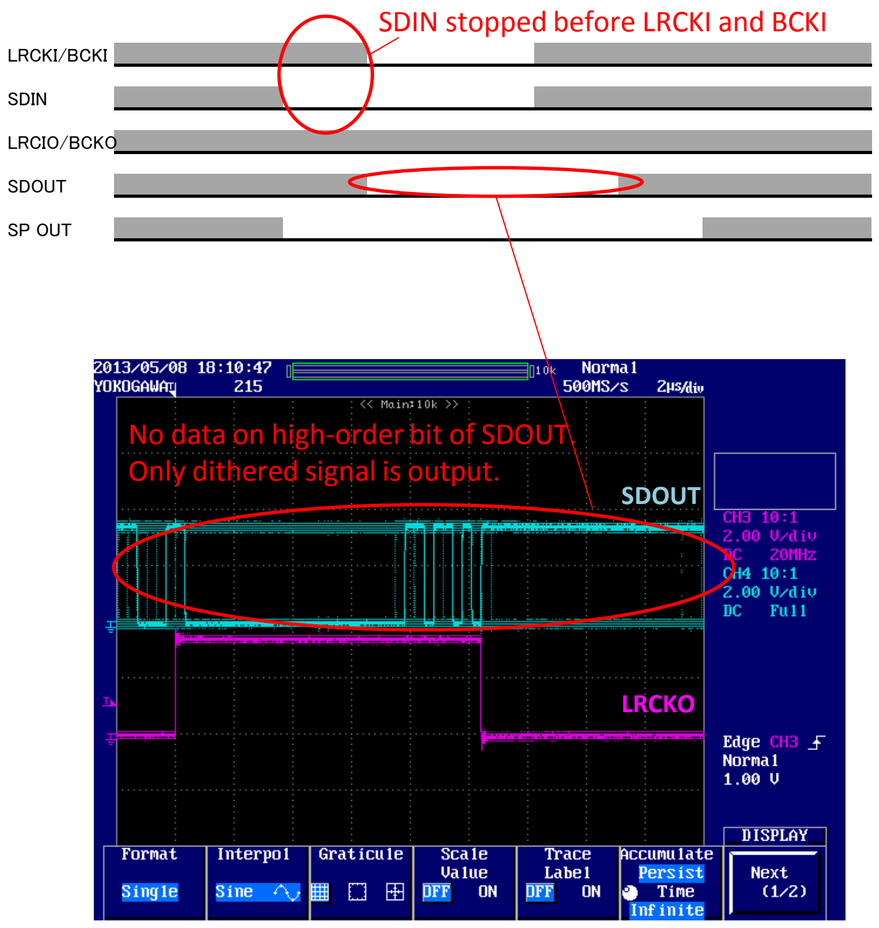


Fig.1

NG case (Data on high-order bit of SDOUT at no LRCKI, BCKI and SDIN input)

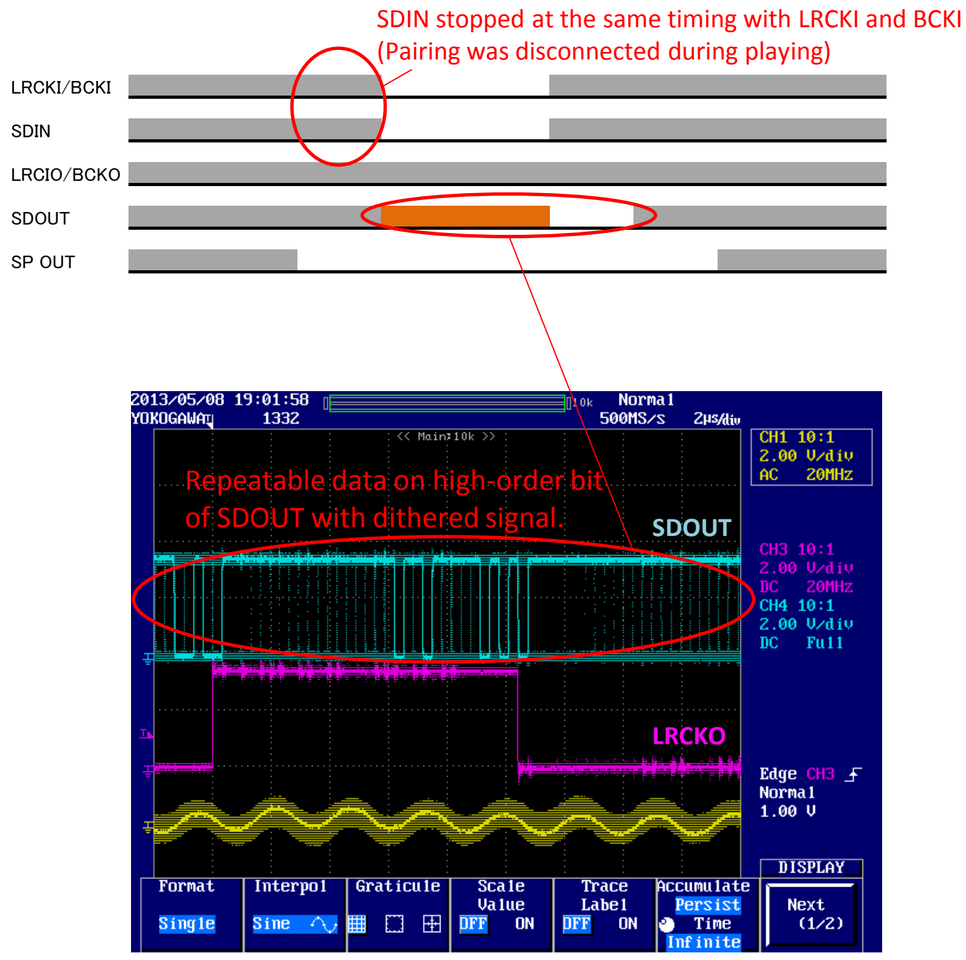


Fig.2

Captured data of SDOUT (Converted to analog data)

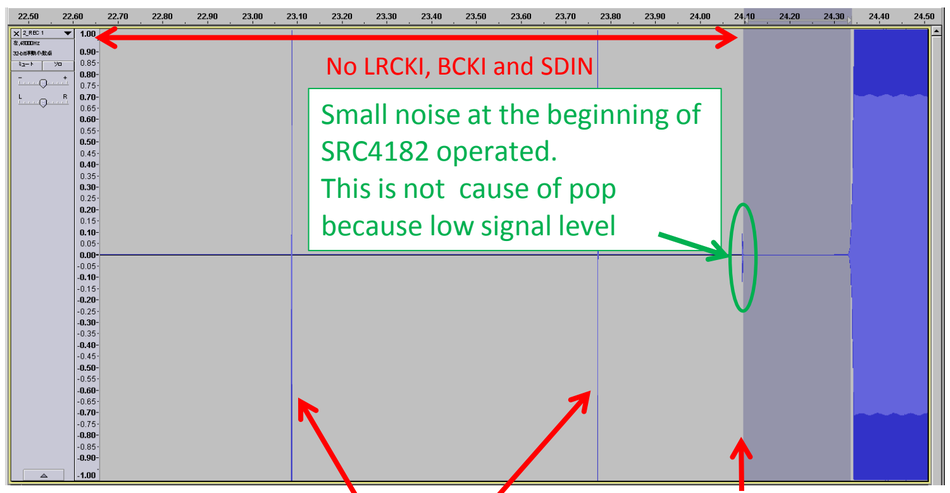


Fig.5

Repeatable signal was output although no SDIN input. This period is 32768Sample (Fs=48kHz).
The pop is happened if this repeatable signal is occurred during delay period as Fig.3

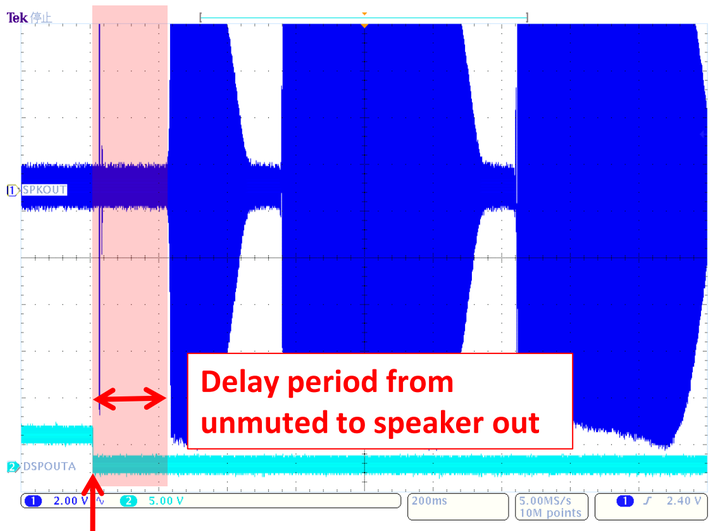


Fig.3

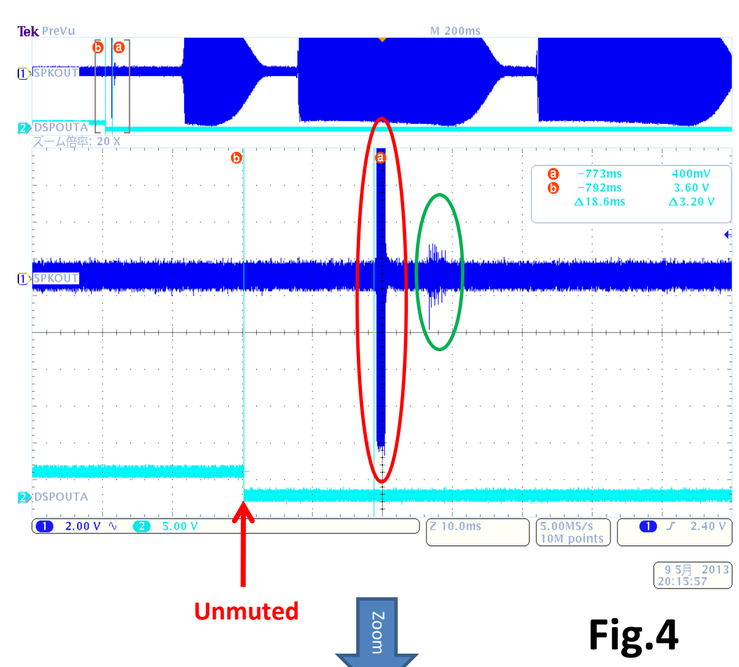


Fig.4

This signal looks like a last part of signal to SDIN.
Then our customer suspect that SRC4182 output the signal periodically with no SDIN, and this output signal is the same with signal which is input to SDIN when LRCKI and BCKI are stopped.

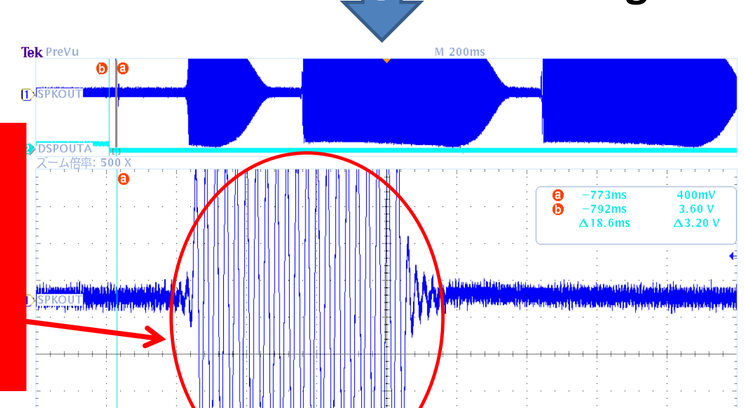


Fig.5