SCH:

Schematic diagram, transmitter side and receiver side is the same circuit. Customer tried both with 27M or without 27M crystal.

Receiver side:



Transmitter side:



Eye Diagram:

CDR ON

CDR OFF

The phenomena,

1. The configuration data has been written to CDR correctly by reading out to compare.
2. When testing with SMPTE pattern (270M, 1.485G, 2.97G), with CDR in line, lock bit has been asserted. But eye diagram is much worse (more jitter, or even crashed eye diagram) when CDR is in line. After bypass the CDR, it’s much better and we can get clear eye diagram.

**Register settings:**

Configuration and schematic diagram

1. Configuration, registers of CDR, start from 0 to 0x45.

code unsigned char TXCDR\_Setting[70] =                                                      // 0x45

{

         0x0,0x0,0x0,0x0,0x06,0x06,0x0,0x0,0x0,0x02,0x0,0x0,0x0,0x0,0x0,0x0,

         0x0,0x88,0xf2,0x0,0x13,0x0,0x0,0x0,0x0,0x0,0x0,0x0,0x24,0x81,0x13,0x0,

         0x18,0x0,0x0,0x40,0x0,0x0,0x0,0x0,0x0,0x0,0x0,0x0,0x0,0x0,0xdb,0xe6,

         0xdc,0x1a,0xdb,0xae,0xdb,0xe1,0xef,0xe4,0xf0,0x1c,0xde,0x1f,0xde,0x53,0x0c,0x0,

         0x0,0x0,0x0,0x0,0x0,0x0

};

code unsigned char RXCDR\_Setting[70] =                                                      // 0x45

{

         0x0,0x0,0x0,0x0,0x06,0x06,0x0,0x0,0x0,0x02,0x0,0x0,0x0,0x0,0x0,0x0,

         0x0,0x88,0xf2,0x0,0x13,0x0,0x0,0x0,0x0,0x0,0x0,0x0,0x24,0x81,0x13,0x0,

         0x18,0x0,0x0,0x40,0x0,0x0,0x0,0x0,0x0,0x0,0x0,0x0,0x0,0x0,0xdb,0xe6,

         0xdc,0x1a,0xdb,0xae,0xdb,0xe1,0xef,0xe4,0xf0,0x1c,0xde,0x1f,0xde,0x53,0x0c,0x0,

         0x0,0x0,0x0,0x0,0x0,0x0

}; Customer **only configure (write) those R/W registers.**