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ISO7xxx

Digital Capacitive Isolators Training Guide

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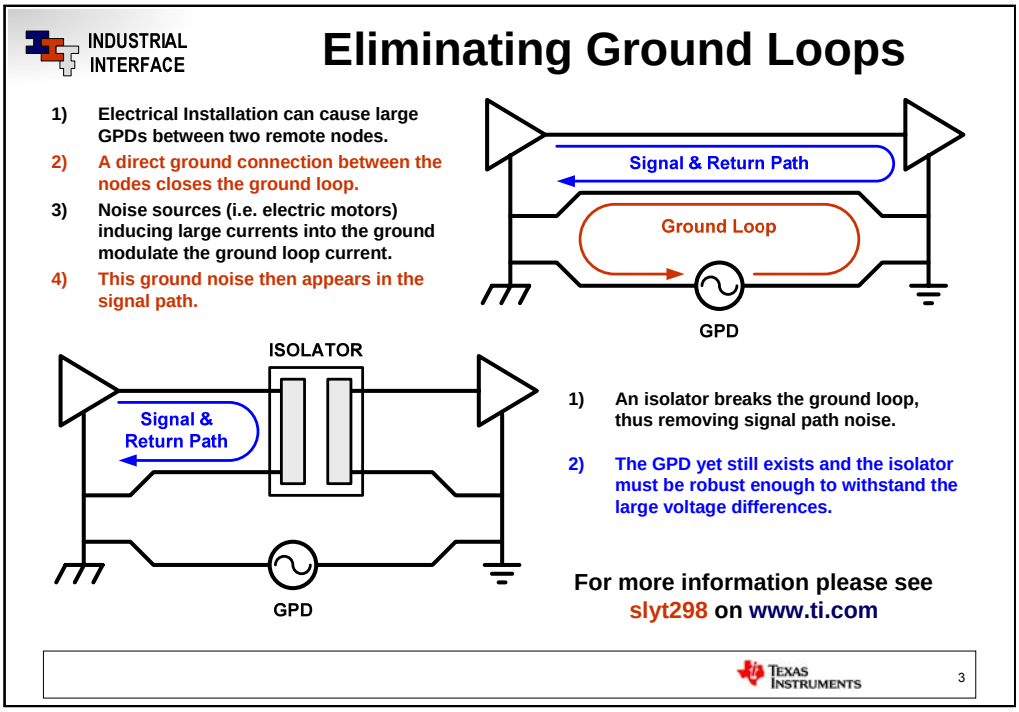
What is (Galvanic) Isolation?

Isolation

- **is a means of preventing current from flowing between two communicating points while allowing the transmission of data or power between these points.**
- **is used to eliminate ground loops while with-standing large ground potential differences (GPDs).**



For data transmission systems it is common to use local grounds as reference potential. Remote located network nodes of a communication network usually draw their supply from different points in the electrical installation system (see **slyt298** on www.ti.com). Remote located power sources, however, can experience large ground potential differences due to multiple, non-standardized, earthing techniques, which are also the cause for multiple ground paths.

Then, when providing a direct connection (i.e. a ground wire) between the transmitter ground and a remote receiver ground, a ground loop has been created. Ground loop currents can be extremely high, because they connect different ground potentials via low-impedance wire.

Thus high loop current can induce voltages into transmission signal wires causing signal distortion and possible data errors.

Breaking ground loops through galvanic isolation not only prevents loop currents but also presents the most reliable method of dealing with high ground potential differences.

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Terminology

Working voltage is the voltage that may be applied continuously across the Isolation barrier. The two most common voltage levels are 560Vpk and 890 Vpk.

Isolation voltage is the voltage that may occur temporarily across the barrier. Typical test durations are 10 sec (UL) or 1 min (VDE). Typical test levels are 4 kV or 6 kV.

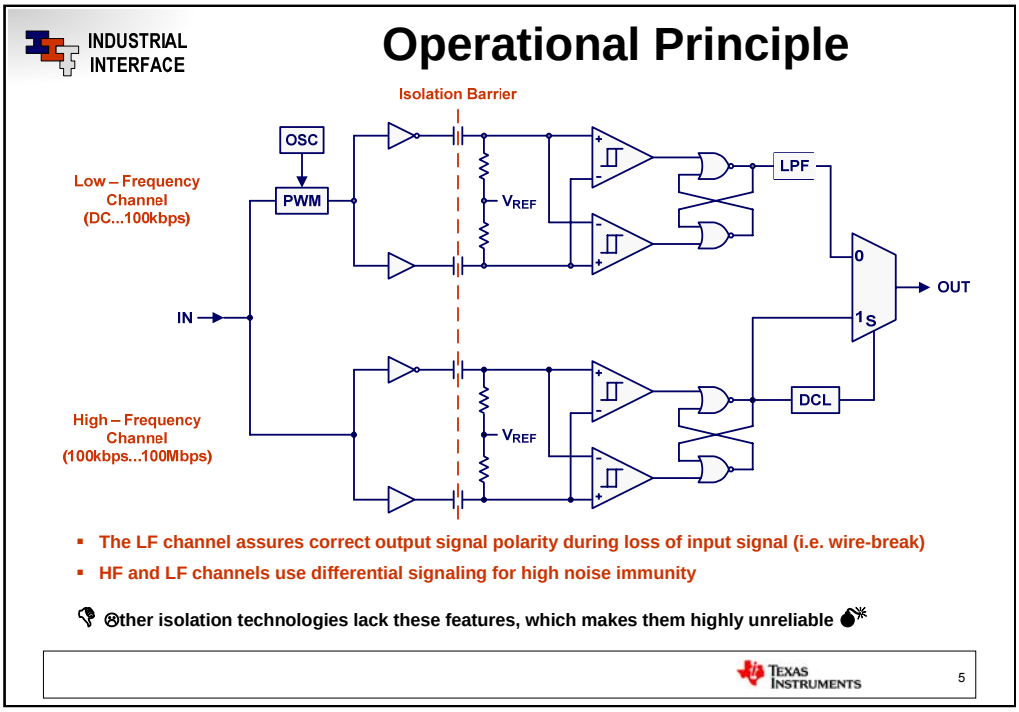
Basic Isolation assumes a single level of isolation rated for 560Vpk working and , 4kVpk transient voltage. It is applicable for most industrial applications and AC-equipment < 400Vrms, and for consumer electronics.

Reinforced Isolation assumes a single level of isolation providing the same reliability as a two-layer isolation. It is mostly rated at 890Vpk working voltage, 6kVpk transient voltage, and/or 10kV surge voltage. It is applicable for future medical applications and today's AC equipment > 400Vrms.

Up to now, Medical only requires 5kVrms transient.

Common Mode Transient Suppression (CMTS) discusses the quick change in ground potential (primary to secondary). It's given as the dV/dt up to which no false toggling of the output will occur (e.g. 35kV/us).

Creepage and Clearance discusses the surface-distance that may conduct if wet/polluted, respectively the air-distance. For 560V/4kV mostly 4mm is sufficient, for 890V/6kV mostly 8mm is needed. This often depends on the degree of pollution.

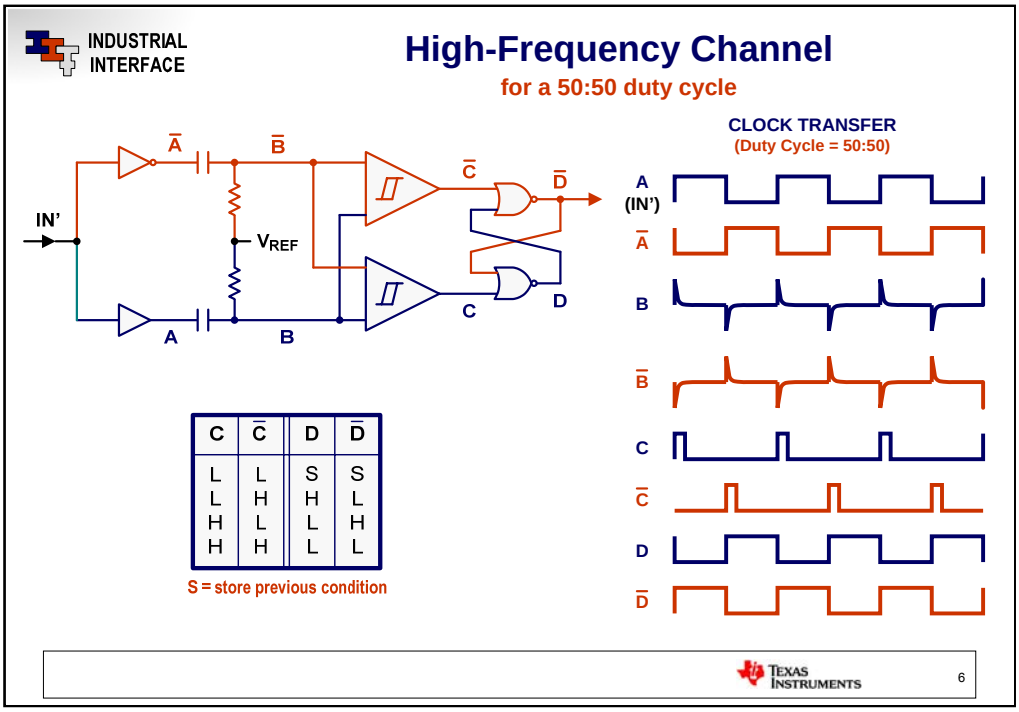


The capacitive isolator consists of two data channels, a high-frequency channel (HF) with a bandwidth from 100 kbps up to 100 Mbps, and a low-frequency channel (LF) covering the range from 100 kbps down to DC.

While the HF channel performs the normal, high-speed data transfer, the LF channel is necessary to detect low-frequency signals, or even the loss-of-signal (LOS) in the case of a wire-break, and to assure the correct signal polarity at the input is transferred to the output.

In principle, a single-ended input signal entering the HF-channel is split into a differential signal via the inverter gate at the input. The following capacitor-resistor networks differentiate the signal into transients, which then are converted into differential pulses by two comparators. The comparator outputs drive a NOR-gate flip-flop whose output feeds an output multiplexer. A decision logic (DCL) at the driving output of the flip-flop measures the durations between signal transients. If the duration between two consecutive transients exceeds a certain time limit, (*as in the case of a low-frequency signal*), the DCL forces the output-mux to switch from the high- to the low-frequency channel.

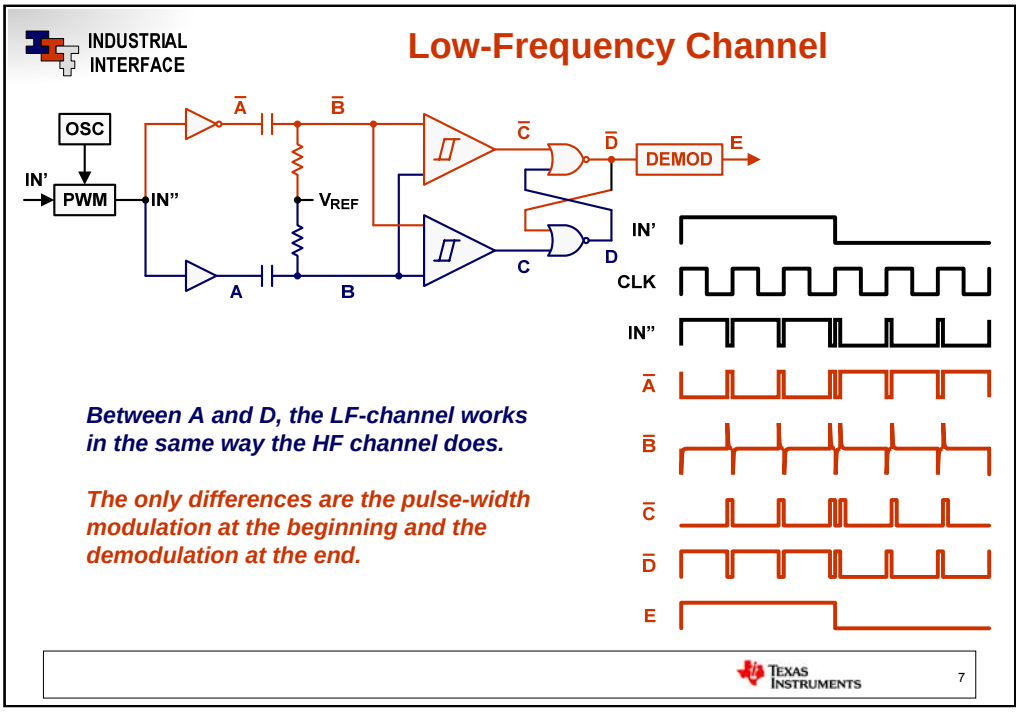
Because low-frequency input signals require the internal capacitors to assume prohibitively large values, these signals are pulse-width modulated (PWM) with the carrier frequency of an internal oscillator, thus creating a sufficiently high frequency, capable of passing the capacitive barrier. As the input is modulated, a low-pass filter (LPF) is needed to remove the high-frequency carrier from the actual data before passing it on to the output multiplexer.



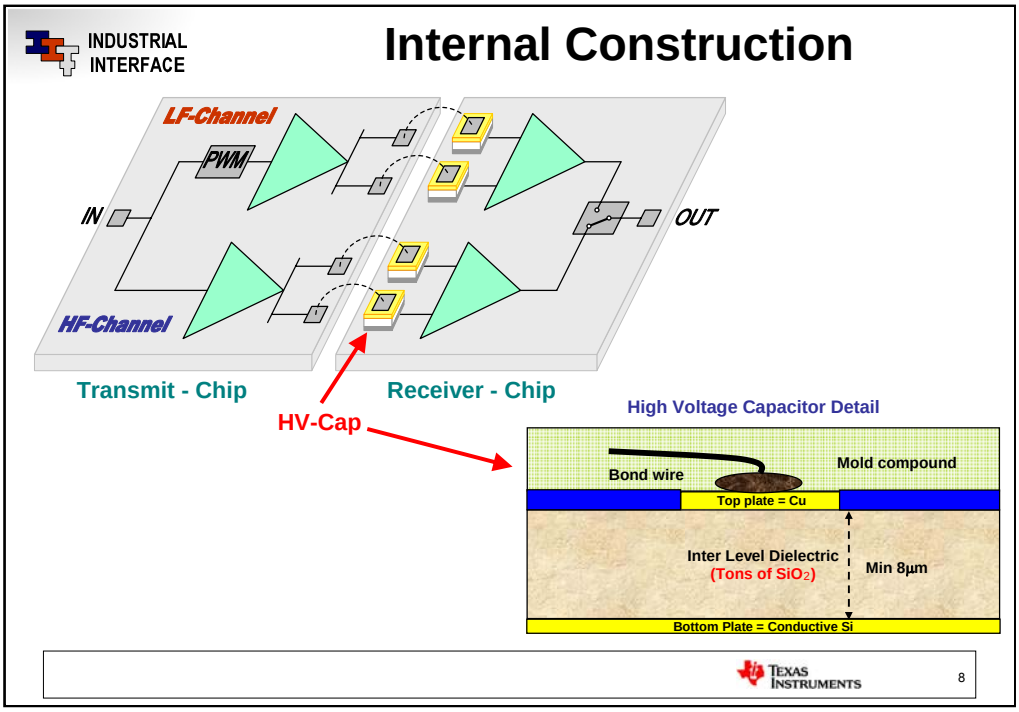
C	$\overline{C}$	D	$\overline{D}$
L	L	S	S
L	H	H	L
H	L	L	H
H	H	L	L

This slide presents the high-frequency channel and the waveforms at specific points of the signal chain. The single-ended input signal is split into the differential signal components A and /A. Each signal component is then differentiated into the transients B and /B. The following comparators compare the differential transients to one another. As long as the positive input of a comparator is on higher potential than its negative input, the comparator output will present a logical High, thus converting an input transient into a short output pulse.

The output pulses set and reset a NOR-gate flip-flop. From the truth table we see that the NOR-gate configuration presents an inverting flip-flop, meaning that a High at input C sets output /D to High, and a High at /C sets D to High. Because the comparator output pulses are of short duration, there will be times where both outputs are low. During this time the flip-flop stores its previous output condition. Since the signal at /D is identical in shape and phase with the input signal, /D becomes the output of the high-speed channel and is connected to the output multiplexer.



In the LF channel slow input signals are pulse-width modulated with a high-frequency carrier such, that a High-level yields a 90:10 duty cycle and a Low level a 10:90 duty cycle at location A. From there on, signal processing is identical with the one in the high-speed channel. The only exception is, that the high-frequency content of the low-speed channel (/D) is filtered by an R-C low-pass before being passed on to the output multiplexer (E).



Internally a capacitive isolator consists of two dies (chips), a transmitter chip and a receiver chip. The receiver chip contains the four, vertically structured, high-voltage capacitors and the receiver logic.

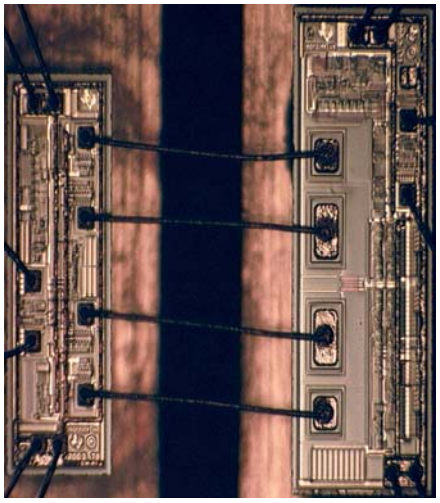
The cross cut through a capacitor shows the top plate connecting to the transmitter chip via bond-wire, while the bottom plate connects to the receiver logic.

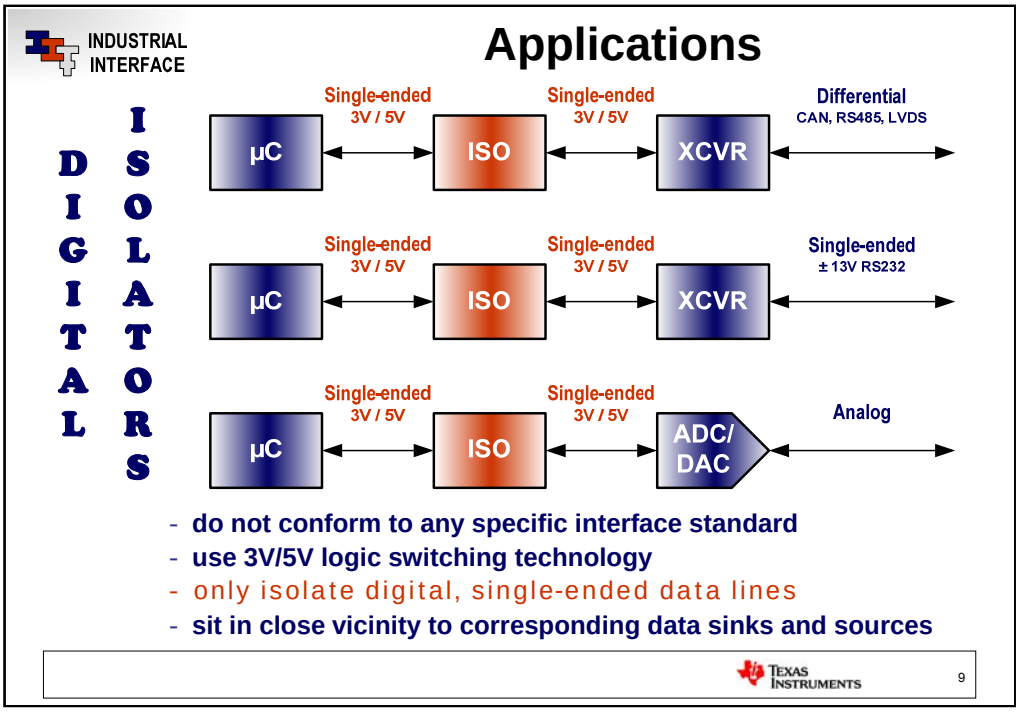
In between the plates is an 16µm thick layer of silicon-dioxide, SiO_2, also known as Glass.

The main advantage of SiO_2 is its small aging effect which translates directly into high reliability and long life time expectancy of > 28 years.

Another benefit of using SIO_2 in isolators is, that it can be produced using standard semiconductor manufacturing processes, which translates to lower production cost and thus lower cost to the customer.

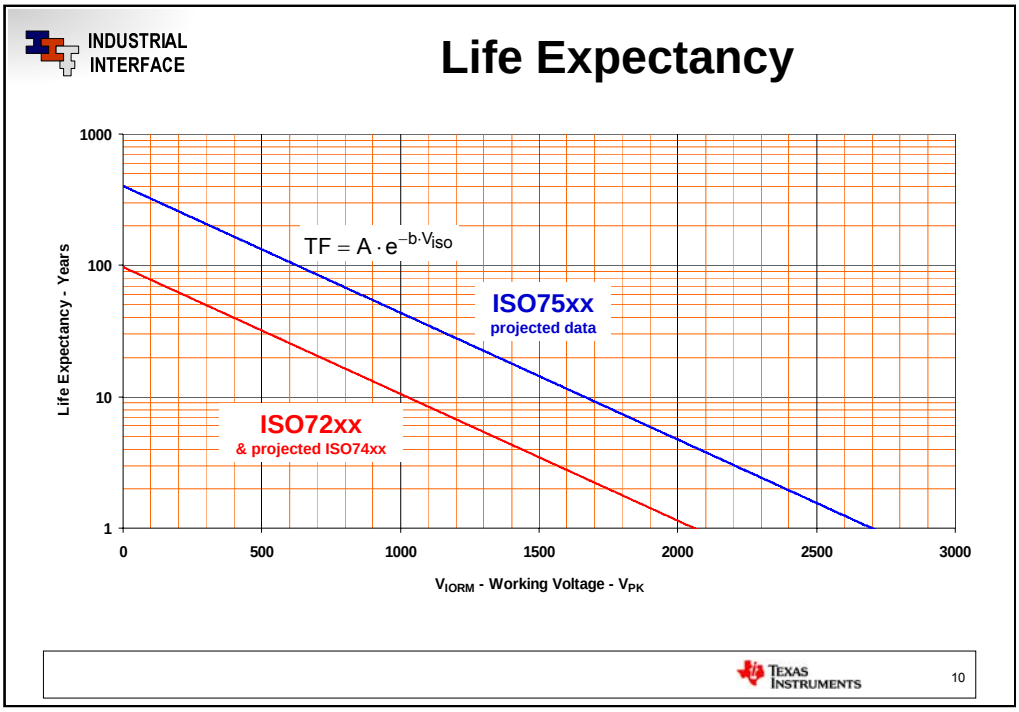
Actual Die Picture





All digital isolators utilize single-ended, 3V/5V CMOS – logic, switching technology. Their nominal supply voltage range is specified from 3.3V to 5V for both supplies, V_{CC1} and V_{CC2}, and allows any combination of these values.

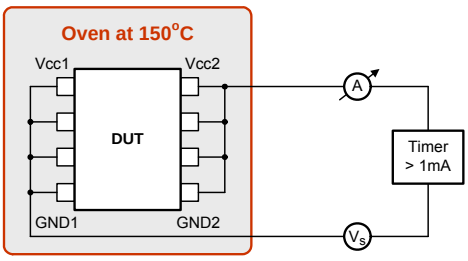
When designing with digital isolators, it is important to keep in mind that due to the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended, 3V/5V digital signal lines.



Time-dependent dielectric breakdown (TDDB) is an important failure mode for dielectric materials like silicon dioxide (SiO2) as it determines the life time expectancy of an isolator.

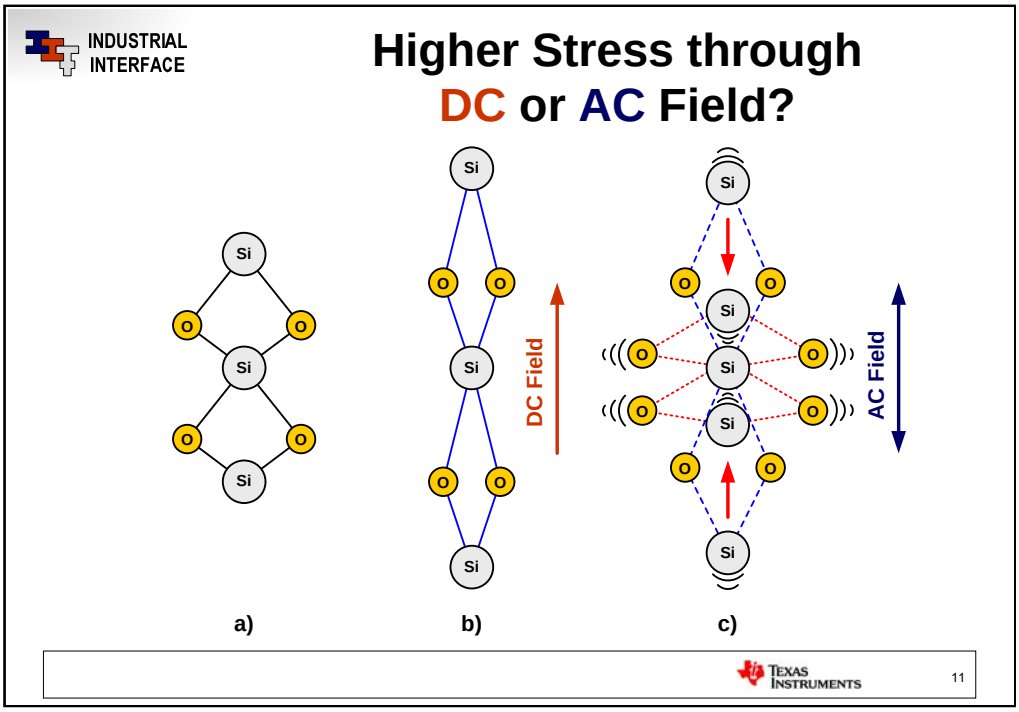
Dielectrics have impurities and imperfections due to manufacturing which cause the insulation properties to change over time and result in the eventual failure of the dielectric. These changes are accelerated by applying an electric field across the dielectric and/or by increasing its temperature.

The slide above shows the life expectancy of the new capacitive isolators as a function of the working voltage at 150 ^{o}C ambient temperature. The determination of the life expectancy is based on the TDDB E-model, the most widely accepted and used model for capacitor breakdown. The E-model is backed by a theoretical physical degradation mechanism and is considered as the most conservative of all models in the literature.



The basic test methodology is the application of a stress voltage from the input to the output of the isolator under test using a high-voltage source, while maintaining the still-air, ambient temperature at 150°C. The start of the test activates a timer; this timer stops when the current in the circuit exceeds 1 mA, which means that the dielectric had failed. The TF (Time-to-Failure) is noted for each applied test voltage.

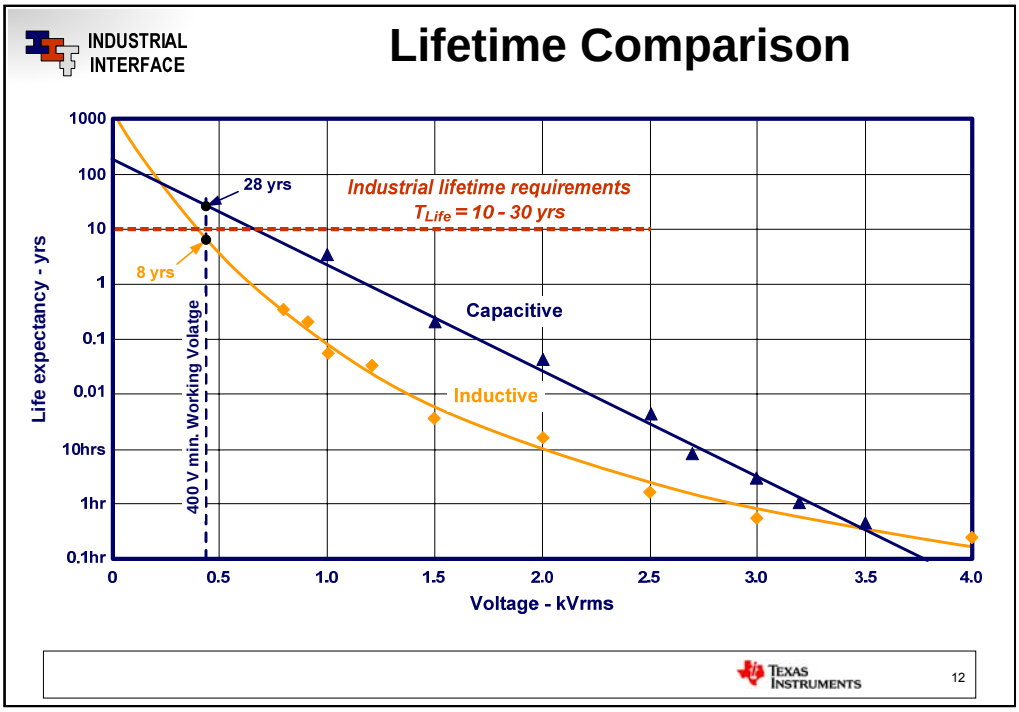
TI's preference for using the TDDB E-model is based on the fact that the E-model is conservative and results in high-confidence predictions compared to any other models or a best data fit methodology.



The often-raised question, whether an AC or DC originated E-field presents a higher stress level on the dielectric, is answered with the rather intuitive example in Slide 12. Here the SiO_2 lattice is resembled by spheres, which are attached to another through elastic strings.

While **Figure a)** shows the lattice at rest, **Figure b)** demonstrates the application of a DC voltage across a dielectric by pulling the upper Si-sphere to its maximum extend in the direction of the arrow. While there is a force working on the connecting string, the lattice can be kept in this position until fatigue sets in and the strings break.

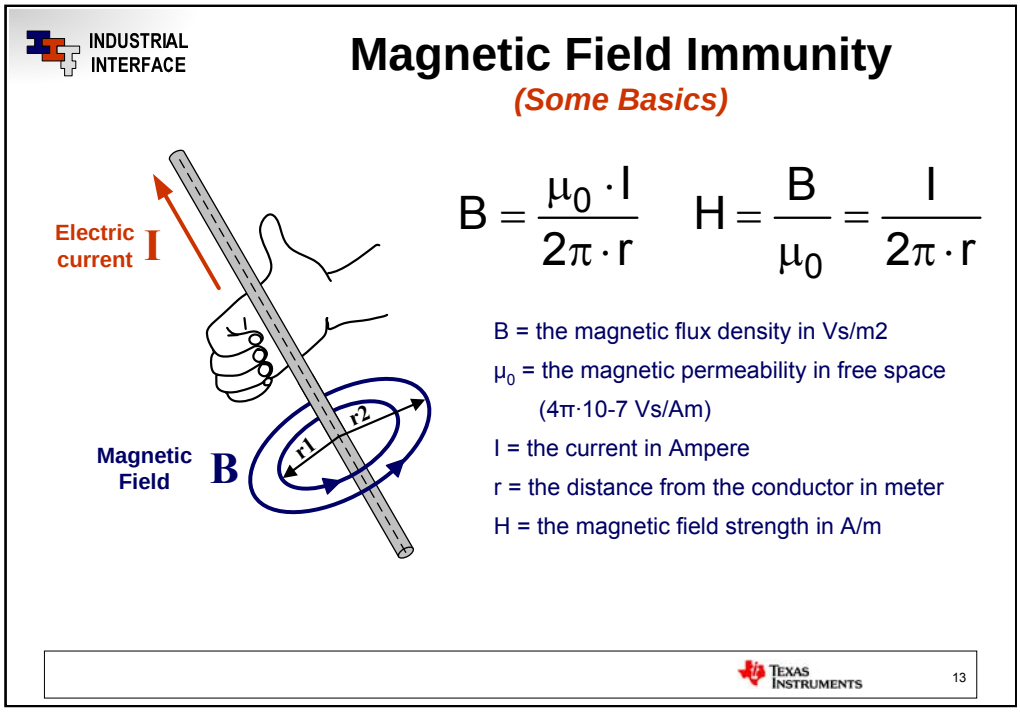
In **Figure c)** the sphere lattice is pushed and pulled resembling an AC field. In this case, elastic fatigue occurs earlier in time than in Figure b). This is equivalent to the earlier wear-out stage of a dielectric when stressed by electric AC fields.



A comparison between the TDDB curves of capacitive isolators and inductive isolators shows that the lifetime prediction for capacitive isolators follows the E-model, while the magnetics utilize the 1/E-model.

For inductive isolators the extrapolated lifetime with 8 years at 400V is in alignment with the life expectancy shown in the previous reliability table of < 10 years. The curve for capacitive isolators shows a significant longer lifetime of 28 years at 400V.

Note that typical industry lifetime expectations range from 10 to 30 years. As can be seen, at voltages between 1kV and 2.5kV, the life expectancy of capacitive isolators is more than 10-times longer than for inductive isolators.



The application environment of digital capacitive isolators often includes close proximity to large electric motors, generators, and other magnetic-field generating equipment. Exposure to these large electromagnetic fields raises concern about the possibility of data corruption, as the electromotive force (EMF), the voltage created by these fields, can interfere with the transferred data signal. Due to this potential threat many users of digital isolators demand proof of an isolator's high magnetic field immunity.

While there are many digital isolator technologies claiming high magnetic field immunity (MFI), capacitive isolators provide an almost infinitely high MFI due to their design and internal construction. This section explains the details behind it.

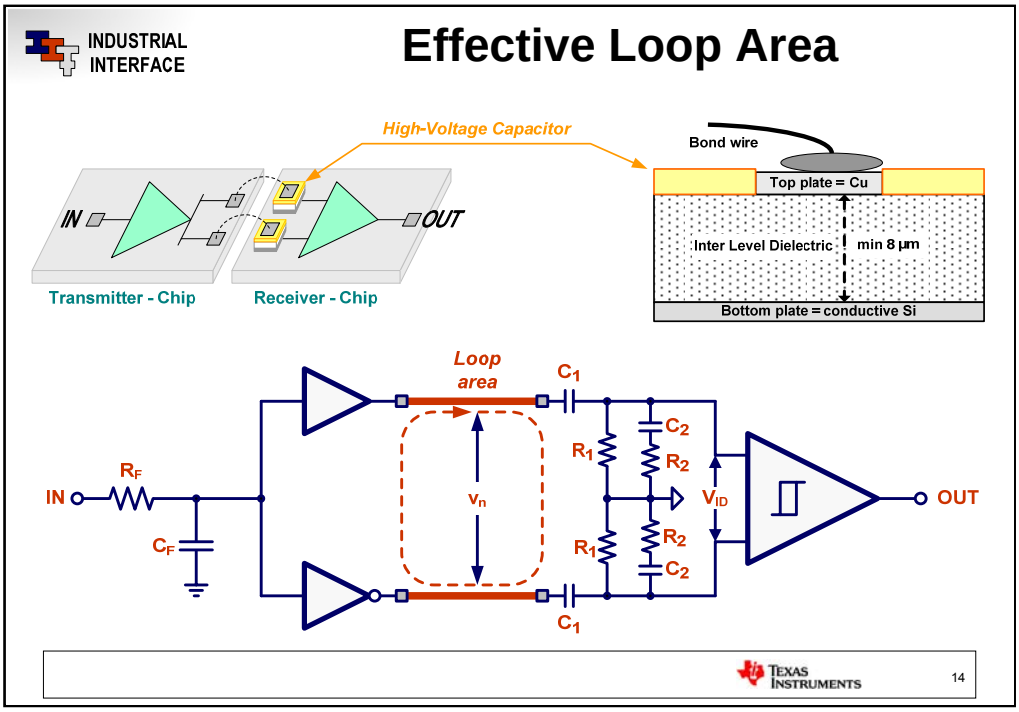
The slide above shows a current-carrying conductor, such as one of the supply lines to an electric motor, which is surrounded by a magnetic field, created by the current flowing through it. The direction of the magnetic field is easily determined by applying the right-hand rule. This rule says that **when grabbing the conductor with the right hand and the thumb pointing in the direction of the current, the fingers encircling the conductor indicate the direction of the magnetic field**. Thus, the plane of the magnetic flux lines is always perpendicular to the current.

The figure shows the magnetic field for a DC current. For an AC current the right-hand rule is applied in both directions and the magnetic field changes with the same frequency, ω, as the AC current: $B(\omega) \sim I(\omega)$.

The magnetic field, or more accurately, the magnetic flux density and its corresponding magnetic field- strength lessen with increasing distance from the center axis of the conductor. These relations are expressed through the equations above.

When the magnetic field lines cross a close-by conductor loop, they generate an electromotive force (EMF) whose magnitude depends on the magnetic flux density (B), its frequency (f), and the loop area (A) via:

$$\mathbf{EMF\ (f) = B \cdot 2\pi f \cdot A} \qquad \mathbf{(1)}$$



All isolators possess conducting loops in some shape or form for magnetic fields to cross and EMF to generate. If large enough this EMF, which is superimposed onto signal voltages, can lead to erroneous data transmission. In fact, some isolation technologies are highly susceptible to magnetic interference. To understand why capacitive isolators are unaffected by magnetic fields, we need to understand their internal construction.

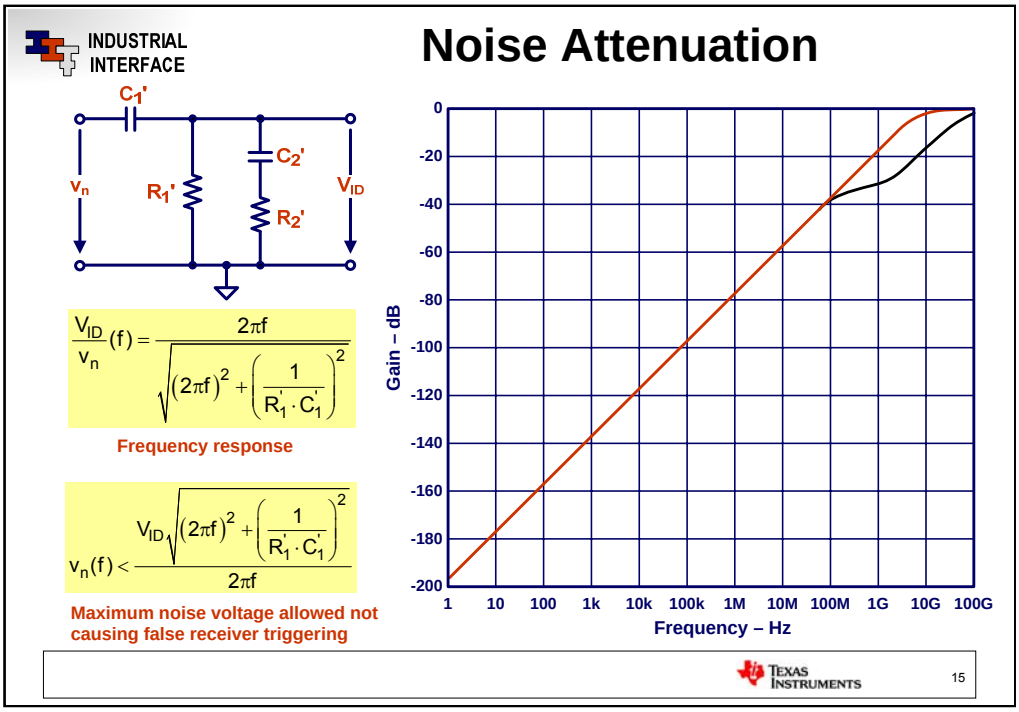
Capacitive isolators consist of two silicon chips, a transmitter and a receiver chip. Data transfer occurs across a differential isolation barrier formed by two capacitors with a copper top plate and a conductive silicon bottom plate on each side of a silicon dioxide (SiO2) dielectric.

The input drivers of the transmitter chip connect via bond wires to the top plates of the isolation capacitors on the receiver chip. With the bottom plates of the capacitors connecting to the receiver inputs, a conducting loop is created. The lower figure shows the equivalent circuit diagram of the isolation barrier design and points out the loop area between the golden bond wires.

Evidently a magnetic field crossing this loop will generate an EMF that represents a noise input voltage, v_{n1}, to the following RC network. A second differential noise component often encountered is due to the conversion from common-mode to differential noise, v_{n2}. Both noise components add to the combined noise, v_n. Examining only the effects of EMF, v_n is conservatively split into half, thus making

$$\mathbf{EMF = v_n/2} \qquad \mathbf{(2)}$$

In order to trigger the receiver, the output of the RC network must provide a differential input voltage, V_{ID}, that exceeds the receiver input thresholds. Whether the possibility of false triggering is given, depends on the gain response, G(f), of the RC network.



The conversion from a differential to a single-ended network (Figure 4) simplifies the derivation of G(f) but requires that C1' = 2C1, R1' = R1/2, C2' = 2C2, and R2' = R2/2.

As the simulation confirms, the R-C network is a first order high-pass filter with significant attenuation below 100 MHz.

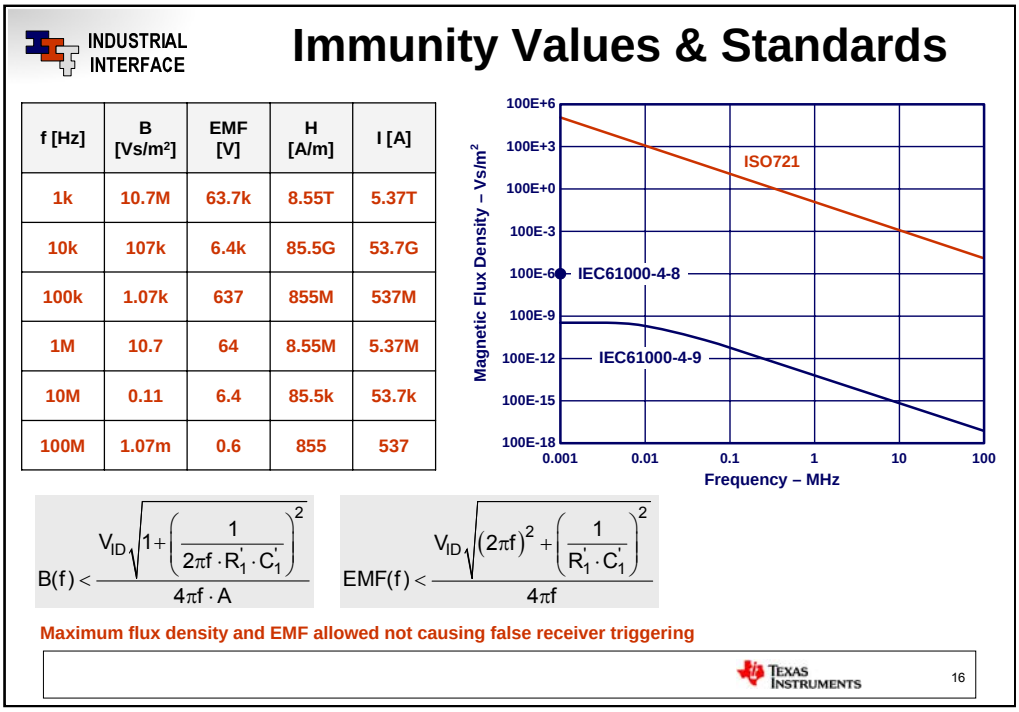
C1' and R1' being the dominant components up to 100 MHz (green curve). Beyond this frequency the parasitic components C2' and R2' become effective causing a slight deviation from the linear slope.

For up to 100 MHz therefore, the gain response is:

$$\frac{V_{ID}}{v_n} = \frac{2\pi f}{\sqrt{(2\pi f)^2 + \left(\frac{1}{R_1' \cdot C_1'}\right)^2}}$$

Solving for v_n provides the maximum noise level allowed that does not cause false receiver triggering:

$$v_n(f) < \frac{V_{ID}\sqrt{(2\pi f)^2 + \left(\frac{1}{R_1' \cdot C_1'}\right)^2}}{2\pi f}$$



Substituting v_n with Equation 2 provides the maximum tolerable EMF, and further substitution of EMF with Equation 1 yields the maximum possible magnet flux density. The final equations for EMF and B are shown above.

Inserting the isolator specific numerical values for the receiver input threshold, the effective RC time constant, the effective loop area, and the frequency range of interest provides the frequency dependent values for B and EMF listed in the table above.

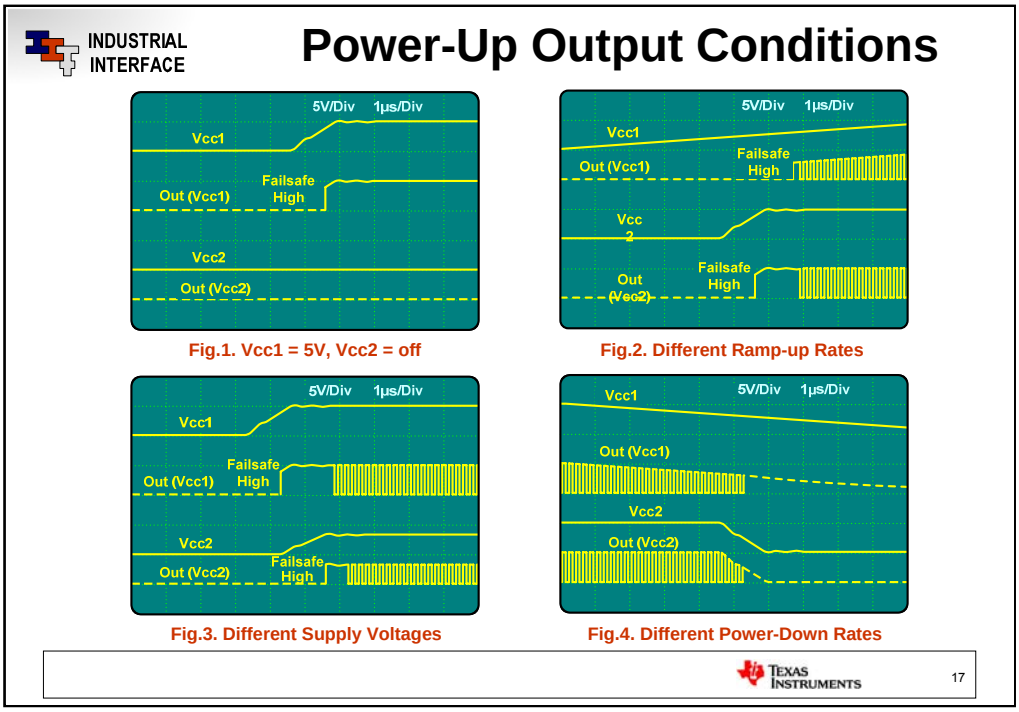
Form the enormous high values it is evident that neither a low-frequency current of 5 Terra amps, nor some 500 A at 100 MHz are capable of stopping this isolator from working correctly.

The reason for this almost infinite magnetic field immunity (MFI) lies in the location of the isolation capacitors. If these capacitors would reside on the transmitter chip, any generated EMF in the bond wires would reach undisturbed the receiver inputs.

Evidently such high MFI values are impossible to test in practice. The data sheets of capacitive isolators therefore only show the modest value of 1000 A/m as the practical test field. However, unshielded capacitive isolators easily pass the Class 5 MFI requirements of the IEC61000-4-8 and IEC61000-4-9 standards.

These standards describe the application of power-frequency fields up to 100 A/m and pulsed fields up to 1000 A/m respectively. Class 5 defines severe industrial environments such as conductors, bus bars, medium- and high-voltage lines, all of which carrying tens of kA. Further included are ground conductors of the lightning protection system, or high structures (such as line towers) carrying the whole lightning current. Switchyards of heavy industrial plants and power stations also represent this type of environment.

The right diagram compares the calculated magnetic field immunity thresholds of a capacitive isolator with the Class-5 (highest) test levels of IEC 61000-4-8 and IEC 61000-4-9.



When powering up the ISO72xx family of digital isolators, the condition of an isolator output solely depends on its corresponding output supply.

As long as the output supply is below an internally fixed voltage threshold of approximately 2.5V, the output is switched-off, or high-impedance. When the supply voltage reaches 2.5V, the output assumes failsafe-high. At this moment the output connects internally to the supply rail and continues tracking with the supply voltage until the full supply level is reached.

Figure 1 gives an example. While Vcc2 and its corresponding output are off, Vcc1 ramps-up from 0V to 5V. Below 2.5V the output is high-impedance (dotted line), above 2.5V the output tracks with Vcc1.

Figure 2 presents the case for equal supply voltages, Vcc1 = Vcc2 = 5V, but different ramp-up slopes. Because Vcc2 ramps-up faster then Vcc1, the Vcc2 related output assumes failsafe-high before the output on the Vcc1-side.

Note that for the Vcc1 related output the timely distance failsafe-high and data transfer is relative short. This is because Vcc2, the input supply for the corresponding transmitter is fully established at that time, and data output only depends on the development of the output supply, Vcc1.

In the other direction, Vcc2 is the fully established output supply. The long delay between data output and failsafe-high is due to the slow increase of the corresponding input supply, Vcc1, and the non-activated transmitters.

In **Figure 3** both supplies have a similar ramp-up but differ in their final supply voltage levels. Again, transfer data on the output assuming failsafe-high first can only occur, once its corresponding transmitter supply is sufficiently established.

In the opposite direction, however, transfer data occurs shortly after failsafe-high.

Figure 4 represent the power-down events at different rates. The outputs on both sides of the isolator track with their corresponding supplies. Once a supply has dropped below the internal failsafe threshold, its corresponding output assumes high-impedance.

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Summary

Performance

Digital Isolators provide…

- functional isolation up to 4 kV & 5 kV
- high reliability
- long lifetime
- wide bandwidth
- high magnetic field immunity
- low supply current at high speed