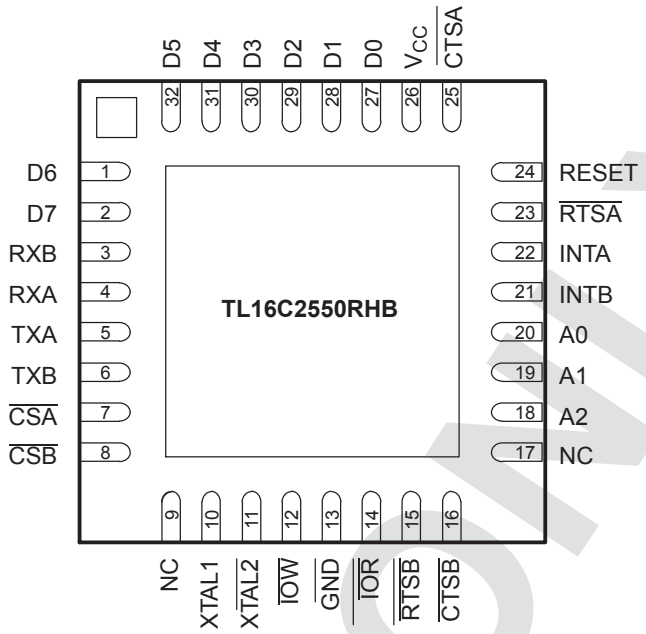
RHB PACKAGE
(TOP VIEW)



NC − No internal connection

NOTE: The 32-pin RHB package does not provide access to DSRA, DRRB, RIA, RIB, CDA, CDB inputs, and OPA, OPB, RXRDYA, RXRDYB, TXRDYA, TXRDYB outputs.

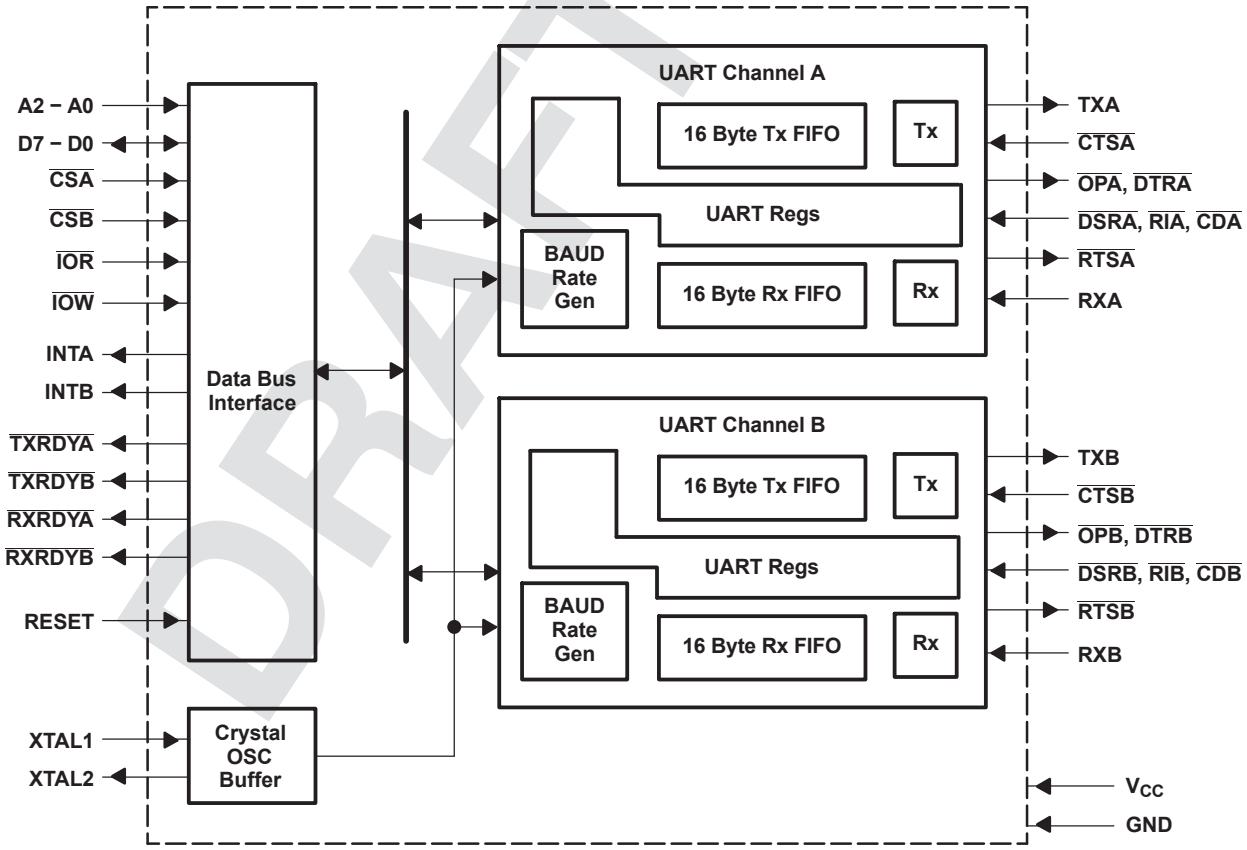


Figure 1. TL16C2550 Block Diagram

DEVICE INFORMATION

TERMINAL FUNCTIONS

TERMINAL				I/O	DESCRIPTION
NAME	PFB NO.	FN NO.	RHB NO.		
A0	28	31	20	I	Address 0 select bit. Internal registers address selection
A1	27	30	19	I	Address 1 select bit. Internal registers address selection
A2	26	29	18	I	Address 2 select bit. Internal registers address selection
$\overline{CDA}$, $\overline{CDB}$	40, 16	42, 21	–	I	Carrier detect (active low). These inputs are associated with individual UART channels A and B. A low on these pins indicates that a carrier has been detected by the modem for that channel. The state of these inputs is reflected in the modem status register (MSR).
$\overline{CSA}$, $\overline{CSB}$	10, 11	16, 17	7, 8	I	Chip select A and B (active low). These pins enable data transfers between the user CPU and the TL16C2550 for the channel(s) addressed. Individual UART sections (A, B) are addressed by providing a low on the respective $\overline{CSA}$ and $\overline{CSB}$ pins.
$\overline{CTSA}$, $\overline{CTSB}$	38, 23	40, 28	25, 16	I	Clear to send (active low). These inputs are associated with individual UART channels A and B. A logic low on the CTS pins indicates the modem or data set is ready to accept transmit data from the 2550. Status can be tested by reading MSR bit 4. These pins only affect the transmit and receive operations when auto CTS function is enabled through the enhanced feature register (EFR) bit 7, for hardware flow control operation.
D0-D4 D5-D7	44 - 48 1 - 3	2 - 6 7 - 9	27 - 31 32, 1, 2	I/O	Data bus (bidirectional). These pins are the eight bit, 3-state data bus for transferring information to or from the controlling CPU. D0 is the least significant bit and the first data bit in a transmit or receive serial data stream.
$\overline{DSRA}$, $\overline{DSRB}$	39, 20	41, 25	–	I	Data set ready (active low). These inputs are associated with individual UART channels A and B. A logic low on these pins indicates the modem or data set is powered on and is ready for data exchange with the UART. The state of these inputs is reflected in the modem status register (MSR).
$\overline{DTRA}$, $\overline{DTRB}$	34, 35	37, 38	–	O	Data terminal ready (active low). These outputs are associated with individual UART channels A and B. A logic low on these pins indicates that theTLI16C2550 is powered on and ready. These pins can be controlled through the modem control register. Writing a 1 to MCR bit 0 sets the $\overline{DTR}$ output to low, enabling the modem. The output of these pins is high after writing a 0 to MCR bit 0, or after a reset.
GND	17	22	13		Signal and power ground.
INTA, INTB	30, 29	33, 32	22, 21	O	Interrupt A and B (active high). These pins provide individual channel interrupts, INT A and B. INT A and B are enabled when MCR bit 3 is set to a logic 1, interrupt sources are enabled in the interrupt enable register (IER). Interrupt conditions include: receiver errors, available receiver buffer data, available transmit buffer space or when a modem status flag is detected. INTA-B are in the high-impedance state after reset.
$\overline{IOR}$	19	24	14	I	Read input (active low strobe). A high to low transition on $\overline{IOR}$ will load the contents of an internal register defined by address bits A0-A2 onto the TL16C2550 data bus (D0-D7) for access by an external CPU.
$\overline{IOW}$	15	20	12	I	Write input (active low strobe). A low to high transition on $\overline{IOW}$ will transfer the contents of the data bus (D0-D7) from the external CPU to an internal register that is defined by address bits A0-A2 and $\overline{CSA}$ and $\overline{CSB}$
NC	12, 24, 25, 37	–	9, 17		No internal connection
$\overline{OPA}$, $\overline{OPB}$	32, 9	35, 15	–	O	User defined outputs. This function is associated with individual channels A and B. The state of these pins is defined by the user through the software settings of the MCR register, bit 3. INTA-B are set to active mode and $\overline{OP}$ to a logic 0 when the MCR-3 is set to a logic 1. INTA-B are set to the 3-state mode and $\overline{OP}$ to a logic 1 when MCR-3 is set to a logic 0. See bit 3, modem control register (MCR bit 3). The output of these two pins is high after reset.
RESET	36	39	24	I	Reset. RESET will reset the internal registers and all the outputs. The UART transmitter output and the receiver input will be disabled during reset time. See TL16C2550 external reset conditions for initialization details. RESET is an active-high input.

DEVICE INFORMATION (continued)

TERMINAL FUNCTIONS (continued)

TERMINAL				I/O	DESCRIPTION
NAME	PFB NO.	FN NO.	RHB NO.		
$\overline{RIA}$, $\overline{RIB}$	41, 21	43, 26	–	I	Ring indicator (active low). These inputs are associated with individual UART channels A and B. A logic low on these pins indicates the modem has received a ringing signal from the telephone line. A low to high transition on these input pins generates a modem status interrupt, if enabled. The state of these inputs is reflected in the modem status register (MSR)
$\overline{RTSA}$, $\overline{RTSB}$	33, 22	36, 27	23, 15	O	Request to send (active low). These outputs are associated with individual UART channels A and B. A low on the $\overline{RTS}$ pin indicates the transmitter has data ready and waiting to send. Writing a 1 in the modem control register (MCR bit 1) sets these pins to low, indicating data is available. After a reset, these pins are set to high. These pins only affects the transmit and receive operation when auto $\overline{RTS}$ function is enabled through the enhanced feature register (EFR) bit 6, for hardware flow control operation.
RXA, RXB	5, 4	11, 10	4, 3	I	Receive data input. These inputs are associated with individual serial channel data to the 2550. During the local loopback mode, these RX input pins are disabled and TX data is internally connected to the UART RX input internally.
$\overline{RXRDYA}$, $\overline{RXRDYB}$	31, 18	34, 23	–	O	Receive ready (active low). $\overline{RXRDY}$ A and B goes low when the trigger level has been reached or a timeout interrupt occurs. They go high when the RX FIFO is empty or there is an error in RX FIFO.
TXA, TXB	7, 8	13, 14	5, 6	O	Transmit data. These outputs are associated with individual serial transmit channel data from the 2550. During the local loopback mode, the TX input pin is disabled and TX data is internally connected to the UART RX input.
$\overline{TXRDYA}$, $\overline{TXRDYB}$	43, 6	11, 12	–	O	Transmit ready (active low). $\overline{TXRDY}$ A and B go low when there are at least a trigger level numbers of spaces available. They go high when the TX buffer is full.
V_{CC}	42	44	26	I	Power supply inputs.
XTAL1	13	18	10	I	Crystal or external clock input. XTAL1 functions as a crystal input or as an external clock input. A crystal can be connected between XTAL1 and XTAL2 to form an internal oscillator circuit (see Figure 10). Alternatively, an external clock can be connected to XTAL1 to provide custom data rates.
XTAL2	14	19	11	O	Output of the crystal oscillator or buffered clock. See also XTAL1. XTAL2 is used as a crystal oscillator output or buffered a clock output.

Detailed Description

Autoflow Control (see Figure 2)

Autoflow control is comprised of auto-$\overline{CTS}$ and auto-$\overline{RTS}$. With auto-$\overline{CTS}$, the $\overline{CTS}$ input must be active before the transmitter FIFO can emit data. With auto-$\overline{RTS}$, $\overline{RTS}$ becomes active when the receiver needs more data and notifies the sending serial device. When $\overline{RTS}$ is connected to $\overline{CTS}$, data transmission does not occur unless the receiver FIFO has space for the data; thus, overrun errors are eliminated using ACE1 and ACE2 from a TLC16C2550 with the autoflow control enabled. If not, overrun errors occur when the transmit data rate exceeds the receiver FIFO read latency.