Isolated RS-485 Extender

Extending a half-duplex RS-485 beyond 1200 m requires an isolated half-duplex extender (Figure 1). The extender design comprises two half-duplex transceivers, a digital isolator and some control logic that performs a bit dependent control of enabling and disabling the extender's driver and receiver sections.

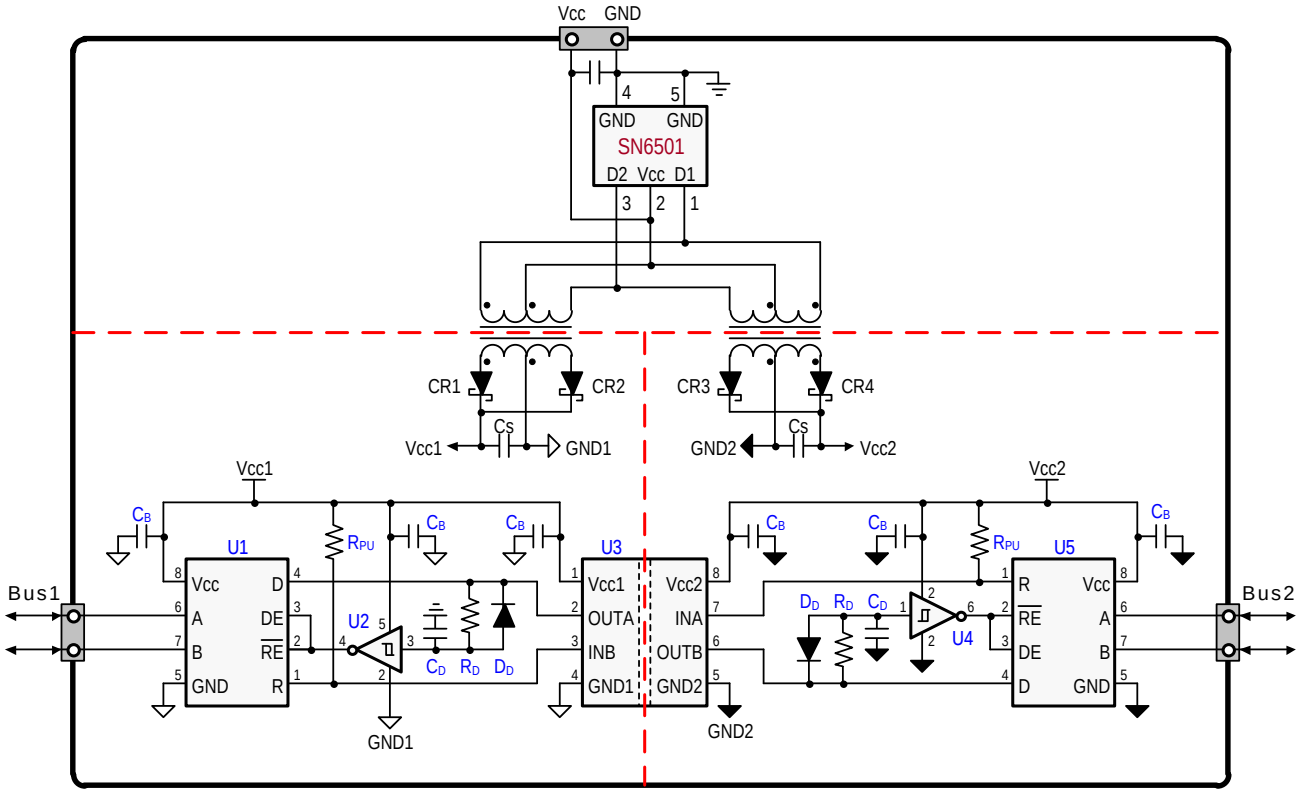

Figure 1. Isolated half-duplex extender design

The underlying principle of the extender is that logic low states are actively driven while logic high states are passively represented by the bus failsafe voltage, V_{FS}. ***This of course implies that failsafe biasing is applied at the bus.***

Stepping through the functional sequence of the repeater clarifies its operation.

– During bus-idling the receiver outputs of both extender ports are high due to V_{FS}. The delay capacitors, C_D, are fully charged, driving the inverter outputs low to maintain both transceivers in receive mode.

– Then a negative bus voltage on bus 1 (representing a low-bit) drives the receiver output of U1 low, thus rapidly discharging C_D at U4 and enabling the driver in U5.

– When the bus voltage turns positive (V_{Bus1} > 200 mV) the receiver output of U1 turns high, thus forcing the driver output of U5 high while slowly charging C_D via R_D at U4. The minimum time constant (R_D x C_D) is so calculated that at the maximum supply voltage, $V_{CC\text{-}max}$, and the minimum positive inverter input threshold, $V_{TH+\,min}$, the delay time, t_D, exceeds the maximum low-to-high propagation delay, $t_{PLH\text{-}max}$, of the driver by say 30 %. For a given capacitance the required resistor value for R_D thus calculates to:

$$R_D \geq \left| \frac{1.3 \cdot t_{PLH-max}}{C_D \cdot \ln\left(1 - V_{IT+min} / V_{CC-max}\right)} \right|$$

The driver enable time is extended beyond the bit length by the delay time, t_D. This method establishes a valid high signal on the bus before the driver in U5 is disabled and its receiver enabled. Thus the receiver output of U5 is kept continuously high. Due to design symmetry the same operational sequence applies to the opposite direction from bus 2 to bus 1.

Table 1. Bill of material

Designator	Function	Device	Manufacturer
U1, U5	5V, 250 kbps RS-485 transceiver	SN65LBC184D	TI
U2, U4	Schmitt-trigger inverter	SN74LVC1G14DBV	TI
U3	Dual Isolator	ISO7221A	TI
R_D	39 k, 5%, 1/16W thick-film resistor	RC0402JR-0739KL	Yageo
R_{PU}	10 k, 5%, 1/16W thick-film resistor	RC0402JR-0710KL	Yageo
C_B	0.1 µF, 50V, Ceramic bypass capacitor	GRM188R71H104KA93D	Murata
C_D	100 pF, 50 V, Ceramic delay capacitor	C0603C101J5RACTU	Kemet
D_D	1N4448 Discharge diode	1N4448WT	Fairchild

The push-pull converter using the transformer driver SN6501 to generate two isolated 5V outputs is shown in Figure 2. Both transformers posses a turns ratio of 1:1.1, and have a saturation product of V·t = 11 Vµs. Their performance characteristics are shown in Figures 3 and 4.

The transformers are available from Wuerth-Electronics / Midcom with the order number: 760390012.

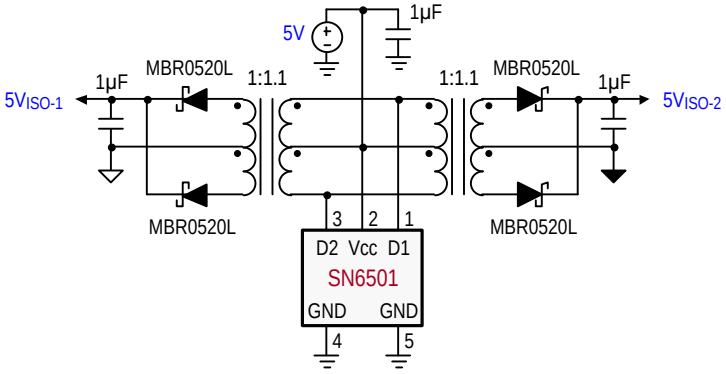

Figure 2. Isolated power supply design

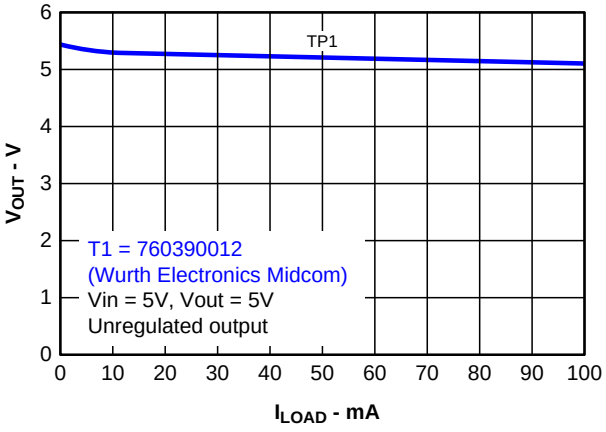

Figure 3. Output Voltage vs. Load Current

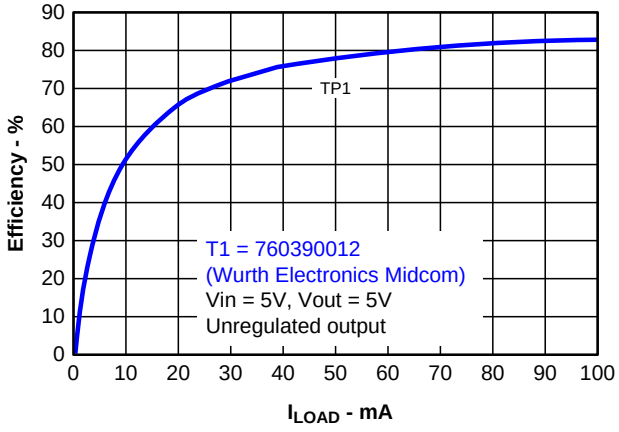

Figure 4. Efficiency vs. Load Current

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