Isolated Profibus Node Design

Many RS-485 networks use isolated bus nodes to prevent the creation of unintended ground loops and their disruptive impact on signal integrity. An isolated bus node typically includes a micro controller that connects to the bus transceiver via a multi-channel, digital isolator (Figure 1).

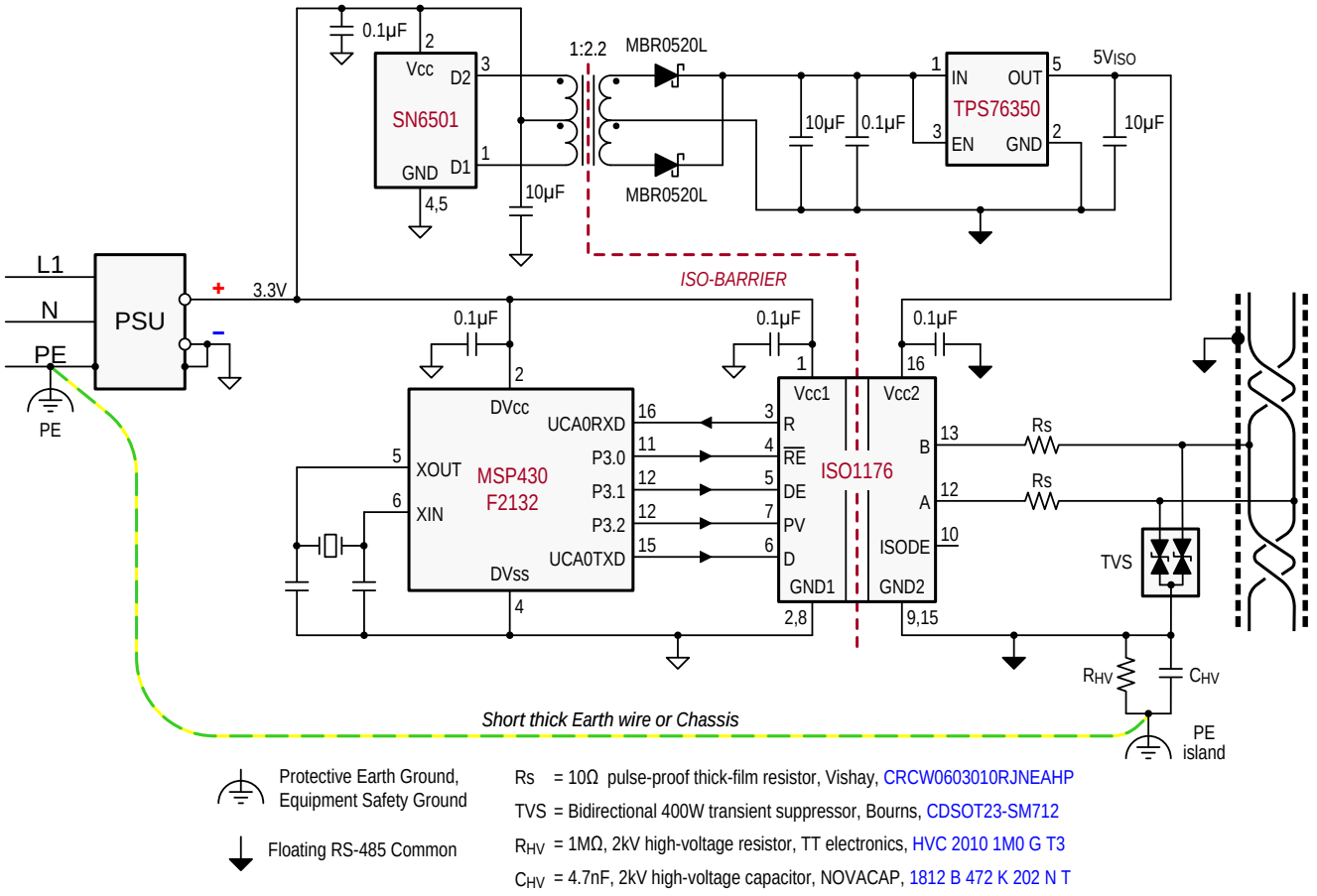

Figure 1. Isolated bus node with transient protection

Power isolation is accomplished using the push-pull transformer driver SN6501 and a low-cost LDO, TLV70733.

Signal isolation utilizes the quadruple digital isolator ISO7241. Notice that both enable inputs, EN1 and EN2, are pulled-up via 4.7k resistors to limit their input currents during transient events.

While the transient protection is similar to the one in Figure A9 (left circuit), an additional high-voltage capacitor is used to divert transient energy from the floating RS-485 common further towards Protective Earth (PE) ground. This is necessary as noise transients on the bus are usually referred to Earth potential.

R_{VH} refers to a high-voltage resistor, and in some applications even a varistor. This resistance is applied to prevent charging of the floating ground to dangerous potentials during normal operation.

Occasionally varistors are used instead of resistors in order to rapidly discharge C_{HV}, if it is expected that fast transients might charge CHV to high-potentials.

Note that the PE island represents a copper island on the PCB for the provision of a short, thick Earth wire connecting this island to PE ground at the entrance of the power supply unit (PSU).

In equipment designs using a chassis, the PE connection is usually provided through the chassis itself. Typically the PE conductor is tied to the chassis at one end while the high-voltage components, C_{HV} and R_{HV}, are connecting to the chassis at the other end.

Design and Layout Considerations for Transient Protection

On-chip IEC-ESD protection is good for laboratory and portable equipment but never sufficient for EFT and surge transients occurring in industrial environments. Therefore robust and reliable bus node design requires the use of external transient protection devices.

Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high-frequency layout techniques must be applied during PCB design.

In order for your PCB design to be successful start with the design of the protection circuit in mind.

1) Place the protection circuitry close to the bus connector to prevent noise transients from penetrating your board.
2) Use Vcc and ground planes to provide low-inductance. Note that high-frequency currents follow the path of least inductance and not the path of least impedance.
3) Design the protection components into the direction of the signal path. Do not force the transients currents to divert from the signal path to reach the protection device.
4) Apply 100 nF to 220 nF bypass capacitors as close as possible to the Vcc-pins of transceiver, UART, controller ICs on the board.
5) Use at least two vias for Vcc and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.
6) Use 1k to 10k pull-up/down resistors for enable lines to limit noise currents in theses lines during transient events.
7) Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus terminals. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
8) While pure TVS protection is sufficient for surge transients up to 1kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.